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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21367cnfa-u0

1.2 Product List

Tables 1.3 and 1.4 list Product List for R8C/36C Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/36C Group.

Table 1.3 Product List for R8C/36C Group (1)

Current of Nov 2010

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F21364CNFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	N version	
R5F21365CNFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CNFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CNFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CNFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACNFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CNFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CNFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CNFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CNFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CNFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACNFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CNFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A	N version	Factory programming product ⁽¹⁾
R5F21365CNFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CNFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CNFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CNFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACNFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCNFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		
R5F21364CNXXXFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A		
R5F21365CNXXXFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CNXXXFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CNXXXFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CNXXXFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACNXXXFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCNXXXFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CNXXXFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CNXXXFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CNXXXFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CNXXXFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CNXXXFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACNXXXFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCNXXXFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CNXXXFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CNXXXFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CNXXXFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CNXXXFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CNXXXFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACNXXXFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCNXXXFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		

(D): Under development

Note:

1. The user ROM is programmed before shipment.

Table 1.4 Product List for R8C/36C Group (2)

Current of Nov 2010

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F21364CDFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	D version	
R5F21365CDFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CDFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CDFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CDFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACDFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CDFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CDFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CDFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CDFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CDFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACDFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CDFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CDFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CDFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CDFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CDFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACDFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCDFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		
R5F21364CDXXXFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	N version	Factory programming product
R5F21365CDXXXFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CDXXXFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CDXXXFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CDXXXFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACDXXXFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCDXXXFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CDXXXFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CDXXXFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CDXXXFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CDXXXFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CDXXXFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACDXXXFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCDXXXFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CDXXXFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CDXXXFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CDXXXFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CDXXXFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CDXXXFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACDXXXFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCDXXXFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		

(D): Under development

Note:

1. The user ROM is programmed before shipment.

Table 1.6 Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B
40		P4_5	INT0		(RXD2/SCL2)			ADTRG
41		P1_7	INT1	(TRAIO)				IVCMP1
42		P1_6			(CLK0)			IVREF1
43		P1_5	(INT1)	(TRAIO)	(RXD0)			
44		P1_4		(TRCCLK)	(TXD0)			
45		P1_3	KI3	TRBO (/TRCIOB)				AN11
46		P1_2	KI2	(TRCIOB)				AN10
47		P1_1	KI1	(TRCIOA/TRCTRG)				AN9
48		P1_0	KI0	(TRCIOD)				AN8
49		P0_7		(TRCIOB)				AN0/DA1
50		P0_6		(TRCIOD)				AN1/DA0
51		P0_5		(TRCIOB)				AN2
52		P0_4		TREO(/TRCIOB)				AN3
53		P0_3		(TRCIOB)	(CLK1)			AN4
54		P0_2		(TRCIOA/TRCTRG)	(RXD1)			AN5
55		P0_1		(TRCIOA/TRCTRG)	(TXD1)			AN6
56		P0_0		(TRCIOA/TRCTRG)				AN7
57		P6_4			(RXD1)			
58		P6_3			(TXD1)			
59		P6_2			(CLK1)			
60		P6_1						
61		P6_0		(TREO)				
62		P5_7		(TRGIOB)				
63		P5_6		(TRA0/TRGIOA)				
64		P3_2	(INT1/ INT2)	(TRAIO/TRGCLKB)				

Note:

1. Can be assigned to the pin in parentheses by a program.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTs	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h	Pull-Up Control Register 2	PUR2	00h
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h	Port P2 Drive Capacity Control Register	P2DRR	00h
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h	Drive Capacity Control Register 2	DRR2	00h
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) ⁽¹⁾

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
⋮			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
⋮			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
⋮			
FFDFh	ID1		(Note 2)
⋮			
FFE3h	ID2		(Note 2)
⋮			
FFEBh	ID3		(Note 2)
⋮			
FFEFh	ID4		(Note 2)
⋮			
FFF3h	ID5		(Note 2)
⋮			
FFF7h	ID6		(Note 2)
⋮			
FFFBh	ID7		(Note 2)
⋮			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

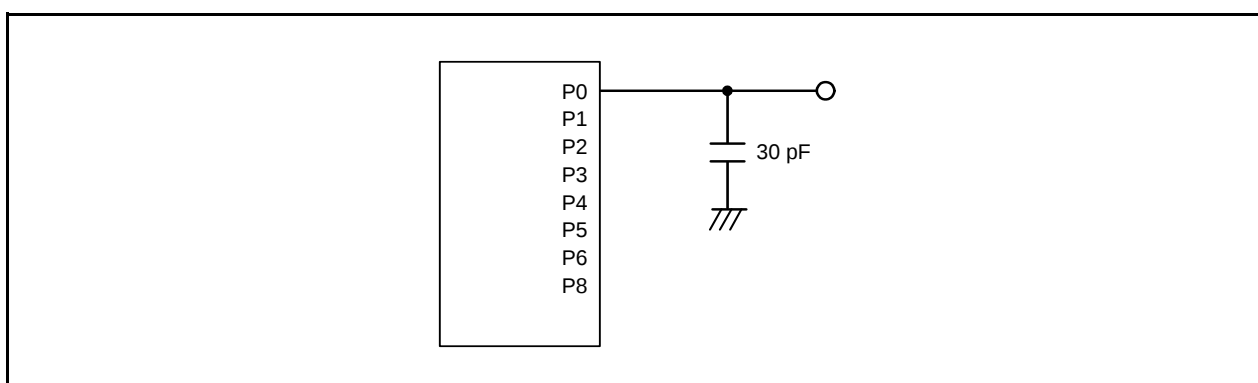


Figure 5.1 Ports P0 to P6, P8 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVCC		—	—	10	Bit
—	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±3	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	20	MHz
			3.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	16	MHz
			2.7 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	10	MHz
			2.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5.0 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				2.2	—	AVCC	V
VIA	Analog input voltage (3)				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.2\text{ to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, and $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level Vdet0_0 ⁽²⁾		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 ⁽²⁾		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 ⁽²⁾		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 ⁽²⁾		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time ⁽⁴⁾	At the falling of Vcc from 5.0 V to (Vdet0_0 – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_0 ⁽²⁾	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 ⁽²⁾	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 ⁽²⁾	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 ⁽²⁾	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 ⁽²⁾	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 ⁽²⁾	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽²⁾	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 ⁽²⁾	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 ⁽²⁾	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 ⁽²⁾	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A ⁽²⁾	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B ⁽²⁾	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C ⁽²⁾	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D ⁽²⁾	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E ⁽²⁾	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F ⁽²⁾	At the falling of Vcc	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽³⁾	At the falling of Vcc from 5.0 V to (Vdet1_0 – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.10 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time (2)	At the falling of Vcc from 5.0 V to (Vdet2_0 – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts (3)		—	—	100	μs

Notes:

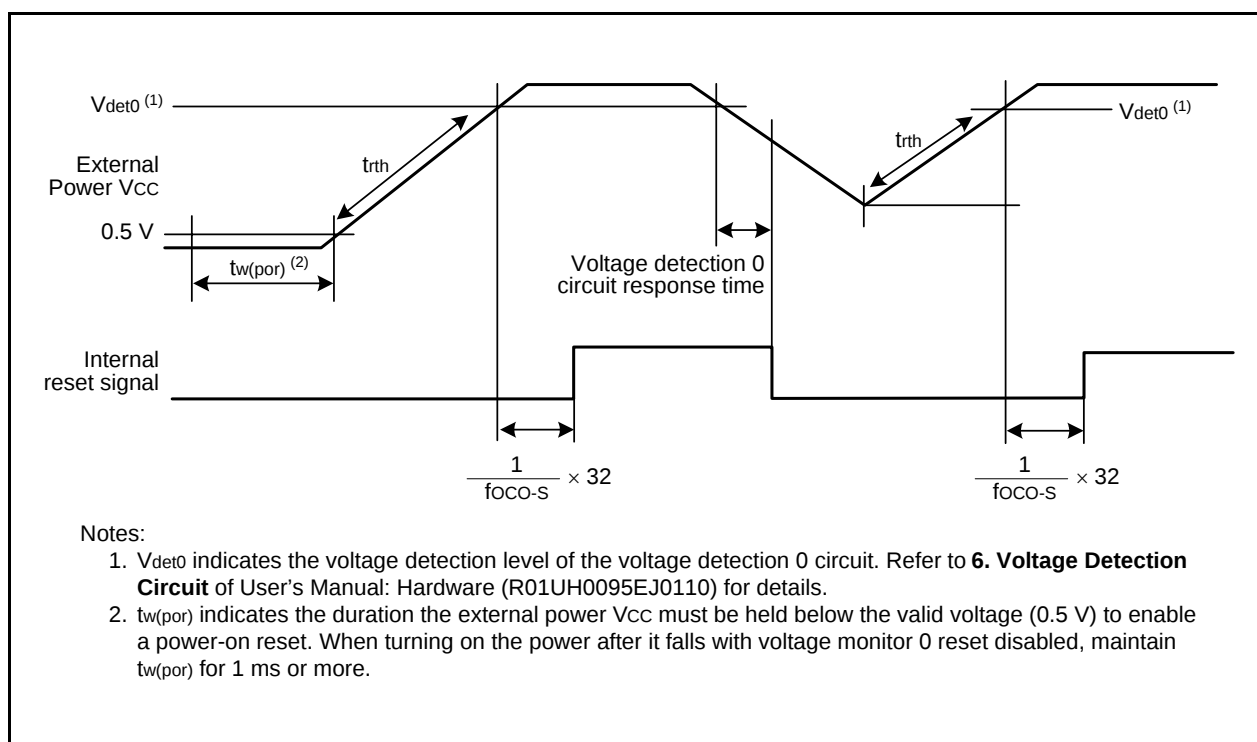
1. The measurement condition is Vcc = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
trth	External power Vcc rise gradient	(1)	0	—	50,000	mV/msec

Notes:

1. The measurement condition is T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

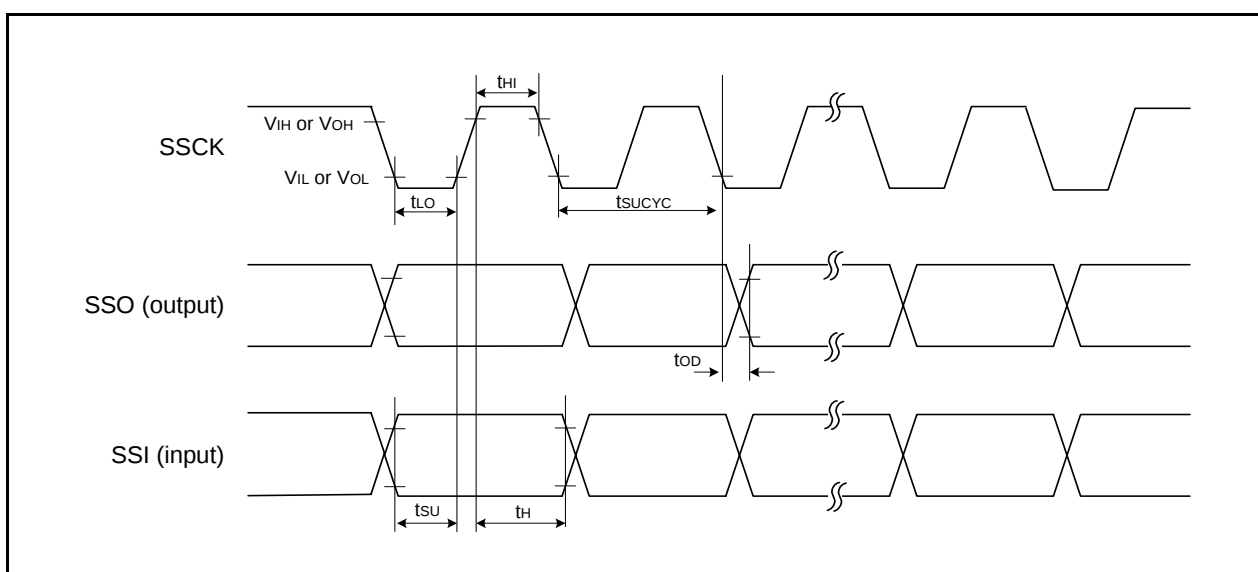


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.17 Electrical Characteristics (1) [4.2 V ≤ V_{CC} ≤ 5.5 V]

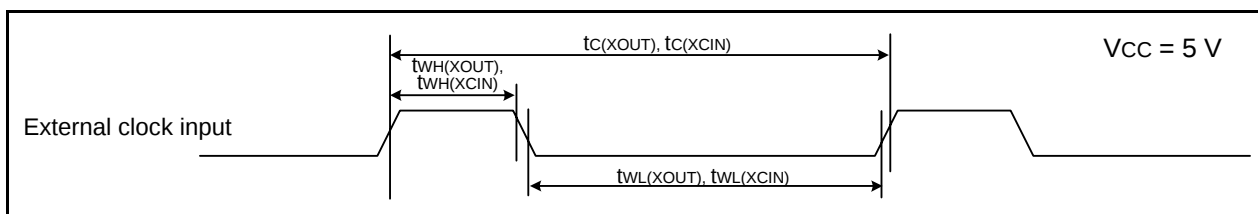
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High V _{CC} = 5 V	I _{OH} = −20 mA	V _{CC} − 2.0	—	V _{CC}	V
			Drive capacity Low V _{CC} = 5 V	I _{OH} = −5 mA	V _{CC} − 2.0	—	V _{CC}	V
		XOUT	V _{CC} = 5 V	I _{OH} = −200 μA	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High V _{CC} = 5 V	I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity Low V _{CC} = 5 V	I _{OL} = 5 mA	—	—	2.0	V
		XOUT	V _{CC} = 5 V	I _{OL} = 200 μA	—	—	0.5	V
V _{T+} –V _{T–}	Hysteresis	INT0, INT1, INT2, INT3, INT4, K10, K11, K12, K13, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, TRGIOA, TRGIOB, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5.0 V		—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5.0 V		—	—	−5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5.0 V		25	50	100	kΩ
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

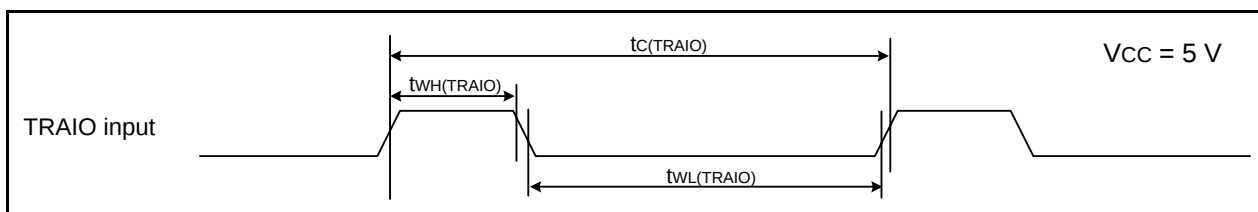
- 4.2 V ≤ V_{CC} ≤ 5.5 V, T_{opr} = −20 to 85 °C (N version)/−40 to 85 °C (D version), and f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements (Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_{opr} = 25\text{ }^{\circ}\text{C}$)**Table 5.19 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input "H" width	24	—	ns
$t_{WL(XOUT)}$	XOUT input "L" width	24	—	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	—	μs
$t_{WH(XCIN)}$	XCIN input "H" width	7	—	μs
$t_{WL(XCIN)}$	XCIN input "L" width	7	—	μs

**Figure 5.8 External Clock Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.20 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	—	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	—	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	—	ns

**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.21 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	400 (1)	—	ns
$t_{WH(TRFI)}$	TRFI input "H" width	200 (2)	—	ns
$t_{WL(TRFI)}$	TRFI input "L" width	200 (2)	—	ns

Notes:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

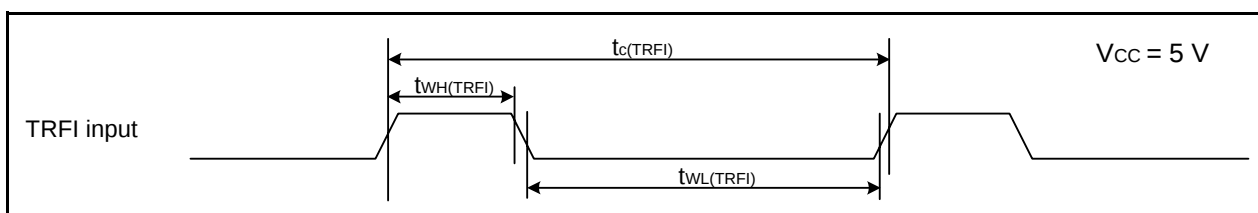
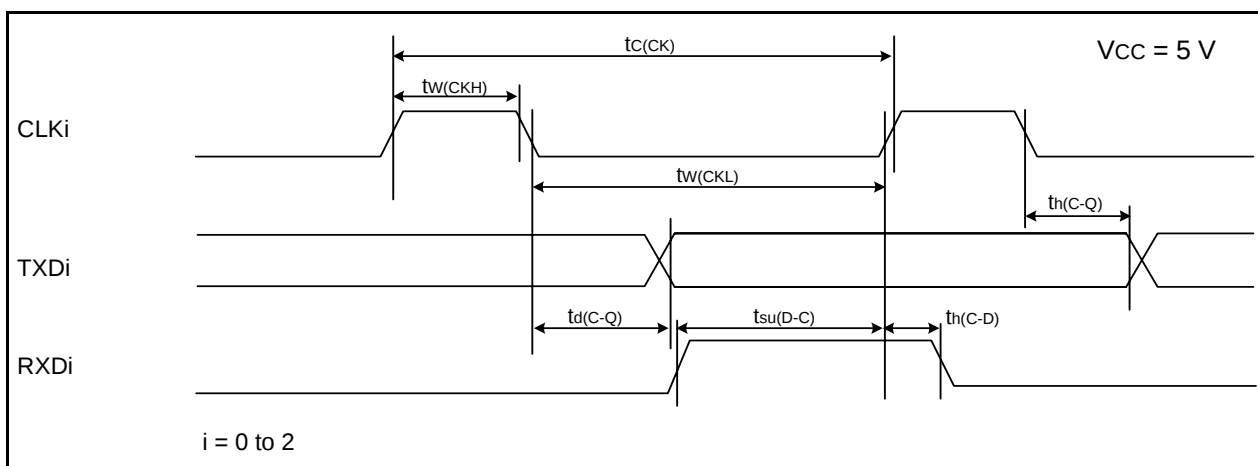
**Figure 5.10 TRFI Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.22 Serial Interface

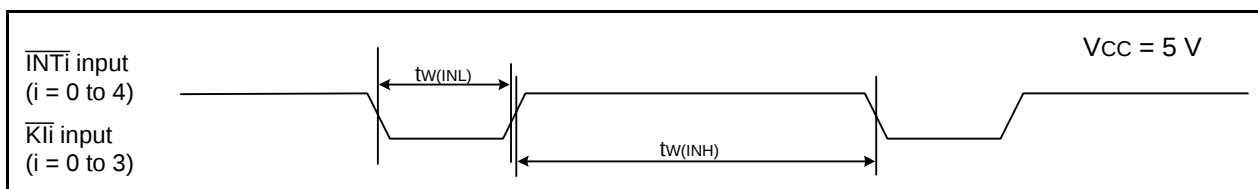
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.11 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.23 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 4$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	250 ⁽²⁾	—	ns

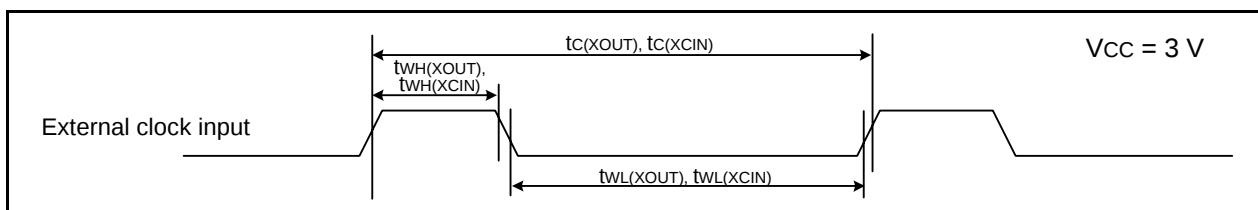
Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

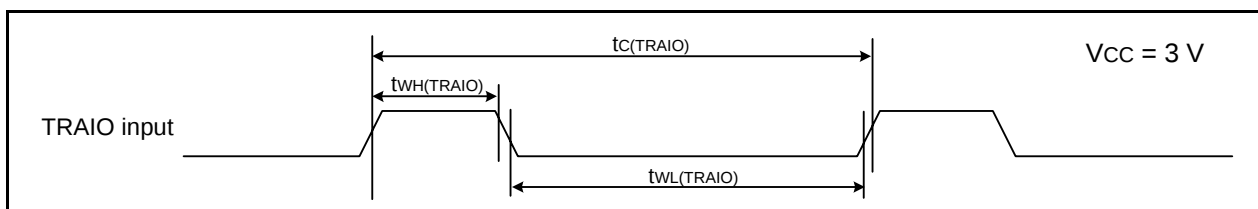
**Figure 5.12 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 5 V**

Timing requirements (Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_{opr} = 25\text{ }^{\circ}\text{C}$)**Table 5.26 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(XOUT)$	XOUT input cycle time	50	—	ns
$t_{WH}(XOUT)$	XOUT input "H" width	24	—	ns
$t_{WL}(XOUT)$	XOUT input "L" width	24	—	ns
$t_c(XCIN)$	XCIN input cycle time	14	—	μs
$t_{WH}(XCIN)$	XCIN input "H" width	7	—	μs
$t_{WL}(XCIN)$	XCIN input "L" width	7	—	μs

**Figure 5.13 External Clock Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.27 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TRAIO)$	TRAIO input cycle time	300	—	ns
$t_{WH}(TRAIO)$	TRAIO input "H" width	120	—	ns
$t_{WL}(TRAIO)$	TRAIO input "L" width	120	—	ns

**Figure 5.14 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.28 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TRFI)$	TRFI input cycle time	1200 (1)	—	ns
$t_{WH}(TRFI)$	TRFI input "H" width	600 (2)	—	ns
$t_{WL}(TRFI)$	TRFI input "L" width	600 (2)	—	ns

Notes:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

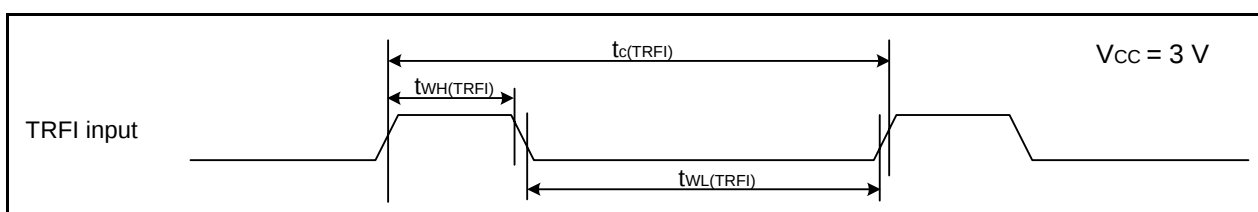
**Figure 5.15 TRFI Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.31 Electrical Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]

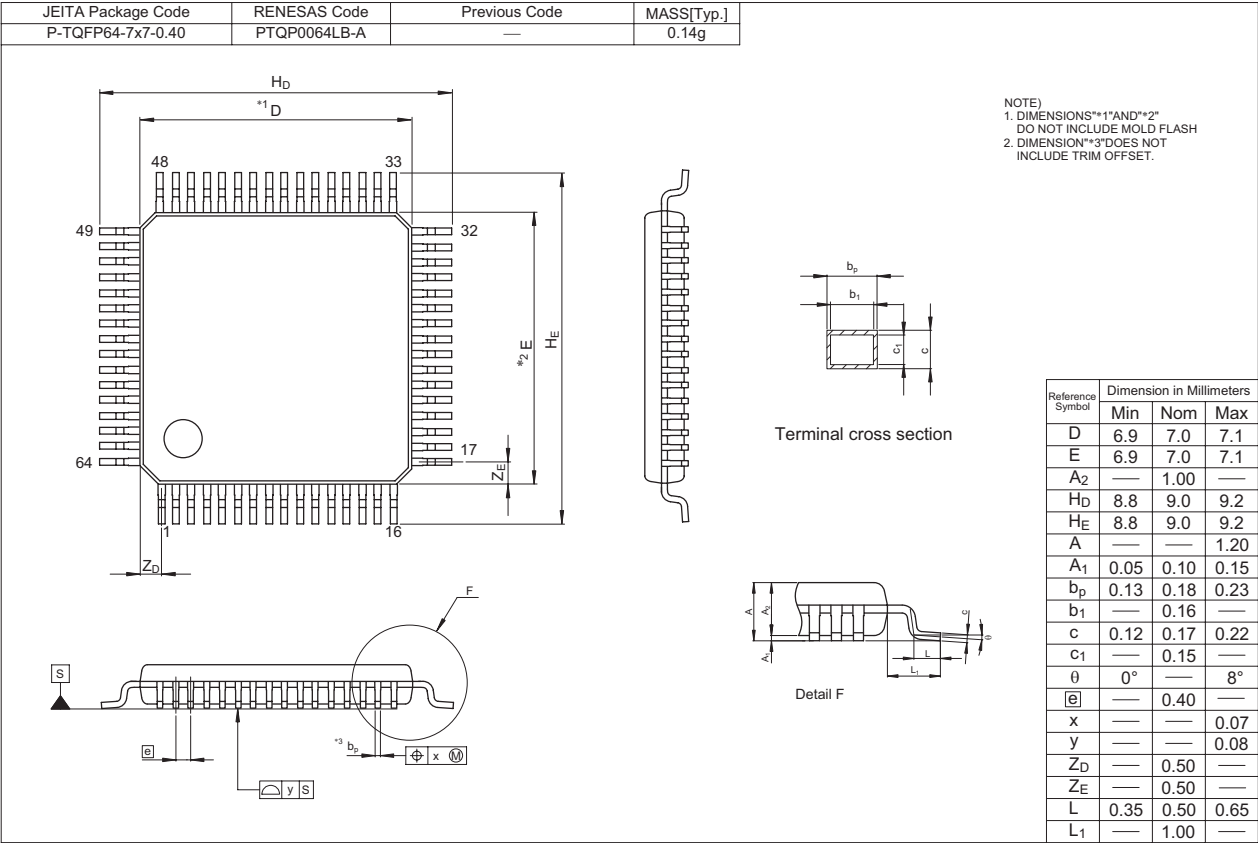
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	NT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, TRGIOA, TRGIOB, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.05	0.20	—	V
		RESET			0.05	0.20	—	V
I _{IH}	Input "H" current		V _I = 2.2 V, V _{CC} = 2.2 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 2.2 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 2.2 V		70	140	300	k Ω
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$, T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), and f(XIN) = 5 MHz, unless otherwise specified.

Table 5.32 Electrical Characteristics (6) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current ($V_{CC} = 1.8\text{ to }2.7\text{ V}$) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	2.2	—	mA
				0.8	—	mA
		High-speed on-chip oscillator mode	—	2.5	10	mA
			—	1.7	—	mA
			—	1	—	mA
		Low-speed on-chip oscillator mode	—	90	300	μA
		Low-speed clock mode	—	80	350	μA
			—	40	—	μA
			—	15	90	μA
		Wait mode	—	4	80	μA
			—	3.5	—	μA
			—	2.0	5	μA
		Stop mode	—	15	—	μA



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