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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21368cdfa-30

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/36C Group.

Table 1.1 Specifications for R8C/36C Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 50 ns ($f(XIN) = 20$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 1.8$ to 5.5 V) • Multiplier: 16 bits \times 16 bits \rightarrow 32 bits • Multiply-accumulate instruction: 16 bits \times 16 bits + 32 bits \rightarrow 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to Table 1.3 Product List for R8C/36C Group
Power Supply Voltage Detection	Voltage detection circuit	<ul style="list-style-type: none"> • Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	<ul style="list-style-type: none"> • Input-only: 1 pin • CMOS I/O ports: 59, selectable pull-up resistor • High current drive ports: 59
Clock	Clock generation circuits	<ul style="list-style-type: none"> • 4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: <ul style="list-style-type: none"> Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		<ul style="list-style-type: none"> • Interrupt Vectors: 69 • External: 9 sources ($\overline{INT} \times 5$, key input $\times 4$) • Priority levels: 7 levels
Watchdog Timer		<ul style="list-style-type: none"> • 14 bits \times 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		<ul style="list-style-type: none"> • 1 channel • Activation sources: 39 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits \times 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits \times 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)

1.2 Product List

Tables 1.3 and 1.4 list Product List for R8C/36C Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/36C Group.

Table 1.3 Product List for R8C/36C Group (1)

Current of Nov 2010

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F21364CNFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	N version	
R5F21365CNFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CNFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CNFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CNFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACNFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CNFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CNFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CNFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CNFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CNFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACNFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CNFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CNFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CNFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CNFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CNFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACNFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCNFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		
R5F21364CNXXXFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	N version Factory programming product (1)	
R5F21365CNXXXFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CNXXXFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CNXXXFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CNXXXFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACNXXXFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCNXXXFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CNXXXFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CNXXXFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CNXXXFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CNXXXFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CNXXXFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACNXXXFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCNXXXFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CNXXXFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CNXXXFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CNXXXFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CNXXXFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CNXXXFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACNXXXFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCNXXXFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		

(D): Under development

Note:

1. The user ROM is programmed before shipment.

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.5 and 1.6 outline the Pin Name Information by Pin Number.

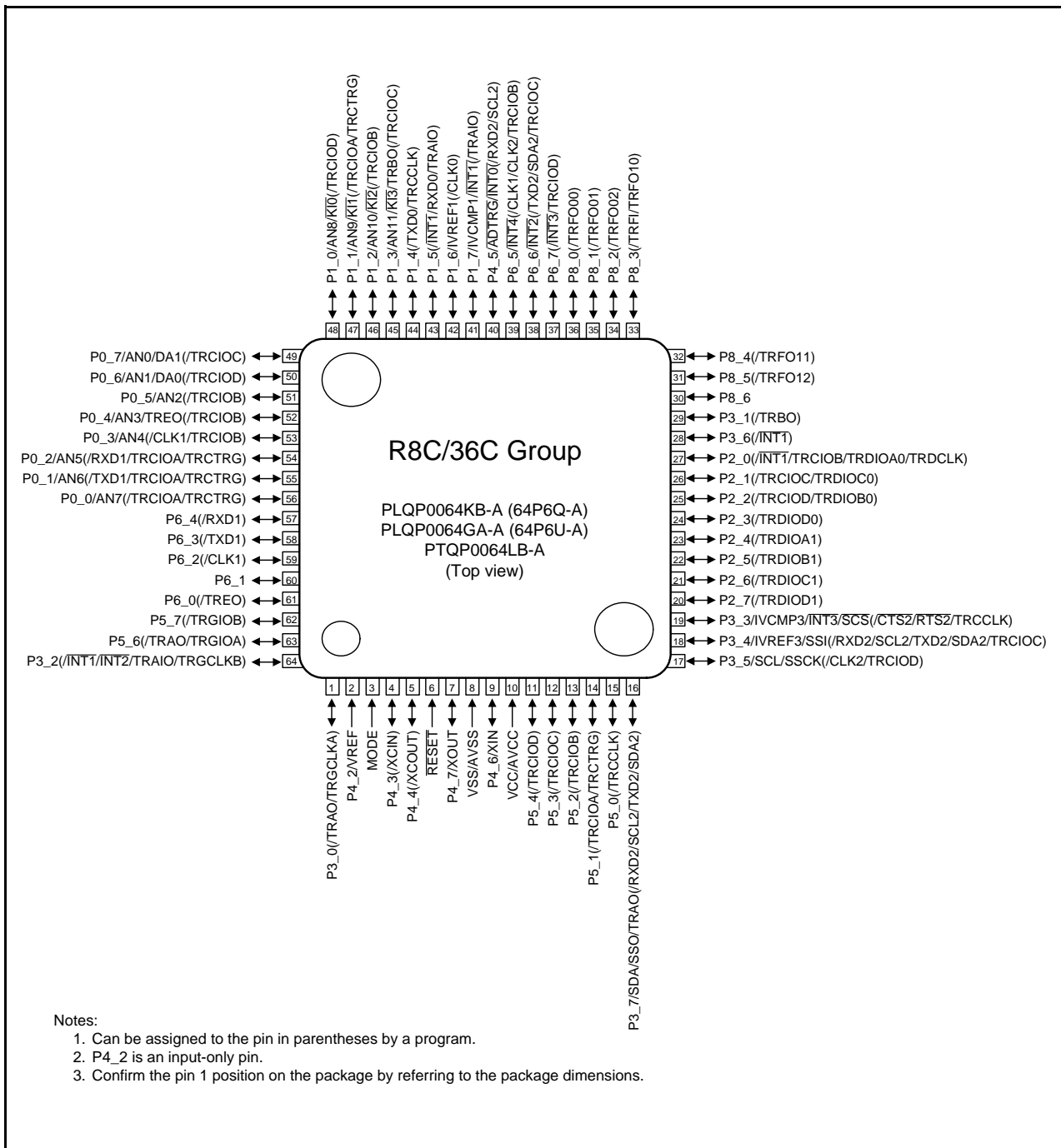


Figure 1.3 Pin Assignment (Top View)

Table 1.5 Pin Name Information by Pin Number (1)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B
1		P3_0		(TRAO/TRGCLKA)				
2		P4_2						VREF
3	MODE							
4	(XCIN)	P4_3						
5	(XCOUT)	P4_4						
6	RESET							
7	XOUT	P4_7						
8	VSS/AVSS							
9	XIN	P4_6						
10	VCC/AVCC							
11		P5_4		(TRCIOD)				
12		P5_3		(TRCIOC)				
13		P5_2		(TRCIOB)				
14		P5_1		(TRCIOA/TRCTRG)				
15		P5_0		(TRCCLK)				
16		P3_7		TRAO	(TXD2/SDA2/ RXD2/SCL2)	SSO	SDA	
17		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
18		P3_4		(TRCIOC)	(TXD2/SDA2/ RXD2/SCL2)	SSI		IVREF3
19		P3_3	INT3	(TRCCLK)	(CTS2/RTS2)	SCS		IVCMP3
20		P2_7		(TRDIOD1)				
21		P2_6		(TRDIOC1)				
22		P2_5		(TRDIOB1)				
23		P2_4		(TRDIOA1)				
24		P2_3		(TRDIOD0)				
25		P2_2		(TRCIOD/TRDIOB0)				
26		P2_1		(TRCIOC/TRDIOC0)				
27		P2_0	(INT1)	(TRCIOB/TRDIOA0/ TRDCLK)				
28		P3_6	(INT1)					
29		P3_1		(TRBO)				
30		P8_6						
31		P8_5		(TRFO12)				
32		P8_4		(TRFO11)				
33		P8_3		(TRFI/TRFO10)				
34		P8_2		(TRFO02)				
35		P8_1		(TRFO01)				
36		P8_0		(TRFO00)				
37		P6_7	(INT3)	(TRCIOD)				
38		P6_6	INT2	(TRCIOC)	(TXD2/SDA2)			
39		P6_5	INT4	(TRCIOB)	(CLK2/CLK1)			

Note:

1. Can be assigned to the pin in parentheses by a program.

Table 1.8 Pin Functions (2)

Item	Pin Name	I/O Type	Description
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter.
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter.
	$\overline{\text{ADTRG}}$	I	AD external trigger input pin.
D/A converter	DA0, DA1	O	D/A converter output pins.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Input port	P4_2	I	Input-only port.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

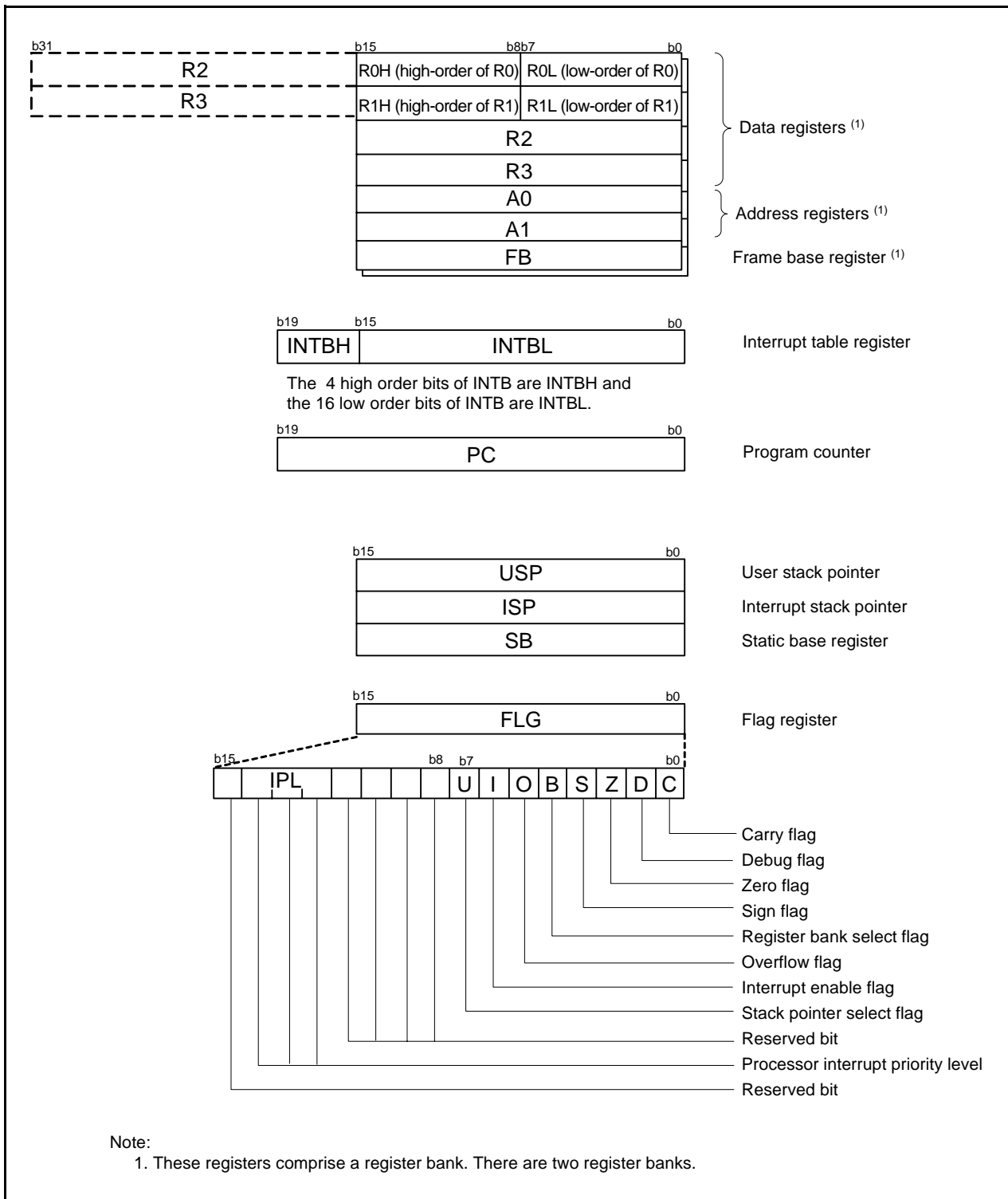


Figure 2.1 CPU Registers

3. Memory

3.1 R8C/36C Group

Figure 3.1 is a Memory Map of R8C/36C Group. The R8C/36C Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

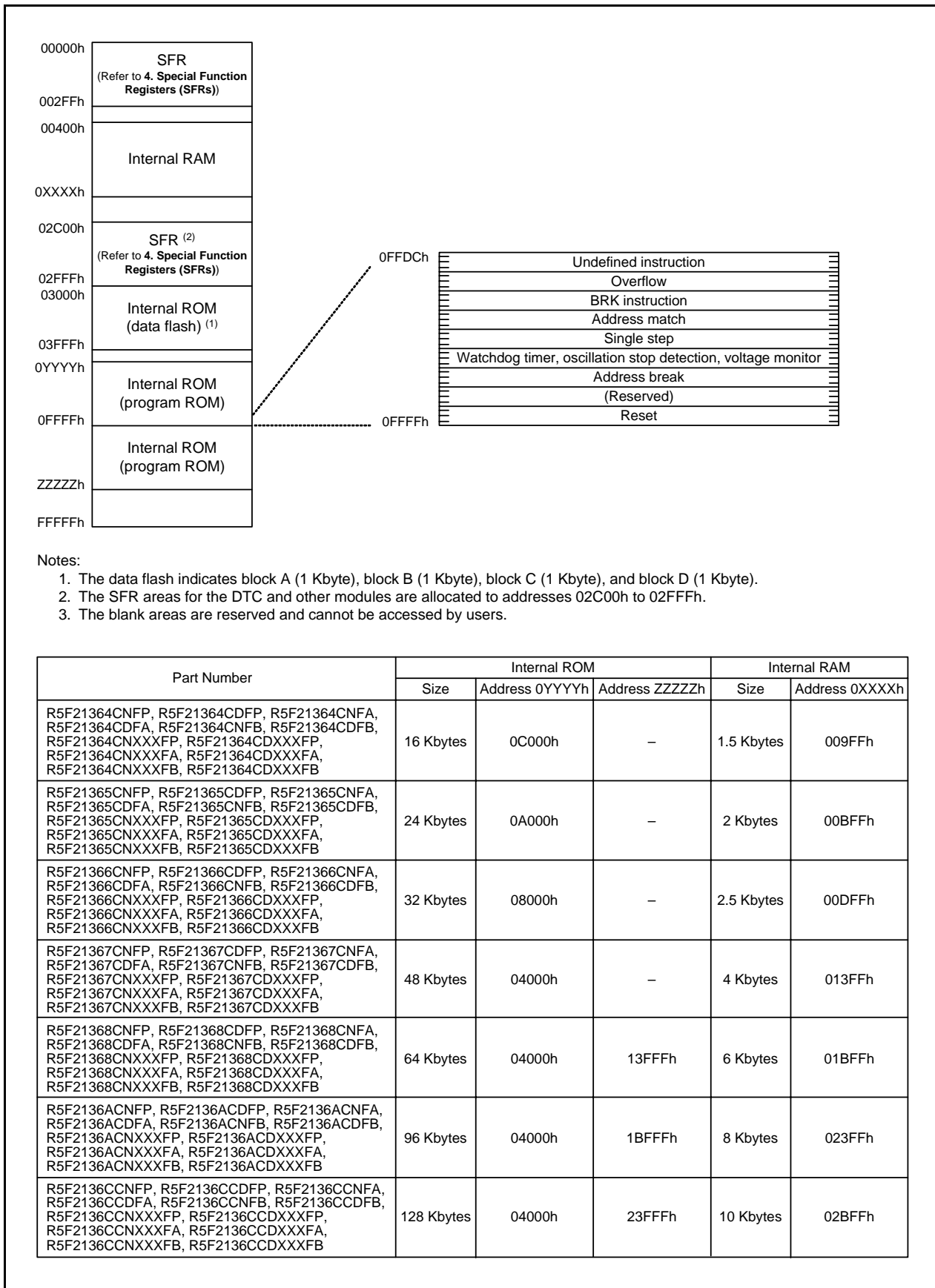


Figure 3.1 Memory Map of R8C/36C Group

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h	Timer RF Register	TRF	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah	Timer RF Control Register 0	TRFCR0	00h
009Bh	Timer RF Control Register 1	TRFCR1	00h
009Ch	Capture and Compare 0 Register	TRFM0	00h
009Dh			00h
009Eh	Compare 1 Register	TRFM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	00X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

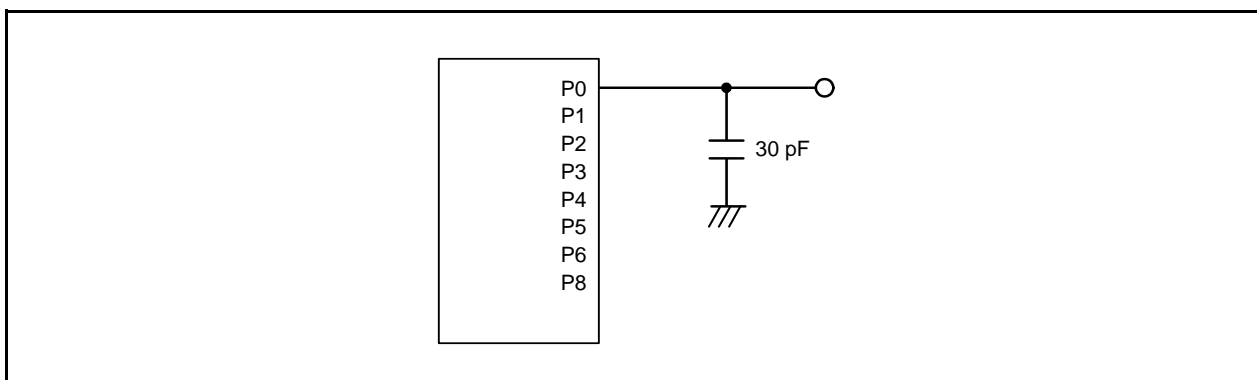


Figure 5.1 Ports P0 to P6, P8 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		$V_{ref} = AV_{CC}$		—	—	10	Bit
—	Absolute accuracy	10-bit mode	$V_{ref} = AV_{CC} = 5.0\text{ V}$	AN0 to AN7 input, AN8 to AN11 input	—	—	± 3	LSB
			$V_{ref} = AV_{CC} = 3.3\text{ V}$	AN0 to AN7 input, AN8 to AN11 input	—	—	± 5	LSB
			$V_{ref} = AV_{CC} = 3.0\text{ V}$	AN0 to AN7 input, AN8 to AN11 input	—	—	± 5	LSB
			$V_{ref} = AV_{CC} = 2.2\text{ V}$	AN0 to AN7 input, AN8 to AN11 input	—	—	± 5	LSB
		8-bit mode	$V_{ref} = AV_{CC} = 5.0\text{ V}$	AN0 to AN7 input, AN8 to AN11 input	—	—	± 2	LSB
			$V_{ref} = AV_{CC} = 3.3\text{ V}$	AN0 to AN7 input, AN8 to AN11 input	—	—	± 2	LSB
			$V_{ref} = AV_{CC} = 3.0\text{ V}$	AN0 to AN7 input, AN8 to AN11 input	—	—	± 2	LSB
			$V_{ref} = AV_{CC} = 2.2\text{ V}$	AN0 to AN7 input, AN8 to AN11 input	—	—	± 2	LSB
ϕ_{AD}	A/D conversion clock		$4.0\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}^{(2)}$		2	—	20	MHz
			$3.2\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}^{(2)}$		2	—	16	MHz
			$2.7\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}^{(2)}$		2	—	10	MHz
			$2.2\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}^{(2)}$		2	—	5	MHz
—	Tolerance level impedance				—	3	—	$k\Omega$
t_{CONV}	Conversion time	10-bit mode	$V_{ref} = AV_{CC} = 5.0\text{ V}$, $\phi_{AD} = 20\text{ MHz}$		2.2	—	—	μs
		8-bit mode	$V_{ref} = AV_{CC} = 5.0\text{ V}$, $\phi_{AD} = 20\text{ MHz}$		2.2	—	—	μs
t_{SAMP}	Sampling time		$\phi_{AD} = 20\text{ MHz}$		0.8	—	—	μs
I_{Vref}	V_{ref} current		$V_{CC} = 5.0\text{ V}$, $XIN = f_1 = \phi_{AD} = 20\text{ MHz}$		—	45	—	μA
V_{ref}	Reference voltage				2.2	—	AV_{CC}	V
V_{IA}	Analog input voltage ⁽³⁾				0	—	V_{ref}	V
OCVREF	On-chip reference voltage		$2\text{ MHz} \leq \phi_{AD} \leq 4\text{ MHz}$		1.19	1.34	1.49	V

Notes:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_{opr} = -20$ to $85\text{ }^\circ\text{C}$ (N version)/ -40 to $85\text{ }^\circ\text{C}$ (D version), unless otherwise specified.
- The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
t_{su}	Setup time		—	—	3	μs
R_o	Output resistor		—	6	—	$k\Omega$
I_{Vref}	Reference power input current	(Note 2)	—	—	1.5	mA

Notes:

- $V_{CC}/AV_{CC} = V_{ref} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.
- This applies when one D/A converter is used and the value of the DA $_i$ register ($i = 0$ or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	$V_{CC} - 1.4$	V
V_i	IVCMP1, IVCMP3 input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time ⁽²⁾	$V_i = V_{ref} \pm 100$ mV	—	0.1	—	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0$ V	—	17.5	—	μA

Notes:

- $V_{CC} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.
- When the digital filter is disabled.

Table 5.6 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

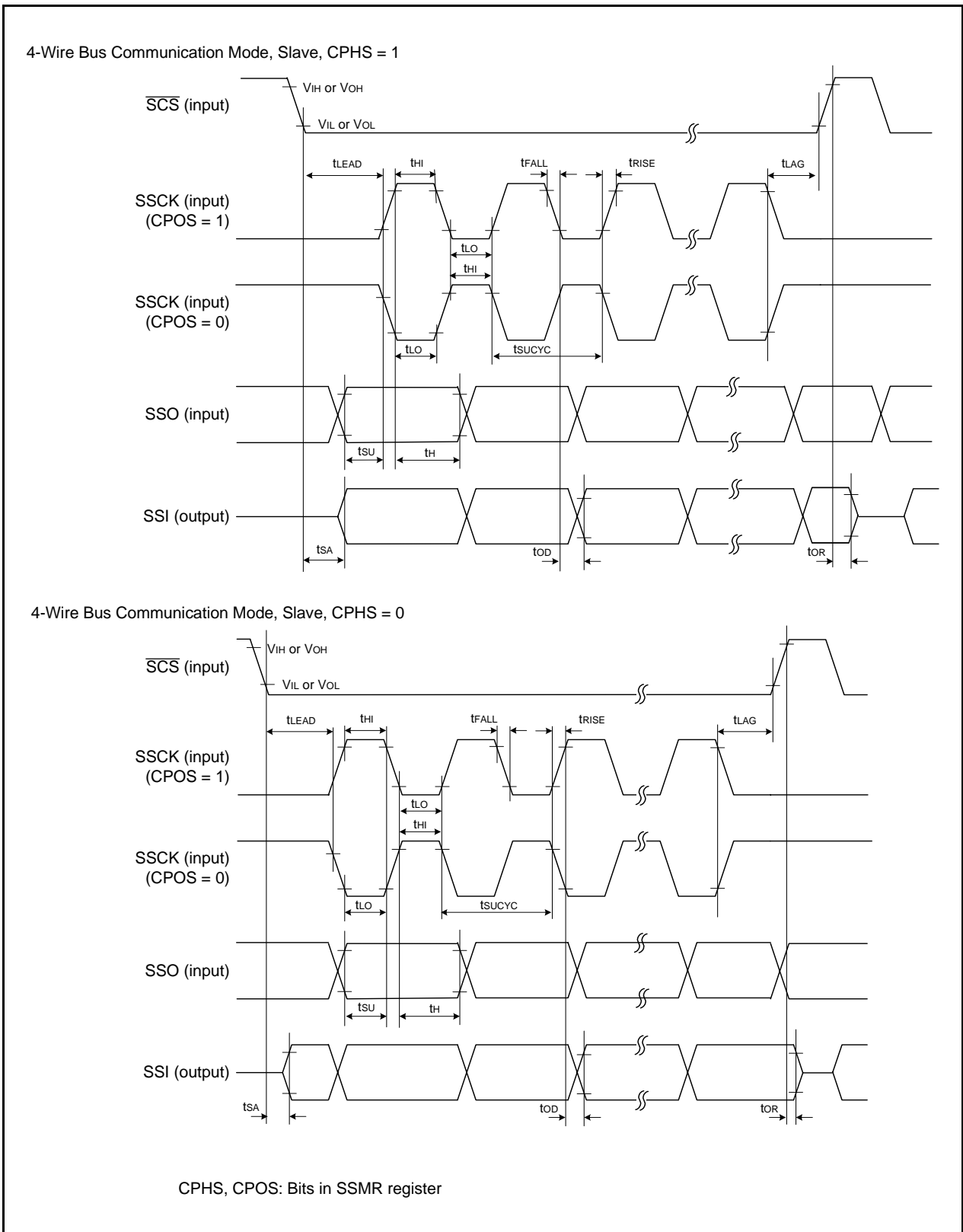


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 5.16 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{CYC} + 600 ⁽²⁾	—	—	ns
t _{SCLH}	SCL input "H" width		3t _{CYC} + 300 ⁽²⁾	—	—	ns
t _{SCLL}	SCL input "L" width		5t _{CYC} + 500 ⁽²⁾	—	—	ns
t _{Sf}	SCL, SDA input fall time		—	—	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		—	—	1t _{CYC} ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5t _{CYC} ⁽²⁾	—	—	ns
t _{STAH}	Start condition input hold time		3t _{CYC} ⁽²⁾	—	—	ns
t _{STAS}	Retransmit start condition input setup time		3t _{CYC} ⁽²⁾	—	—	ns
t _{STOP}	Stop condition input setup time		3t _{CYC} ⁽²⁾	—	—	ns
t _{SDAS}	Data input setup time		1t _{CYC} + 40 ⁽²⁾	—	—	ns
t _{SDAH}	Data input hold time		10	—	—	ns

Notes:

1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.
2. 1t_{CYC} = 1/f₁(s)

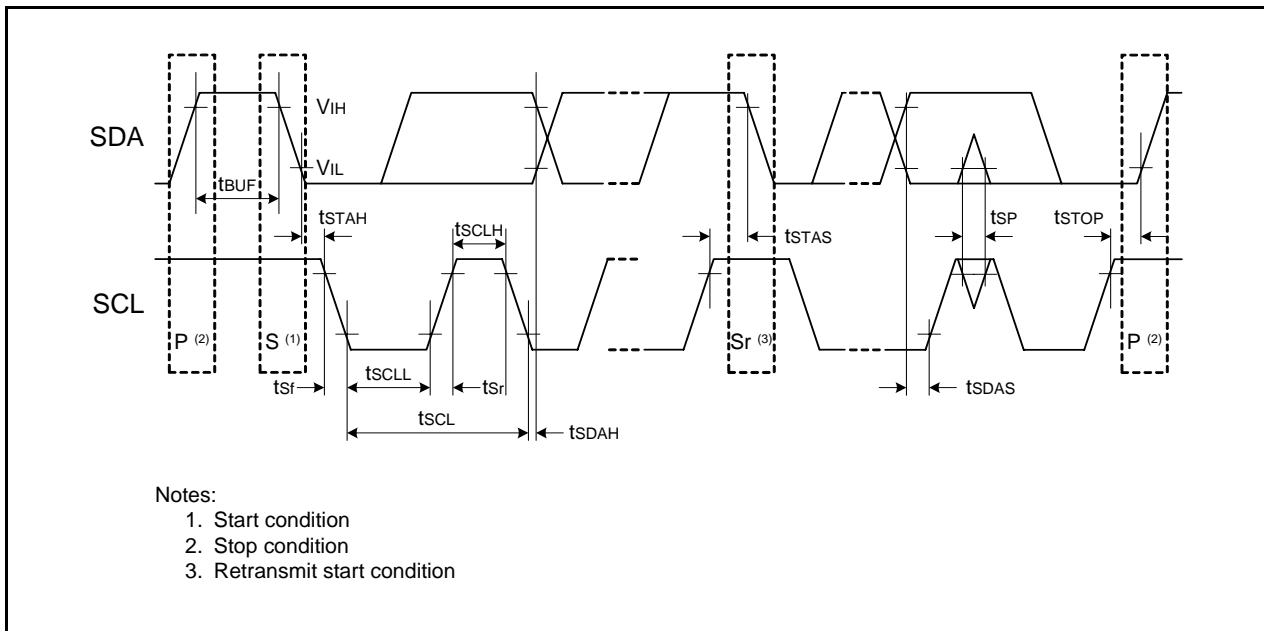
**Figure 5.7 I/O Timing of I²C bus Interface**

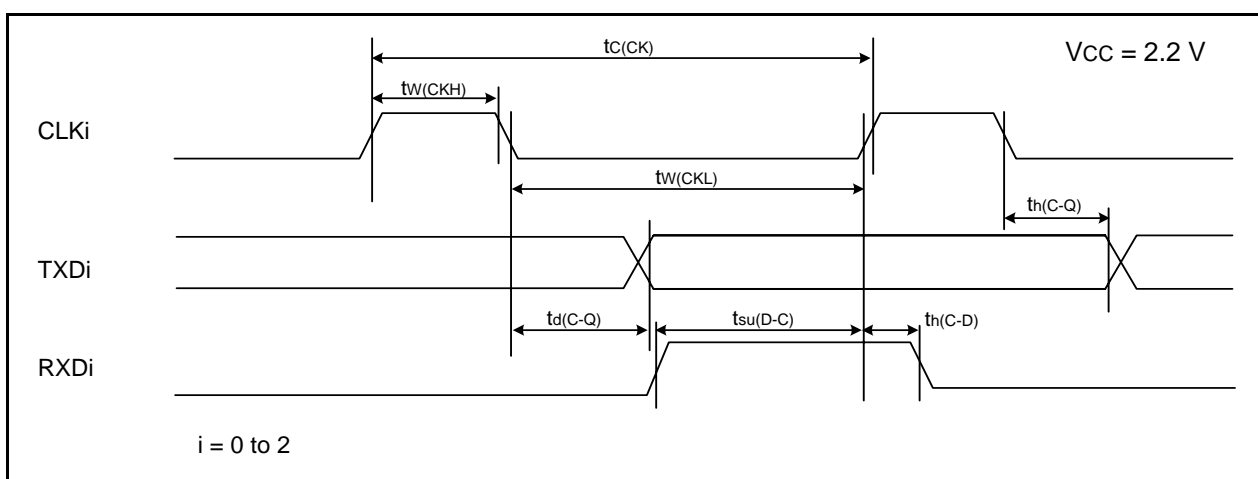
Table 5.18 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]
(Topr = −20 to 85 °C (N version)/−40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.2	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
			High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15
		XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8		—	3.0	—	mA
		XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRD = MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	400	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	—	85	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division	—	47	—	μA
			Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	—	—	—	—
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	100	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	μA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	μA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	μA

Table 5.36 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

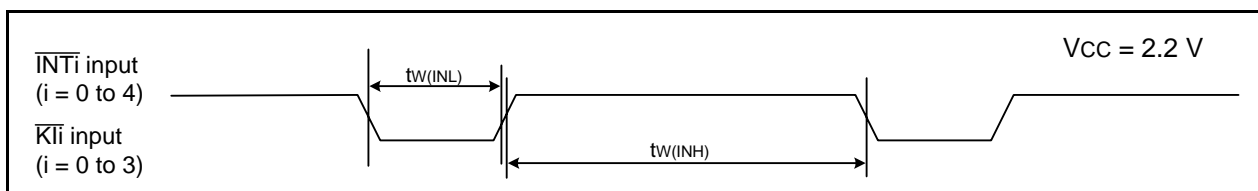
i = 0 to 2

**Figure 5.21 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.37 External Interrupt \overline{INTi} (i = 0 to 4) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input "H" width, \overline{Kli} input "H" width	1000 (1)	—	ns
$t_{w(INL)}$	\overline{INTi} input "L" width, \overline{Kli} input "L" width	1000 (2)	—	ns

Notes:

- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.

**Figure 5.22 Input Timing Diagram for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 2.2 V**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

