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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21368cdfa-50

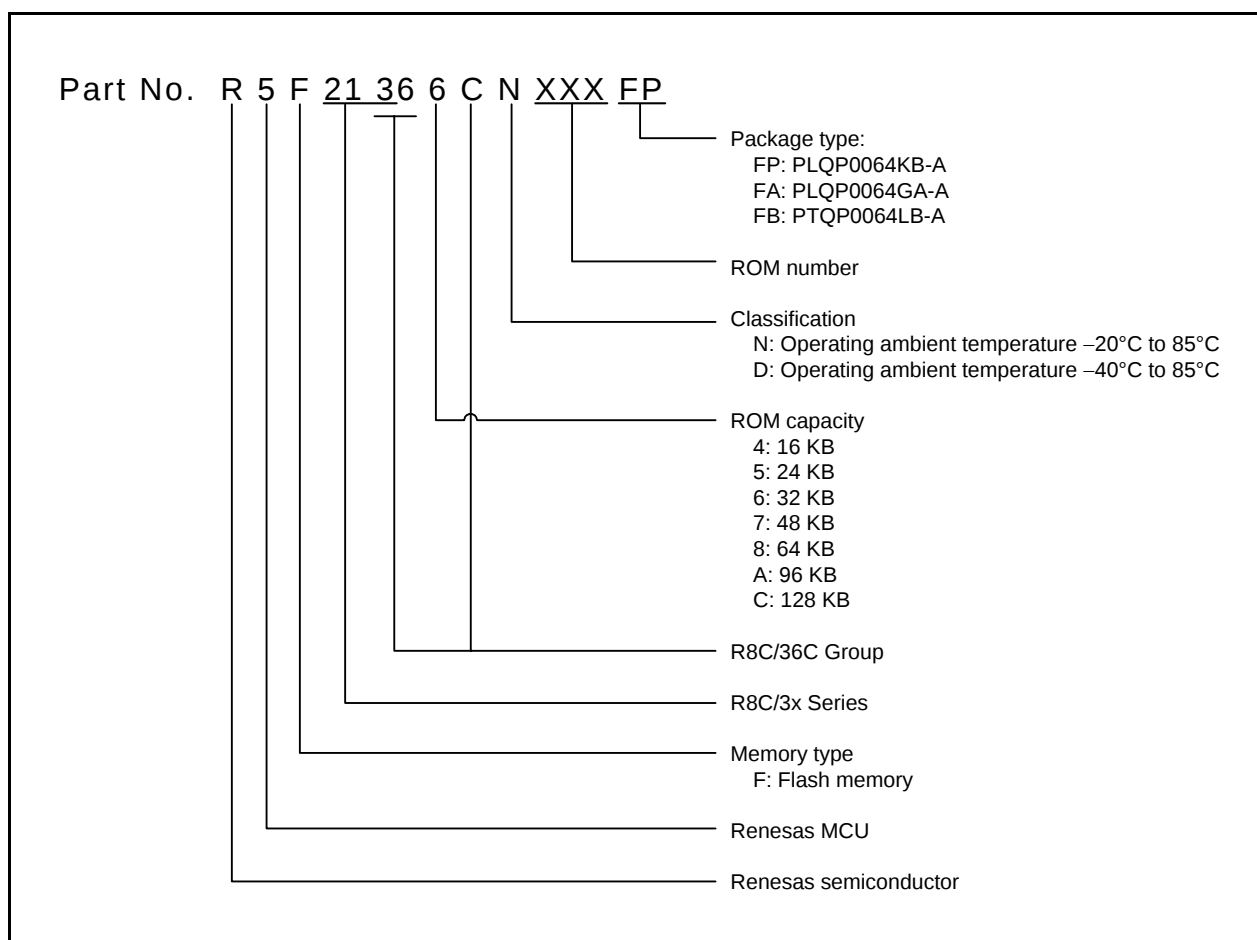


Figure 1.1 Part Number, Memory Size, and Package of R8C/36C Group

Table 1.8 Pin Functions (2)

Item	Pin Name	I/O Type	Description
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter.
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter.
	$\overline{\text{ADTRG}}$	I	AD external trigger input pin.
D/A converter	DA0, DA1	O	D/A converter output pins.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Input port	P4_2	I	Input-only port.

I: Input O: Output I/O: Input and output

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Table 4.2 SFR Information (2) ⁽¹⁾

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC bus Interrupt Control Register ⁽²⁾	SSUIC/IICIC	XXXXX000b
0050h	Timer RF Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Timer RF Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh	Timer RF Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	Timer RG Interrupt Control Register	TRGIC	XXXXX000b
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUICSR register.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h	Timer RF Register	TRF	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah	Timer RF Control Register 0	TRFCR0	00h
009Bh	Timer RF Control Register 1	TRFCR1	00h
009Ch	Capture and Compare 0 Register	TRFM0	00h
009Dh			00h
009Eh	Compare 1 Register	TRFM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			XXh
00A9h	UART2 Transmit/Receive Mode Register	U2MR	00h
00AAh	UART2 Bit Rate Register	U2BRG	XXh
00ABh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.4 SFR Information (4) ⁽¹⁾

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h			XXh
00C3h	A/D Register 1	AD1	000000XXb
00C4h			XXh
00C5h			000000XXb
00C6h	A/D Register 2	AD2	XXh
00C7h			000000XXb
00C8h			XXh
00C9h	A/D Register 3	AD3	000000XXb
00CAh			XXh
00CBh			000000XXb
00CCh	A/D Register 4	AD4	XXh
00CDh			000000XXb
00CEh			XXh
00CFh	A/D Register 5	AD5	000000XXb
00D0h			XXh
00D1h			000000XXb
00D2h	A/D Register 6	AD6	XXh
00D3h			000000XXb
00D4h			XXh
00D5h	A/D Register 7	AD7	000000XXb
00D6h			XXh
00D7h			000000XXb
00D8h	A/D Mode Register	ADMOD	00h
00D9h			11000000b
00DAh			00h
00DBh	A/D Input Select Register	ADINSEL	00h
00DCh			00h
00DDh			00h
00DEh	A/D Control Register 0	ADCON0	00h
00DFh			00h
00E0h			00h
00E1h	A/D Control Register 1	ADCON1	00h
00E2h			00h
00E3h			00h
00E4h	D/A0 Register	DA0	00h
00E5h			00h
00E6h			00h
00E7h	D/A1 Register	DA1	00h
00E8h			00h
00E9h			00h
00EAh	D/A Control Register	DACON	00h
00EBh			00h
00ECh			00h
00EDh	Port P0 Register	P0	XXh
00EEh			XXh
00EFh			00h
00F0h	Port P1 Register	P1	00h
00F1h			00h
00F2h			00h
00F3h	Port P0 Direction Register	PD0	00h
00F4h			00h
00F5h			00h
00F6h	Port P1 Direction Register	PD1	00h
00F7h			00h
00F8h			00h
00F9h	Port P2 Register	P2	XXh
00FAh			XXh
00FBh			00h
00FCh	Port P3 Register	P3	00h
00FDh			00h
00FEh			00h
00FFh	Port P2 Direction Register	PD2	00h
			00h
			00h
	Port P3 Direction Register	PD3	00h
			00h
			00h
	Port P4 Register	P4	XXh
			XXh
			00h
	Port P5 Register	P5	00h
			00h
			00h
	Port P4 Direction Register	PD4	00h
			00h
			00h
	Port P5 Direction Register	PD5	00h
			00h
			00h
	Port P6 Register	P6	XXh
			XXh
			00h
	Port P6 Direction Register	PD6	00h
			00h
			00h
	Port P8 Register	P8	XXh
			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V _{CC} /AV _{CC}	Supply voltage					1.8	—	5.5	V
V _{SS} /AV _{SS}	Supply voltage					—	0	—	V
V _{IH}	Input “H” voltage	Other than CMOS input				0.8 V _{CC}	—	V _{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.5 V _{CC}	—	V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0.55 V _{CC}	—	V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0.65 V _{CC}	—	V _{CC}	V
				Input level selection: 0.5 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.65 V _{CC}	—	V _{CC}	V
				2.7 V ≤ V _{CC} < 4.0 V	0.7 V _{CC}	—	V _{CC}	V	
				1.8 V ≤ V _{CC} < 2.7 V	0.8 V _{CC}	—	V _{CC}	V	
				Input level selection: 0.7 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.85 V _{CC}	—	V _{CC}	V
				2.7 V ≤ V _{CC} < 4.0 V	0.85 V _{CC}	—	V _{CC}	V	
				1.8 V ≤ V _{CC} < 2.7 V	0.85 V _{CC}	—	V _{CC}	V	
		External clock input (XOUT)				1.2	—	V _{CC}	V
	V _{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 V _{CC}
CMOS input			Input level switching function (I/O port)	Input level selection: 0.35 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.2 V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0	—	0.2 V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0	—	0.2 V _{CC}	V
				Input level selection: 0.5 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.4 V _{CC}	V
				2.7 V ≤ V _{CC} < 4.0 V	0	—	0.3 V _{CC}	V	
				1.8 V ≤ V _{CC} < 2.7 V	0	—	0.2 V _{CC}	V	
				Input level selection: 0.7 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.55 V _{CC}	V
				2.7 V ≤ V _{CC} < 4.0 V	0	—	0.45 V _{CC}	V	
				1.8 V ≤ V _{CC} < 2.7 V	0	—	0.35 V _{CC}	V	
		External clock input (XOUT)				0	—	0.4	V
I _{OH} (sum)		Peak sum output “H” current	Sum of all pins I _{OH} (peak)		—	—	−160	mA	
I _{OH} (sum)	Average sum output “H” current	Sum of all pins I _{OH} (avg)		—	—	−80	mA		
I _{OH} (peak)	Peak output “H” current	Drive capacity Low		—	—	−10	mA		
		Drive capacity High		—	—	−40	mA		
I _{OH} (avg)	Average output “H” current	Drive capacity Low		—	—	−5	mA		
		Drive capacity High		—	—	−20	mA		
I _{OL} (sum)	Peak sum output “L” current	Sum of all pins I _{OL} (peak)		—	—	160	mA		
I _{OL} (sum)	Average sum output “L” current	Sum of all pins I _{OL} (avg)		—	—	80	mA		
I _{OL} (peak)	Peak output “L” current	Drive capacity Low		—	—	10	mA		
		Drive capacity High		—	—	40	mA		
I _{OL} (avg)	Average output “L” current	Drive capacity Low		—	—	5	mA		
		Drive capacity High		—	—	20	mA		
f _(XIN)	XIN clock input oscillation frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
f _(XCIN)	XCIN clock input oscillation frequency			1.8 V ≤ V _{CC} ≤ 5.5 V	—	32.768	50	kHz	
f _{OCO40M}	When used as the count source for timer RC, timer RD or timer RG ⁽³⁾			2.7 V ≤ V _{CC} ≤ 5.5 V	32	—	40	MHz	
f _{OCO-F}	f _{OCO-F} frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
—	System clock frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
f _(BCLK)	CPU clock frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	

Notes:

- V_{CC} = 1.8 to 5.5 V and T_{opr} = −20 to 85 °C (N version)/−40 to 85 °C (D version), unless otherwise specified.
- The average output current indicates the average value of current measured during 100 ms.
- f_{OCO40M} can be used as the count source for timer RC, timer RD or timer RG in the range of V_{CC} = 2.7 to 5.5 V.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVCC		—	—	10	Bit
—	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±3	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	20	MHz
			3.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	16	MHz
			2.7 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	10	MHz
			2.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5.0 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				2.2	—	AVCC	V
VIA	Analog input voltage (3)				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_{opr} = -20$ to $85\text{ }^{\circ}\text{C}$ (N version)/ -40 to $85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.6 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.10 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time (2)	At the falling of Vcc from 5.0 V to (Vdet2_0 – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts (3)		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
trth	External power Vcc rise gradient	(1)	0	—	50,000	mV/msec

Notes:

1. The measurement condition is T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

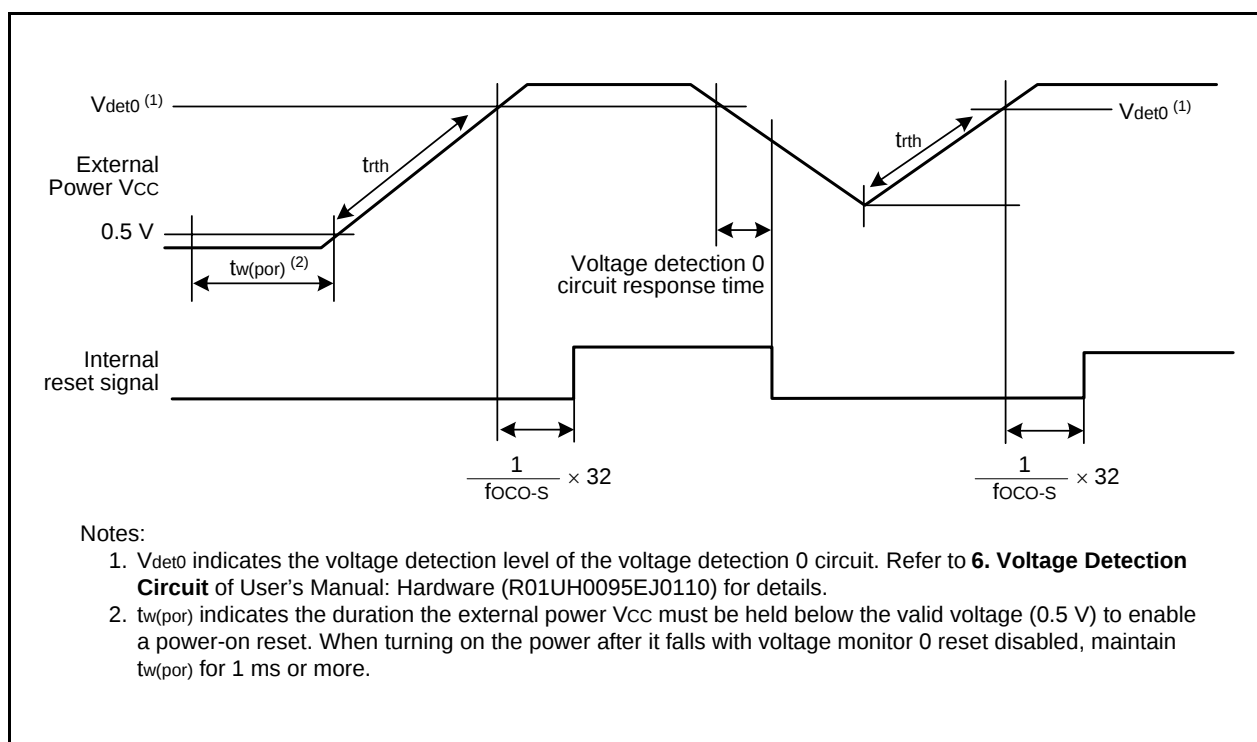
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

Table 5.16 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{cyC} + 600 ⁽²⁾	—	—	ns
t _{SCLH}	SCL input "H" width		3t _{cyC} + 300 ⁽²⁾	—	—	ns
t _{SCLL}	SCL input "L" width		5t _{cyC} + 500 ⁽²⁾	—	—	ns
t _{sf}	SCL, SDA input fall time		—	—	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		—	—	1t _{cyC} ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5t _{cyC} ⁽²⁾	—	—	ns
t _{STAH}	Start condition input hold time		3t _{cyC} ⁽²⁾	—	—	ns
t _{STAS}	Retransmit start condition input setup time		3t _{cyC} ⁽²⁾	—	—	ns
t _{STOP}	Stop condition input setup time		3t _{cyC} ⁽²⁾	—	—	ns
t _{SDAS}	Data input setup time		1t _{cyC} + 40 ⁽²⁾	—	—	ns
t _{SDAH}	Data input hold time		10	—	—	ns

Notes:

1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.
2. 1t_{cyC} = 1/f₁(s)

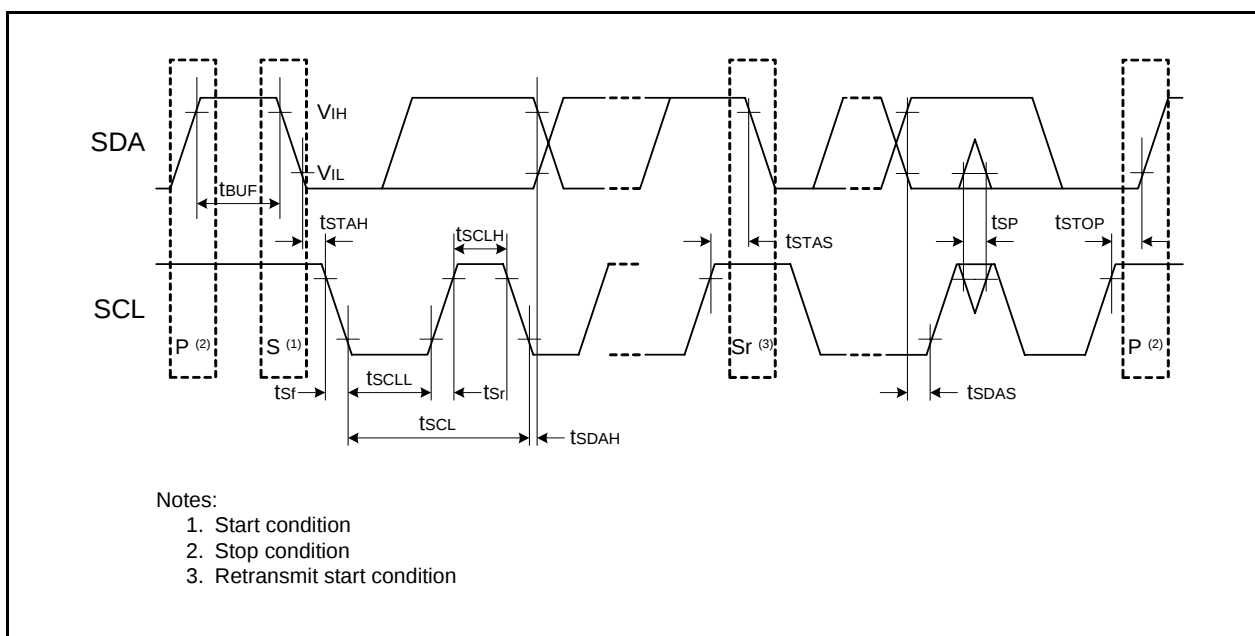
**Figure 5.7 I/O Timing of I²C bus Interface**

Table 5.17 Electrical Characteristics (1) [4.2 V ≤ V_{CC} ≤ 5.5 V]

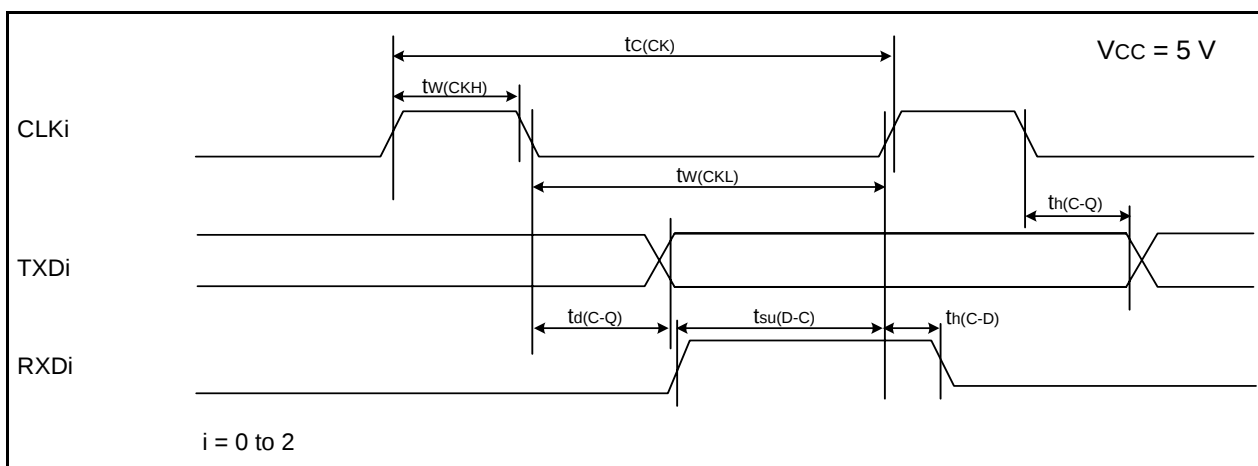
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High V _{CC} = 5 V	I _{OH} = −20 mA	V _{CC} − 2.0	—	V _{CC}	V
			Drive capacity Low V _{CC} = 5 V	I _{OH} = −5 mA	V _{CC} − 2.0	—	V _{CC}	V
		XOUT	V _{CC} = 5 V	I _{OH} = −200 μA	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High V _{CC} = 5 V	I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity Low V _{CC} = 5 V	I _{OL} = 5 mA	—	—	2.0	V
		XOUT	V _{CC} = 5 V	I _{OL} = 200 μA	—	—	0.5	V
V _{T+} –V _{T–}	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRIG, TRCCLK, TRFI, TRGIOA, TRGIOB, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5.0 V		—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5.0 V		—	—	−5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5.0 V		25	50	100	kΩ
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. 4.2 V ≤ V_{CC} ≤ 5.5 V, T_{opr} = −20 to 85 °C (N version)/−40 to 85 °C (D version), and f(XIN) = 20 MHz, unless otherwise specified.

Table 5.22 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.11 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.23 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 4$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	250 ⁽²⁾	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

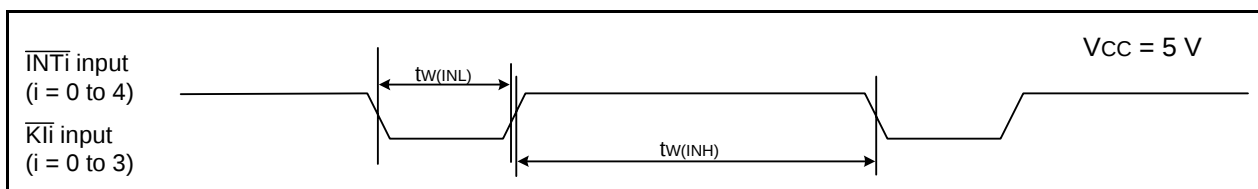
**Figure 5.12 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 5 V**

Table 5.24 Electrical Characteristics (3) [$2.7\text{ V} \leq V_{CC} < 4.2\text{ V}$]

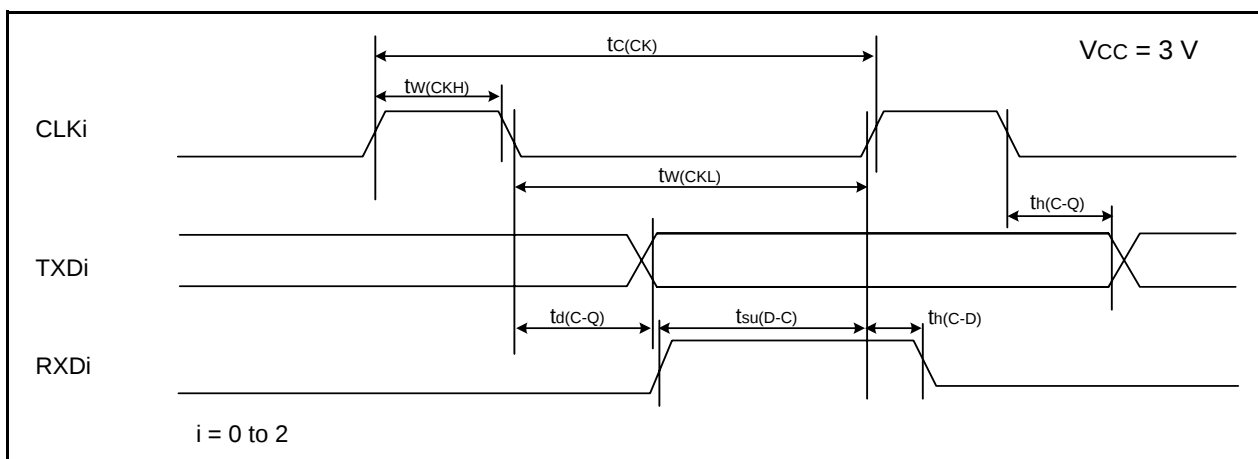
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, TRGIOA, TRGIOB, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	V _{CC} = 3.0 V		0.1	0.4	—	V
		RESET	V _{CC} = 3.0 V		0.1	0.5	—	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3.0 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3.0 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3.0 V		42	84	168	k Ω
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. $2.7\text{ V} \leq V_{CC} < 4.2\text{ V}$, T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), and f(XIN) = 10 MHz, unless otherwise specified.

Table 5.29 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.16 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.30 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 4$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	380 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	380 (2)	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

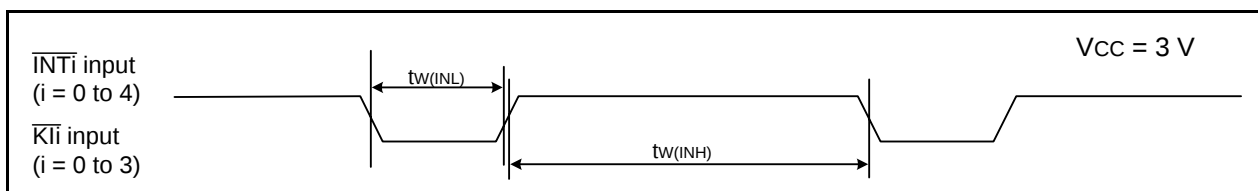
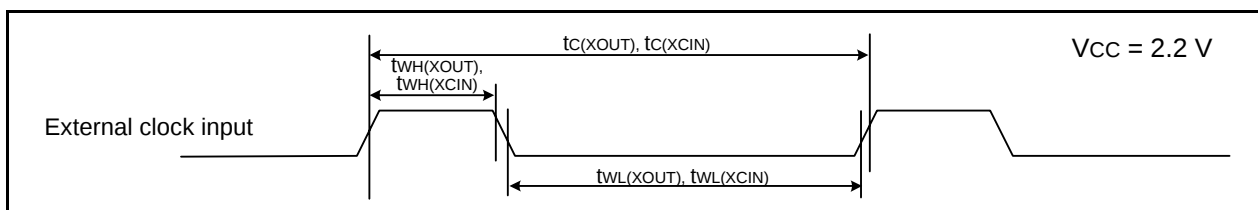
**Figure 5.17 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 3 V**

Table 5.32 Electrical Characteristics (6) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

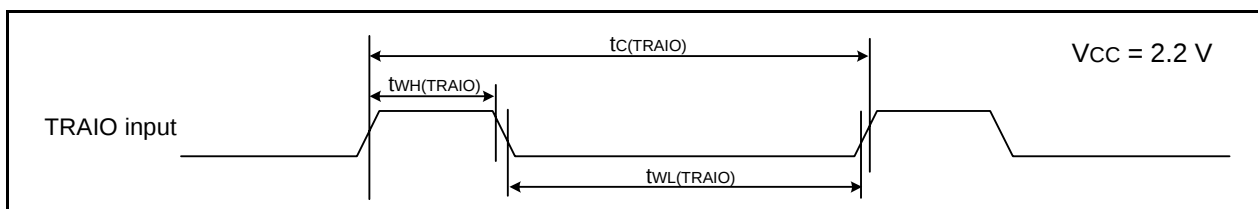
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current ($V_{CC} = 1.8\text{ to }2.7\text{ V}$) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	—	2.2	—	mA
				0.8	—	mA
		High-speed on-chip oscillator mode	—	2.5	10	mA
				1.7	—	mA
				1	—	mA
		Low-speed on-chip oscillator mode	—	90	300	μA
		Low-speed clock mode	—	80	350	μA
				40	—	μA
				15	90	μA
		Wait mode	—	4	80	μA
				3.5	—	μA
				2.0	5	μA
		Stop mode	—	15	—	μA

Timing requirements (Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$, $T_{opr} = 25\text{ }^{\circ}\text{C}$)**Table 5.33 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(XOUT)$	XOUT input cycle time	200	—	ns
$t_{WH}(XOUT)$	XOUT input "H" width	90	—	ns
$t_{WL}(XOUT)$	XOUT input "L" width	90	—	ns
$t_c(XCIN)$	XCIN input cycle time	14	—	μs
$t_{WH}(XCIN)$	XCIN input "H" width	7	—	μs
$t_{WL}(XCIN)$	XCIN input "L" width	7	—	μs

**Figure 5.18 External Clock Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.34 TRAIO Input**

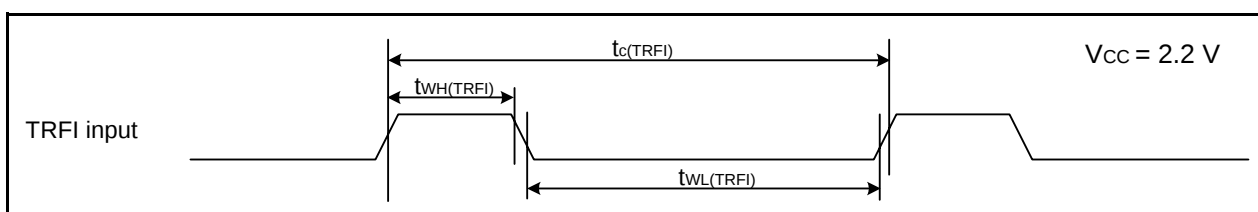
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TRAIO)$	TRAIO input cycle time	500	—	ns
$t_{WH}(TRAIO)$	TRAIO input "H" width	200	—	ns
$t_{WL}(TRAIO)$	TRAIO input "L" width	200	—	ns

**Figure 5.19 TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.35 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(TRFI)$	TRFI input cycle time	2000 (1)	—	ns
$t_{WH}(TRFI)$	TRFI input "H" width	1000 (2)	—	ns
$t_{WL}(TRFI)$	TRFI input "L" width	1000 (2)	—	ns

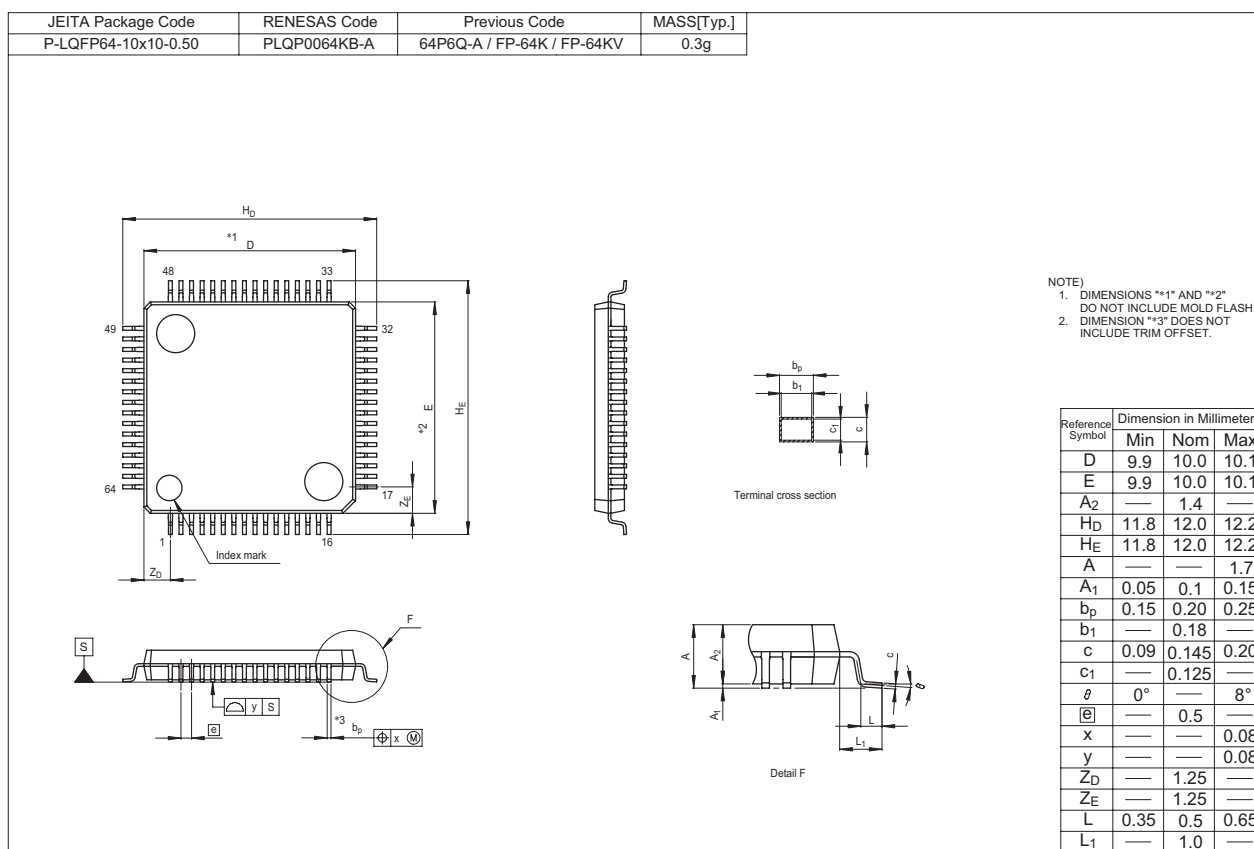
Notes:

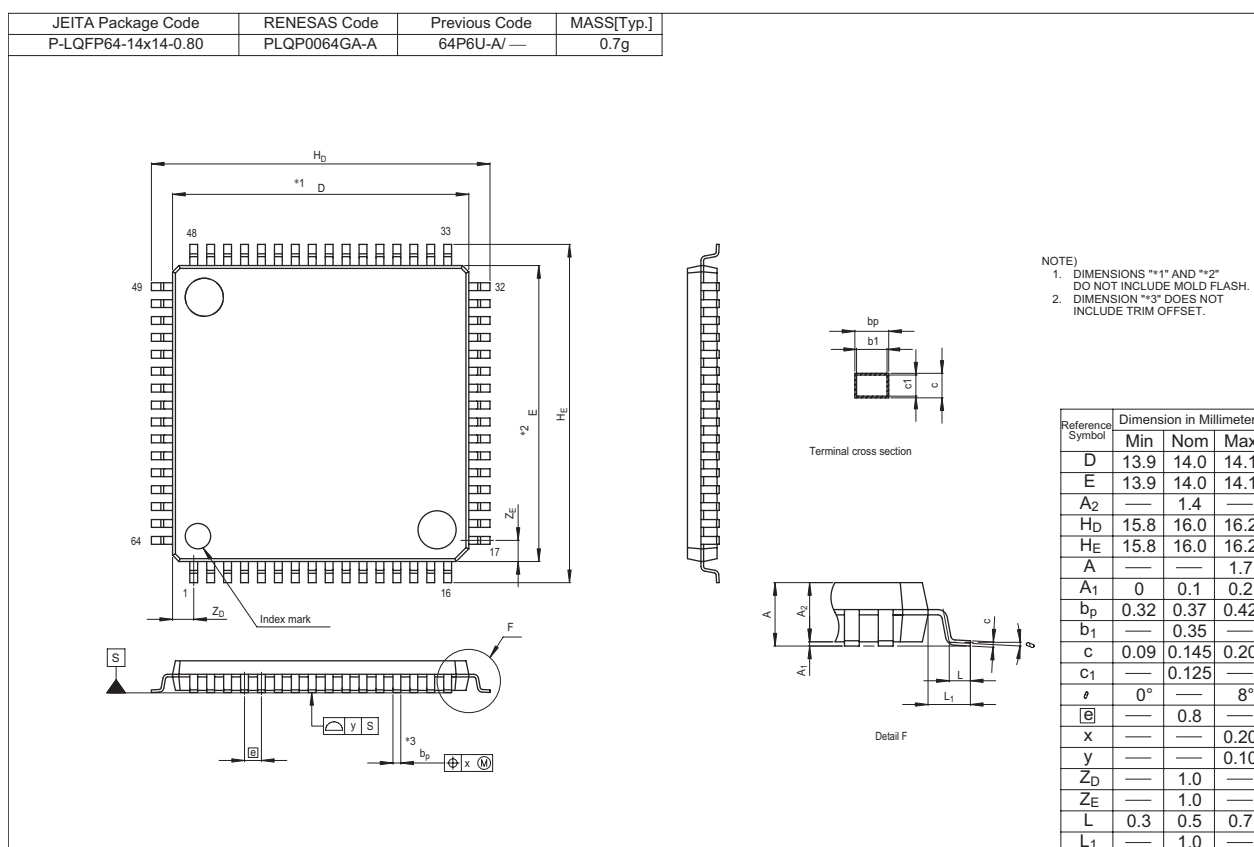
1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

**Figure 5.20 TRFI Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.





REVISION HISTORY	R8C/36C Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Oct 30, 2009	—	First Edition issued
1.00	Nov 02, 2010	All pages 4 28 to 54	“Preliminary”, “Under development” deleted Table 1.3 revised “5. Electrical Characteristics” added
1.10	Nov 02, 2010	— 3 4 and 5 6 8 17 33 47 51 55 59	TN-R8C-A015A/E reflected Table 1.2 “Timer RG” and “Package” revised Tables 1.3 and 1.4 revised Figure 1.1 revised Figure 1.3 “PTQP0064LB-A” added Figure 3.1 “Part Number” revised Table 5.3 “tCONV”, “tSAMP” revised Table 5.21 revised Table 5.28 revised Table 5.35 revised Package (PTQP0064LB-A) added

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