# Renesas Electronics America Inc - R5F21368CNFA#W4 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 59 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 12x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21368cnfa-w4 |

### 1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/36C Group.

**Table 1.1 Specifications for R8C/36C Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C CPU core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)<br>200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, Data flash | Refer to **Table 1.3 Product List for R8C/36C Group** |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | • Input-only: 1 pin<br>• CMOS I/O ports: 59, selectable pull-up resistor<br>• High current drive ports: 59 |
| Clock | Clock generation circuits | • 4 circuits: XIN clock oscillation circuit,<br>XCIN clock oscillation circuit (32 kHz),<br>High-speed on-chip oscillator (with frequency adjustment function),<br>Low-speed on-chip oscillator<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| | | Real-time clock (timer RE) |
| Interrupts | | • Interrupt Vectors: 69<br>• External: 9 sources ($\overline{\text{INT}}$ × 5, key input × 4)<br>• Priority levels: 7 levels |
| Watchdog Timer | | • 14 bits × 1 (with prescaler)<br>• Reset start selectable<br>• Low-speed on-chip oscillator for watchdog timer selectable |
| DTC (Data Transfer Controller) | | • 1 channel<br>• Activation sources: 39<br>• Transfer modes: 2 (normal mode, repeat mode) |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits × 2 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |

## 1.2 Product List

Tables 1.3 and 1.4 list Product List for R8C/36C Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/36C Group.

**Table 1.3 Product List for R8C/36C Group (1) Current of Nov 2010**

| Part No. | ROM Capacity | | RAM Capacity | Package Type | Remarks | |
|---|---|---|---|---|---|---|
| | Program ROM | Data flash | | | | |
| R5F21364CNFP | 16 Kbytes | 1 Kbyte × 4 | 1.5 Kbytes | PLQP0064KB-A | N version | |
| R5F21365CNFP | 24 Kbytes | 1 Kbyte × 4 | 2 Kbytes | PLQP0064KB-A | | |
| R5F21366CNFP | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0064KB-A | | |
| R5F21367CNFP | 48 Kbytes | 1 Kbyte × 4 | 4 Kbytes | PLQP0064KB-A | | |
| R5F21368CNFP | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0064KB-A | | |
| R5F2136ACNFP | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0064KB-A | | |
| R5F2136CCNFP | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0064KB-A | | |
| R5F21364CNFA | 16 Kbytes | 1 Kbyte × 4 | 1.5 Kbytes | PLQP0064GA-A | | |
| R5F21365CNFA | 24 Kbytes | 1 Kbyte × 4 | 2 Kbytes | PLQP0064GA-A | | |
| R5F21366CNFA | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0064GA-A | | |
| R5F21367CNFA | 48 Kbytes | 1 Kbyte × 4 | 4 Kbytes | PLQP0064GA-A | | |
| R5F21368CNFA | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0064GA-A | | |
| R5F2136ACNFA | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0064GA-A | | |
| R5F2136CCNFA | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0064GA-A | | |
| R5F21364CNFB (D) | 16 Kbytes | 1 Kbyte × 4 | 1.5 Kbytes | PTQP0064LB-A | | |
| R5F21365CNFB (D) | 24 Kbytes | 1 Kbyte × 4 | 2 Kbytes | PTQP0064LB-A | | |
| R5F21366CNFB (D) | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PTQP0064LB-A | | |
| R5F21367CNFB (D) | 48 Kbytes | 1 Kbyte × 4 | 4 Kbytes | PTQP0064LB-A | | |
| R5F21368CNFB (D) | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PTQP0064LB-A | | |
| R5F2136ACNFB (D) | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PTQP0064LB-A | | |
| R5F2136CCNFB (D) | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PTQP0064LB-A | | |
| R5F21364CNXXXFP | 16 Kbytes | 1 Kbyte × 4 | 1.5 Kbytes | PLQP0064KB-A | N version | Factory programming product (1) |
| R5F21365CNXXXFP | 24 Kbytes | 1 Kbyte × 4 | 2 Kbytes | PLQP0064KB-A | | |
| R5F21366CNXXXFP | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0064KB-A | | |
| R5F21367CNXXXFP | 48 Kbytes | 1 Kbyte × 4 | 4 Kbytes | PLQP0064KB-A | | |
| R5F21368CNXXXFP | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0064KB-A | | |
| R5F2136ACNXXXFP | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0064KB-A | | |
| R5F2136CCNXXXFP | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0064KB-A | | |
| R5F21364CNXXXFA | 16 Kbytes | 1 Kbyte × 4 | 1.5 Kbytes | PLQP0064GA-A | | |
| R5F21365CNXXXFA | 24 Kbytes | 1 Kbyte × 4 | 2 Kbytes | PLQP0064GA-A | | |
| R5F21366CNXXXFA | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0064GA-A | | |
| R5F21367CNXXXFA | 48 Kbytes | 1 Kbyte × 4 | 4 Kbytes | PLQP0064GA-A | | |
| R5F21368CNXXXFA | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0064GA-A | | |
| R5F2136ACNXXXFA | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0064GA-A | | |
| R5F2136CCNXXXFA | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0064GA-A | | |
| R5F21364CNXXXFB (D) | 16 Kbytes | 1 Kbyte × 4 | 1.5 Kbytes | PTQP0064LB-A | | |
| R5F21365CNXXXFB (D) | 24 Kbytes | 1 Kbyte × 4 | 2 Kbytes | PTQP0064LB-A | | |
| R5F21366CNXXXFB (D) | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PTQP0064LB-A | | |
| R5F21367CNXXXFB (D) | 48 Kbytes | 1 Kbyte × 4 | 4 Kbytes | PTQP0064LB-A | | |
| R5F21368CNXXXFB (D) | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PTQP0064LB-A | | |
| R5F2136ACNXXXFB (D) | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PTQP0064LB-A | | |
| R5F2136CCNXXXFB (D) | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PTQP0064LB-A | | |

(D): Under development

Note:

1. The user ROM is programmed before shipment.

## 1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

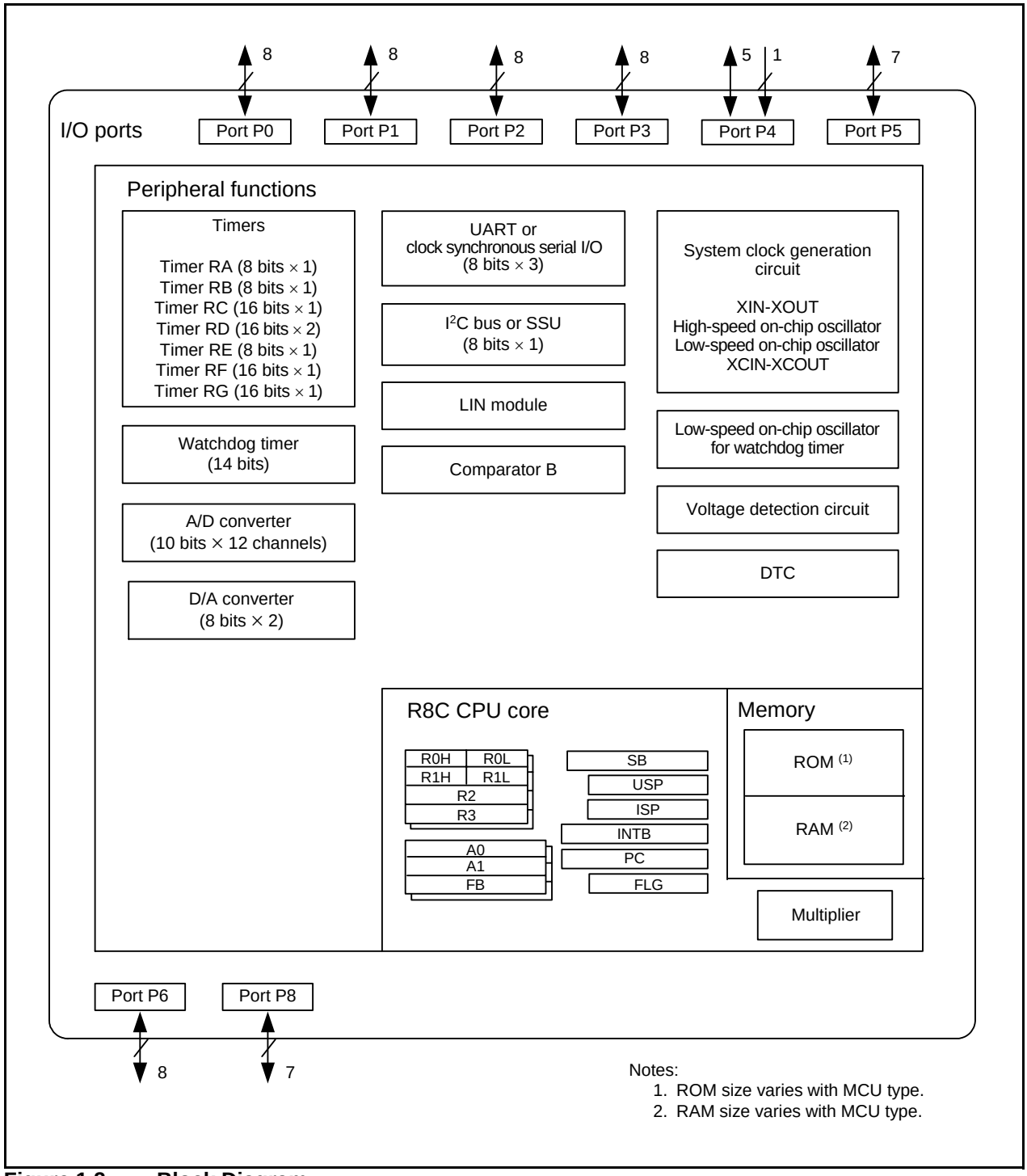



**Figure 1.2 Block Diagram**

**Table 1.6 Pin Name Information by Pin Number (2)**

| Pin Number | Control Pin | Port | I/O Pin Functions for Peripheral Modules | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Interrupt | Timer | Serial Interface | SSU | $I^2C$ bus | A/D Converter, D/A Converter, Comparator B |
| 40 | | P4_5 | INT0 | | (RXD2/SCL2) | | | ADTRG |
| 41 | | P1_7 | $\overline{\text{INT1}}$ | (TRAIO) | | | | IVCMP1 |
| 42 | | P1_6 | | | (CLK0) | | | IVREF1 |
| 43 | | P1_5 | ($\overline{\text{INT1}}$) | (TRAIO) | (RXD0) | | | |
| 44 | | P1_4 | | (TRCCLK) | (TXD0) | | | |
| 45 | | P1_3 | $\overline{\text{KI3}}$ | TRBO (/TRCIOC) | | | | AN11 |
| 46 | | P1_2 | $\overline{\text{KI2}}$ | (TRCIOB) | | | | AN10 |
| 47 | | P1_1 | $\overline{\text{KI1}}$ | (TRCIOA/TRCTRG) | | | | AN9 |
| 48 | | P1_0 | $\overline{\text{KI0}}$ | (TRCIOD) | | | | AN8 |
| 49 | | P0_7 | | (TRCIOC) | | | | AN0/DA1 |
| 50 | | P0_6 | | (TRCIOD) | | | | AN1/DA0 |
| 51 | | P0_5 | | (TRCIOB) | | | | AN2 |
| 52 | | P0_4 | | TREO(/TRCIOB) | | | | AN3 |
| 53 | | P0_3 | | (TRCIOB) | (CLK1) | | | AN4 |
| 54 | | P0_2 | | (TRCIOA/TRCTRG) | (RXD1) | | | AN5 |
| 55 | | P0_1 | | (TRCIOA/TRCTRG) | (TXD1) | | | AN6 |
| 56 | | P0_0 | | (TRCIOA/TRCTRG) | | | | AN7 |
| 57 | | P6_4 | | | (RXD1) | | | |
| 58 | | P6_3 | | | (TXD1) | | | |
| 59 | | P6_2 | | | (CLK1) | | | |
| 60 | | P6_1 | | | | | | |
| 61 | | P6_0 | | (TREO) | | | | |
| 62 | | P5_7 | | (TRGIOB) | | | | |
| 63 | | P5_6 | | (TRAO/TRGIOA) | | | | |
| 64 | | P3_2 | ($\overline{\text{INT1}}$/ $\overline{\text{INT2}}$) | (TRAIO/TRGCLKB) | | | | |

Note:
1. Can be assigned to the pin in parentheses by a program.

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

**Table 4.3 SFR Information (3) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0080h | DTC Activation Control Register | DTCTL | 00h |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | | | |
| 0085h | | | |
| 0086h | | | |
| 0087h | | | |
| 0088h | DTC Activation Enable Register 0 | DTCEN0 | 00h |
| 0089h | DTC Activation Enable Register 1 | DTCEN1 | 00h |
| 008Ah | DTC Activation Enable Register 2 | DTCEN2 | 00h |
| 008Bh | DTC Activation Enable Register 3 | DTCEN3 | 00h |
| 008Ch | DTC Activation Enable Register 4 | DTCEN4 | 00h |
| 008Dh | DTC Activation Enable Register 5 | DTCEN5 | 00h |
| 008Eh | DTC Activation Enable Register 6 | DTCEN6 | 00h |
| 008Fh | | | |
| 0090h | Timer RF Register | TRF | 00h |
| 0091h | | | 00h |
| 0092h | | | |
| 0093h | | | |
| 0094h | | | |
| 0095h | | | |
| 0096h | | | |
| 0097h | | | |
| 0098h | | | |
| 0099h | | | |
| 009Ah | Timer RF Control Register 0 | TRFCR0 | 00h |
| 009Bh | Timer RF Control Register 1 | TRFCR1 | 00h |
| 009Ch | Capture and Compare 0 Register | TRFM0 | 00h |
| 009Dh | | | 00h |
| 009Eh | Compare 1 Register | TRFM1 | FFh |
| 009Fh | | | FFh |
| 00A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 00A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 00A3h | | | XXh |
| 00A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 00A7h | | | XXh |
| 00A8h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 00A9h | UART2 Bit Rate Register | U2BRG | XXh |
| 00AAh | UART2 Transmit Buffer Register | U2TB | XXh |
| 00ABh | | | XXh |
| 00ACh | UART2 Transmit/Receive Control Register 0 | U2C0 | 00001000b |
| 00ADh | UART2 Transmit/Receive Control Register 1 | U2C1 | 00000010b |
| 00AEh | UART2 Receive Buffer Register | U2RB | XXh |
| 00AFh | | | XXh |
| 00B0h | UART2 Digital Filter Function Select Register | URXDF | 00h |
| 00B1h | | | |
| 00B2h | | | |
| 00B3h | | | |
| 00B4h | | | |
| 00B5h | | | |
| 00B6h | | | |
| 00B7h | | | |
| 00B8h | | | |
| 00B9h | | | |
| 00BAh | | | |
| 00BBh | UART2 Special Mode Register 5 | U2SMR5 | 00h |
| 00BCh | UART2 Special Mode Register 4 | U2SMR4 | 00h |
| 00BDh | UART2 Special Mode Register 3 | U2SMR3 | 000X0X0Xb |
| 00BEh | UART2 Special Mode Register 2 | U2SMR2 | X0000000b |
| 00BFh | UART2 Special Mode Register | U2SMR | X0000000b |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

# 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

| Symbol | Parameter | Condition | Rated Value | Unit |
|---|---|---|---|---|
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | −0.3 to 6.5 | V |
| $V_I$ | Input voltage | | −0.3 to $V_{CC}$ + 0.3 | V |
| $V_O$ | Output voltage | | −0.3 to $V_{CC}$ + 0.3 | V |
| $P_d$ | Power dissipation | −40°C ≤ $T_{opr}$ ≤ 85°C | 500 | mW |
| $T_{opr}$ | Operating ambient temperature | | −20 to 85 (N version)/<br>−40 to 85 (D version) | °C |
| $T_{stg}$ | Storage temperature | | −65 to 150 | °C |

**Table 5.2 Recommended Operating Conditions (1)**

| Symbol | Parameter | | | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Typ. | Max. | |
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | | | | 1.8 | — | 5.5 | V |
| $V_{SS}$/$AV_{SS}$ | Supply voltage | | | | | — | 0 | — | V |
| $V_{IH}$ | Input “H” voltage | Other than CMOS input | | | | 0.8 $V_{CC}$ | — | $V_{CC}$ | V |
| | | CMOS input | Input level switching function (I/O port) | Input level selection: 0.35 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.5 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.55 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.65 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | Input level selection: 0.5 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.65 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.7 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.8 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | Input level selection: 0.7 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.85 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.85 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.85 $V_{CC}$ | — | $V_{CC}$ | V |
| | | External clock input (XOUT) | | | | 1.2 | — | $V_{CC}$ | V |
| $V_{IL}$ | Input “L” voltage | Other than CMOS input | | | | 0 | — | 0.2 $V_{CC}$ | V |
| | | CMOS input | Input level switching function (I/O port) | Input level selection: 0.35 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | — | 0.2 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | — | 0.2 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | — | 0.2 $V_{CC}$ | V |
| | | | | Input level selection: 0.5 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | — | 0.4 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | — | 0.3 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | — | 0.2 $V_{CC}$ | V |
| | | | | Input level selection: 0.7 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | — | 0.55 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | — | 0.45 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | — | 0.35 $V_{CC}$ | V |
| | | External clock input (XOUT) | | | | 0 | — | 0.4 | V |
| $I_{OH(sum)}$ | Peak sum output “H” current | | Sum of all pins $I_{OH(peak)}$ | | | — | — | –160 | mA |
| $I_{OH(sum)}$ | Average sum output “H” current | | Sum of all pins $I_{OH(avg)}$ | | | — | — | –80 | mA |
| $I_{OH(peak)}$ | Peak output “H” current | | Drive capacity Low | | | — | — | –10 | mA |
| | | | Drive capacity High | | | — | — | –40 | mA |
| $I_{OH(avg)}$ | Average output “H” current | | Drive capacity Low | | | — | — | –5 | mA |
| | | | Drive capacity High | | | — | — | –20 | mA |
| $I_{OL(sum)}$ | Peak sum output “L” current | | Sum of all pins $I_{OL(peak)}$ | | | — | — | 160 | mA |
| $I_{OL(sum)}$ | Average sum output “L” current | | Sum of all pins $I_{OL(avg)}$ | | | — | — | 80 | mA |
| $I_{OL(peak)}$ | Peak output “L” current | | Drive capacity Low | | | — | — | 10 | mA |
| | | | Drive capacity High | | | — | — | 40 | mA |
| $I_{OL(avg)}$ | Average output “L” current | | Drive capacity Low | | | — | — | 5 | mA |
| | | | Drive capacity High | | | — | — | 20 | mA |
| $f_{(XIN)}$ | XIN clock input oscillation frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | — | — | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | — | — | 5 | MHz |
| $f_{(XCIN)}$ | XCIN clock input oscillation frequency | | | | 1.8 V ≤ $V_{CC}$ ≤ 5.5 V | — | 32.768 | 50 | kHz |
| fOCO40M | When used as the count source for timer RC, timer RD or timer RG (3) | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | 32 | — | 40 | MHz |
| fOCO-F | fOCO-F frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | — | — | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | — | — | 5 | MHz |
| — | System clock frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | — | — | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | — | — | 5 | MHz |
| $f_{(BCLK)}$ | CPU clock frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | — | — | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | — | — | 5 | MHz |

Notes:
1. $V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC, timer RD or timer RG in the range of $V_{CC}$ = 2.7 to 5.5 V.

**Table 5.6 Flash Memory (Program ROM) Electrical Characteristics**

| Symbol | Parameter | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| — | Program/erase endurance (2) | | 1,000 (3) | — | — | times |
| — | Byte program time | | — | 80 | 500 | µs |
| — | Block erase time | | — | 0.3 | — | s |
| $t_{d(SR-SUS)}$ | Time delay from suspend request until suspend | | — | — | 5 + CPU clock × 3 cycles | ms |
| — | Interval from erase start/restart until following suspend request | | 0 | — | — | µs |
| — | Time from suspend until erase restart | | — | — | 30 + CPU clock × 1 cycle | µs |
| $t_{d(CMDRST-READY)}$ | Time from when command is forcibly stopped until reading is enabled | | — | — | 30 + CPU clock × 1 cycle | µs |
| — | Program, erase voltage | | 2.7 | — | 5.5 | V |
| — | Read voltage | | 1.8 | — | 5.5 | V |
| — | Program, erase temperature | | 0 | — | 60 | °C |
| — | Data hold time (7) | Ambient temperature = 55 °C | 20 | — | — | year |

Notes:
1. $V_{CC}$ = 2.7 to 5.5 V and $T_{opr}$ = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

### Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det0}$ | Voltage detection level Vdet0_0 (2) | | 1.80 | 1.90 | 2.05 | V |
| | Voltage detection level Vdet0_1 (2) | | 2.15 | 2.35 | 2.50 | V |
| | Voltage detection level Vdet0_2 (2) | | 2.70 | 2.85 | 3.05 | V |
| | Voltage detection level Vdet0_3 (2) | | 3.55 | 3.80 | 4.05 | V |
| — | Voltage detection 0 circuit response time (4) | At the falling of $V_{CC}$ from 5.0 V to (Vdet0_0 – 0.1) V | — | 6 | 150 | µs |
| — | Voltage detection circuit self power consumption | VCA25 = 1, $V_{CC}$ = 5.0 V | — | 1.5 | — | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts (3) | | — | — | 100 | µs |

Notes:
1. The measurement condition is $V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes $V_{det0}$.

### Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

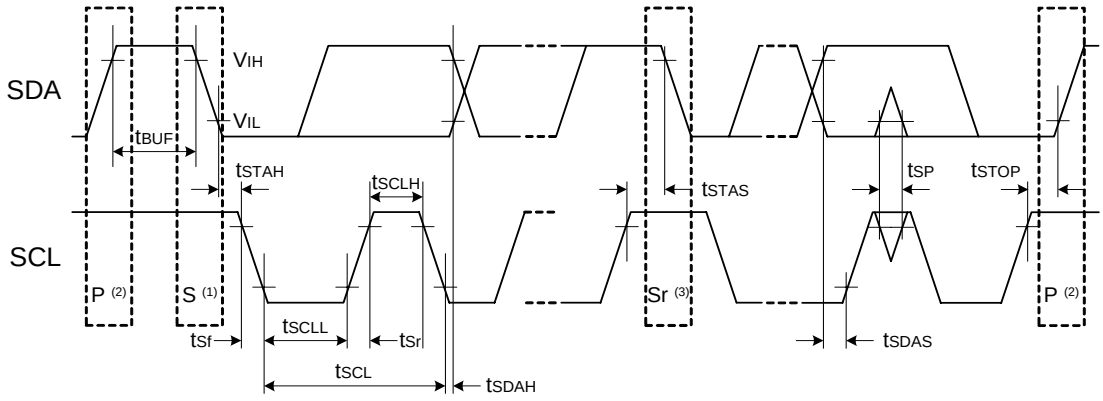
| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level Vdet1_0 (2) | At the falling of $V_{CC}$ | 2.00 | 2.20 | 2.40 | V |
| | Voltage detection level Vdet1_1 (2) | At the falling of $V_{CC}$ | 2.15 | 2.35 | 2.55 | V |
| | Voltage detection level Vdet1_2 (2) | At the falling of $V_{CC}$ | 2.30 | 2.50 | 2.70 | V |
| | Voltage detection level Vdet1_3 (2) | At the falling of $V_{CC}$ | 2.45 | 2.65 | 2.85 | V |
| | Voltage detection level Vdet1_4 (2) | At the falling of $V_{CC}$ | 2.60 | 2.80 | 3.00 | V |
| | Voltage detection level Vdet1_5 (2) | At the falling of $V_{CC}$ | 2.75 | 2.95 | 3.15 | V |
| | Voltage detection level Vdet1_6 (2) | At the falling of $V_{CC}$ | 2.85 | 3.10 | 3.40 | V |
| | Voltage detection level Vdet1_7 (2) | At the falling of $V_{CC}$ | 3.00 | 3.25 | 3.55 | V |
| | Voltage detection level Vdet1_8 (2) | At the falling of $V_{CC}$ | 3.15 | 3.40 | 3.70 | V |
| | Voltage detection level Vdet1_9 (2) | At the falling of $V_{CC}$ | 3.30 | 3.55 | 3.85 | V |
| | Voltage detection level Vdet1_A (2) | At the falling of $V_{CC}$ | 3.45 | 3.70 | 4.00 | V |
| | Voltage detection level Vdet1_B (2) | At the falling of $V_{CC}$ | 3.60 | 3.85 | 4.15 | V |
| | Voltage detection level Vdet1_C (2) | At the falling of $V_{CC}$ | 3.75 | 4.00 | 4.30 | V |
| | Voltage detection level Vdet1_D (2) | At the falling of $V_{CC}$ | 3.90 | 4.15 | 4.45 | V |
| | Voltage detection level Vdet1_E (2) | At the falling of $V_{CC}$ | 4.05 | 4.30 | 4.60 | V |
| | Voltage detection level Vdet1_F (2) | At the falling of $V_{CC}$ | 4.20 | 4.45 | 4.75 | V |
| — | Hysteresis width at the rising of $V_{CC}$ in voltage detection 1 circuit | Vdet1_0 to Vdet1_5 selected | — | 0.07 | — | V |
| | | Vdet1_6 to Vdet1_F selected | — | 0.10 | — | V |
| — | Voltage detection 1 circuit response time (3) | At the falling of $V_{CC}$ from 5.0 V to (Vdet1_0 – 0.1) V | — | 60 | 150 | µs |
| — | Voltage detection circuit self power consumption | VCA26 = 1, $V_{CC}$ = 5.0 V | — | 1.7 | — | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts (4) | | — | — | 100 | µs |

Notes:
1. The measurement condition is $V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes $V_{det1}$.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 5.16 Timing Requirements of I²C bus Interface**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{SCL}$ | SCL input cycle time | | $12t_{CYC} + 600$ (2) | — | — | ns |
| $t_{SCLH}$ | SCL input “H” width | | $3t_{CYC} + 300$ (2) | — | — | ns |
| $t_{SCLL}$ | SCL input “L” width | | $5t_{CYC} + 500$ (2) | — | — | ns |
| $t_{sf}$ | SCL, SDA input fall time | | — | — | 300 | ns |
| $t_{SP}$ | SCL, SDA input spike pulse rejection time | | — | — | $1t_{CYC}$ (2) | ns |
| $t_{BUF}$ | SDA input bus-free time | | $5t_{CYC}$ (2) | — | — | ns |
| $t_{STAH}$ | Start condition input hold time | | $3t_{CYC}$ (2) | — | — | ns |
| $t_{STAS}$ | Retransmit start condition input setup time | | $3t_{CYC}$ (2) | — | — | ns |
| $t_{STOP}$ | Stop condition input setup time | | $3t_{CYC}$ (2) | — | — | ns |
| $t_{SDAS}$ | Data input setup time | | $1t_{CYC} + 40$ (2) | — | — | ns |
| $t_{SDAH}$ | Data input hold time | | 10 | — | — | ns |

Notes:
1. $V_{CC}$ = 1.8 to 5.5 V, $V_{SS}$ = 0 V, and $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$




Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

**Figure 5.7 I/O Timing of I²C bus Interface**

**Table 5.24 Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Other than XOUT | Drive capacity High | $I_{OH}$ = –5 mA | $V_{CC}$ – 0.5 | — | $V_{CC}$ | V |
| | | | Drive capacity Low | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | — | $V_{CC}$ | V |
| | | XOUT | | $I_{OH}$ = –200 μA | 1.0 | — | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Other than XOUT | Drive capacity High | $I_{OL}$ = 5 mA | — | — | 0.5 | V |
| | | | Drive capacity Low | $I_{OL}$ = 1 mA | — | — | 0.5 | V |
| | | XOUT | | $I_{OL}$ = 200 μA | — | — | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, TRGIOA, TRGIOB, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO | $V_{CC}$ = 3.0 V | | 0.1 | 0.4 | — | V |
| | | $\overline{RESET}$ | $V_{CC}$ = 3.0 V | | 0.1 | 0.5 | — | V |
| $I_{IH}$ | Input “H” current | | $V_I$ = 3 V, $V_{CC}$ = 3.0 V | | — | — | 4.0 | μA |
| $I_{IL}$ | Input “L” current | | $V_I$ = 0 V, $V_{CC}$ = 3.0 V | | — | — | –4.0 | μA |
| $R_{PULLUP}$ | Pull-up resistance | | $V_I$ = 0 V, $V_{CC}$ = 3.0 V | | 42 | 84 | 168 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | — | 0.3 | — | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | — | 8 | — | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | — | — | V |

Note:
1. 2.7 V ≤ $V_{CC}$ < 4.2 V, $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version), and f(XIN) = 10 MHz, unless otherwise specified.

**Table 5.25 Electrical Characteristics (4) [2.7 V ≤ Vcc ≤ 3.3 V]**
**(Topr = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.)**

| Symbol | Parameter | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Icc | Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss | High-speed clock mode | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | — | 3.5 | 10 | mA |
| | | | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | — | 1.5 | 7.5 | mA |
| | | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | — | 7.0 | 15 | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | — | 3.0 | — | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division | — | 4.0 | — | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8 | — | 1.5 | — | mA |
| | | | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 4 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-16, MSTIIC = MSTTRD = MSTTRC = 1 | — | 1 | — | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0 | — | 90 | 390 | µA |
| | | Low-speed clock mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>FMR27 = 1, VCA20 = 0 | — | 80 | 400 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>Program operation on RAM<br>Flash memory off, FMSTP = 1, VCA20 = 0 | — | 40 | — | µA |
| | | Wait mode | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | — | 15 | 90 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | — | 4 | 80 | µA |
| | | | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (peripheral clock off)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | — | 3.5 | — | µA |
| | | Stop mode | XIN clock off, Topr = 25 °C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | — | 2.0 | 5.0 | µA |
| | | | XIN clock off, Topr = 85 °C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0 | — | 15 | — | µA |

**Timing requirements (Unless Otherwise Specified: $V_{CC}$ = 3 V, $V_{SS}$ = 0 V, $T_{opr}$ = 25 °C)**

**Table 5.26 External Clock Input (XOUT, XCIN)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XOUT)}$ | XOUT input cycle time | 50 | — | ns |
| $t_{WH(XOUT)}$ | XOUT input “H” width | 24 | — | ns |
| $t_{WL(XOUT)}$ | XOUT input “L” width | 24 | — | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | — | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | — | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | — | µs |

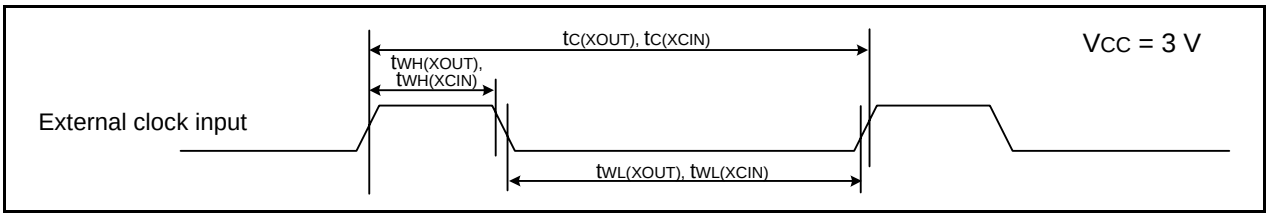



**Figure 5.13 External Clock Input Timing Diagram when VCC = 3 V**

**Table 5.27 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 300 | — | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 120 | — | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 120 | — | ns |

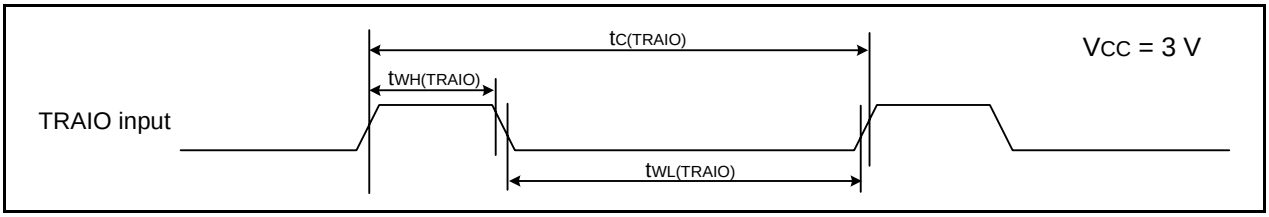



**Figure 5.14 TRAIO Input Timing Diagram when Vcc = 3 V**

**Table 5.28 TRFI Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRFI)}$ | TRFI input cycle time | 1200 (1) | — | ns |
| $t_{WH(TRFI)}$ | TRFI input “H” width | 600 (2) | — | ns |
| $t_{WL(TRFI)}$ | TRFI input “L” width | 600 (2) | — | ns |

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

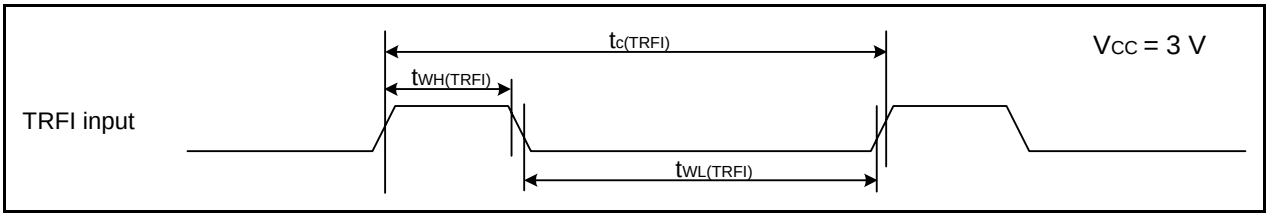



**Figure 5.15 TRFI Input Timing Diagram when Vcc = 3 V**

**Timing requirements (Unless Otherwise Specified: $V_{CC}$ = 2.2 V, $V_{SS}$ = 0 V, $T_{opr}$ = 25 °C)**

**Table 5.33 External Clock Input (XOUT, XCIN)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XOUT)}$ | XOUT input cycle time | 200 | — | ns |
| $t_{WH(XOUT)}$ | XOUT input “H” width | 90 | — | ns |
| $t_{WL(XOUT)}$ | XOUT input “L” width | 90 | — | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | — | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | — | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | — | µs |

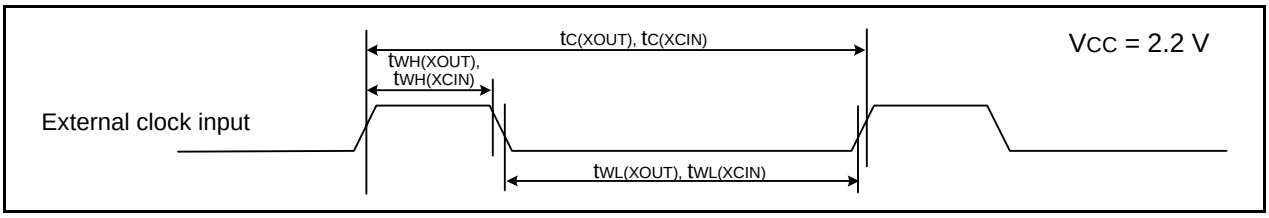



**Figure 5.18 External Clock Input Timing Diagram when VCC = 2.2 V**

**Table 5.34 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 500 | — | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 200 | — | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 200 | — | ns |

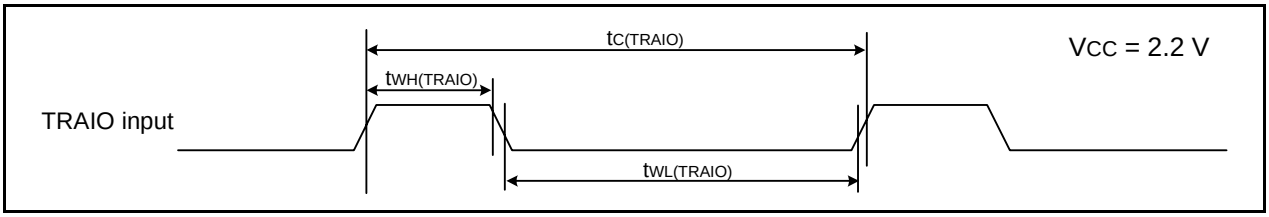



**Figure 5.19 TRAIO Input Timing Diagram when Vcc = 2.2 V**

**Table 5.35 TRFI Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRFI)}$ | TRFI input cycle time | 2000 (1) | — | ns |
| $t_{WH(TRFI)}$ | TRFI input “H” width | 1000 (2) | — | ns |
| $t_{WL(TRFI)}$ | TRFI input “L” width | 1000 (2) | — | ns |

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

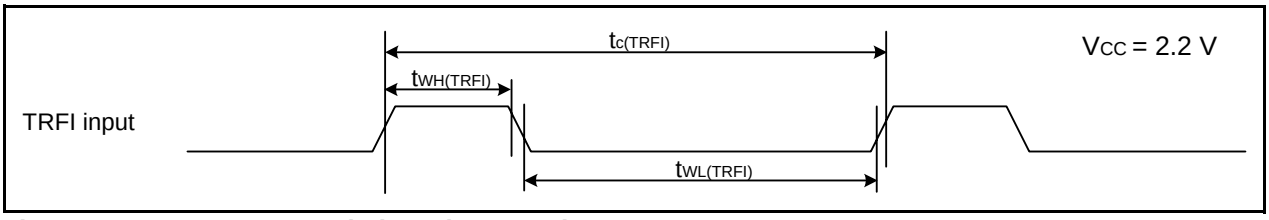
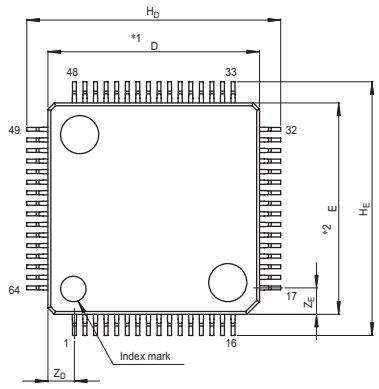


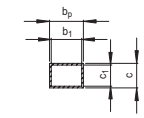

**Figure 5.20 TRFI Input Timing Diagram when Vcc = 2.2 V**

# Package Dimensions

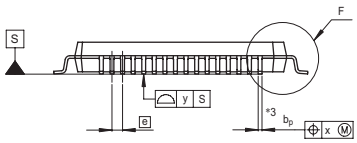
Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

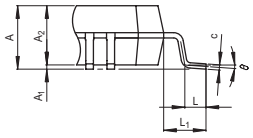
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP64-10x10-0.50 | PLQP0064KB-A | 64P6Q-A / FP-64K / FP-64KV | 0.3g |




Terminal cross section



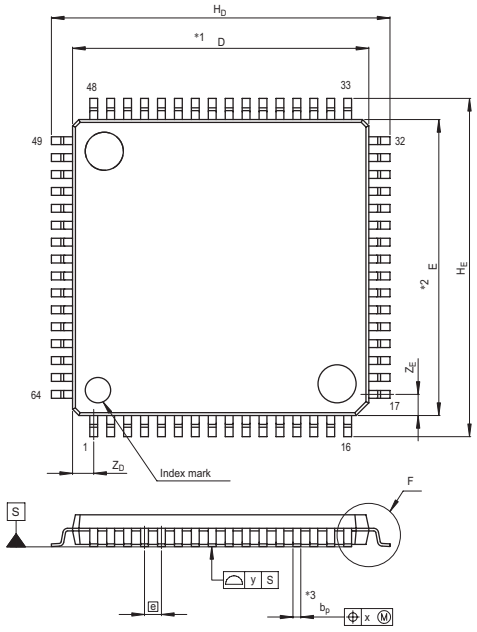



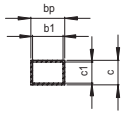

Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

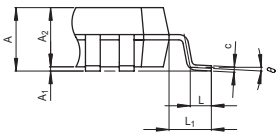
| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP64-14x14-0.80 | PLQP0064GA-A | 64P6U-A/ — | 0.7g |




Terminal cross section




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0 | 0.1 | 0.2 |
| $b_p$ | 0.32 | 0.37 | 0.42 |
| $b_1$ | — | 0.35 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.8 | — |
| x | — | — | 0.20 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.0 | — |
| $Z_E$ | — | 1.0 | — |
| L | 0.3 | 0.5 | 0.7 |
| $L_1$ | — | 1.0 | — |

# General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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