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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136acdfp-v0

Table 1.4 Product List for R8C/36C Group (2)

Current of Nov 2010

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F21364CDFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	D version	
R5F21365CDFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CDFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CDFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CDFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACDFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CDFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CDFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CDFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CDFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CDFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACDFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CDFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CDFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CDFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CDFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CDFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACDFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCDFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		
R5F21364CDXXXFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	N version	Factory programming product
R5F21365CDXXXFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CDXXXFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CDXXXFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CDXXXFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACDXXXFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCDXXXFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CDXXXFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CDXXXFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CDXXXFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CDXXXFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CDXXXFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACDXXXFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCDXXXFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CDXXXFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CDXXXFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CDXXXFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CDXXXFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CDXXXFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACDXXXFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCDXXXFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		

(D): Under development

Note:

1. The user ROM is programmed before shipment.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h	Timer RF Register	TRF	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah	Timer RF Control Register 0	TRFCR0	00h
009Bh	Timer RF Control Register 1	TRFCR1	00h
009Ch	Capture and Compare 0 Register	TRFM0	00h
009Dh			00h
009Eh	Compare 1 Register	TRFM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			XXh
00A9h	UART2 Transmit/Receive Mode Register	U2MR	00h
00AAh	UART2 Bit Rate Register	U2BRG	XXh
00ABh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) ⁽¹⁾

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h	Timer RD Control Expansion Register	TRDECR	00h
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

Note:

1. The blank areas are reserved and cannot be accessed by users.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage		−0.3 to 6.5	V
V _I	Input voltage		−0.3 to V _{CC} + 0.3	V
V _O	Output voltage		−0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	−40°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature		−20 to 85 (N version)/ −40 to 85 (D version)	°C
T _{stg}	Storage temperature		−65 to 150	°C

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVCC		—	—	10	Bit
—	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±3	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	20	MHz
			3.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	16	MHz
			2.7 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	10	MHz
			2.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5.0 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				2.2	—	AVCC	V
VIA	Analog input voltage (3)				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.2\text{ to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, and $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.6 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.7 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		10,000 ⁽³⁾	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		-20 ⁽⁷⁾	—	85	°C
—	Data hold time ⁽⁸⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. -40 °C for D version.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

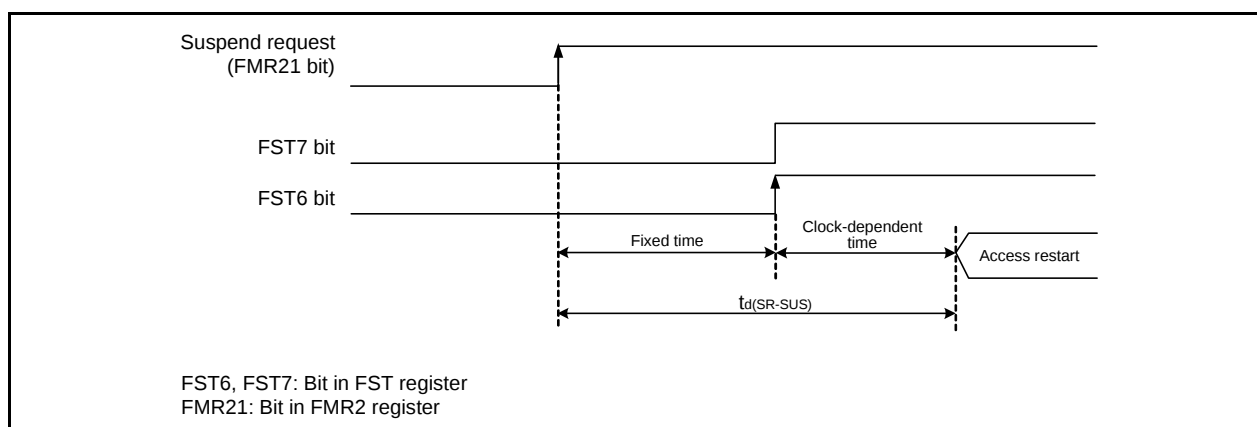
**Figure 5.2 Time delay until Suspend**

Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level Vdet0_0 ⁽²⁾		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 ⁽²⁾		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 ⁽²⁾		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 ⁽²⁾		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time ⁽⁴⁾	At the falling of Vcc from 5.0 V to (Vdet0_0 – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and Topr = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_0 ⁽²⁾	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 ⁽²⁾	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 ⁽²⁾	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 ⁽²⁾	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 ⁽²⁾	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 ⁽²⁾	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽²⁾	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 ⁽²⁾	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 ⁽²⁾	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 ⁽²⁾	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A ⁽²⁾	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B ⁽²⁾	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C ⁽²⁾	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D ⁽²⁾	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E ⁽²⁾	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F ⁽²⁾	At the falling of Vcc	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽³⁾	At the falling of Vcc from 5.0 V to (Vdet1_0 – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and Topr = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.10 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time (2)	At the falling of Vcc from 5.0 V to (Vdet2_0 – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts (3)		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
trth	External power Vcc rise gradient	(1)	0	—	50,000	mV/msec

Notes:

1. The measurement condition is T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

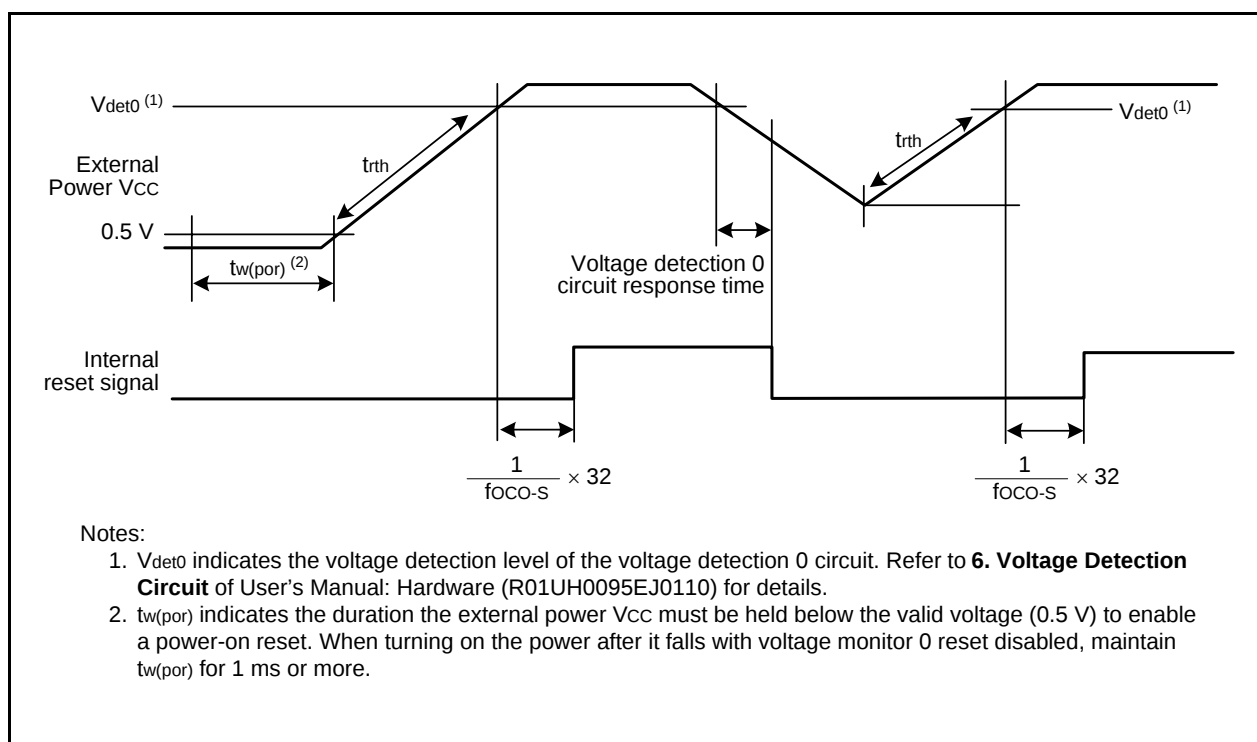
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

Table 5.15 Timing Requirements of Synchronous Serial Communication Unit (SSU)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	—	—	tcyc (2)
tHI	SSCK clock "H" width			0.4	—	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	—	0.6	tsucyc
tRISE	SSCK clock rising time	Master		—	—	1	tcyc (2)
		Slave		—	—	1	μs
tFALL	SSCK clock falling time	Master		—	—	1	tcyc (2)
		Slave		—	—	1	μs
tsu	SSO, SSI data input setup time			100	—	—	ns
tH	SSO, SSI data input hold time			1	—	—	tcyc (2)
tLEAD	SCS setup time	Slave		1tcyc + 50	—	—	ns
tLAG	SCS hold time	Slave		1tcyc + 50	—	—	ns
tOD	SSO, SSI data output delay time			—	—	1	tcyc (2)
tsA	SSI slave access time		2.7 V ≤ Vcc ≤ 5.5 V	—	—	1.5tcyc + 100	ns
			1.8 V ≤ Vcc < 2.7 V	—	—	1.5tcyc + 200	ns
toR	SSI slave out open time		2.7 V ≤ Vcc ≤ 5.5 V	—	—	1.5tcyc + 100	ns
			1.8 V ≤ Vcc < 2.7 V	—	—	1.5tcyc + 200	ns

Notes:

1. Vcc = 1.8 to 5.5 V, Vss = 0 V, and T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.
2. 1tcyc = 1/f1(s)

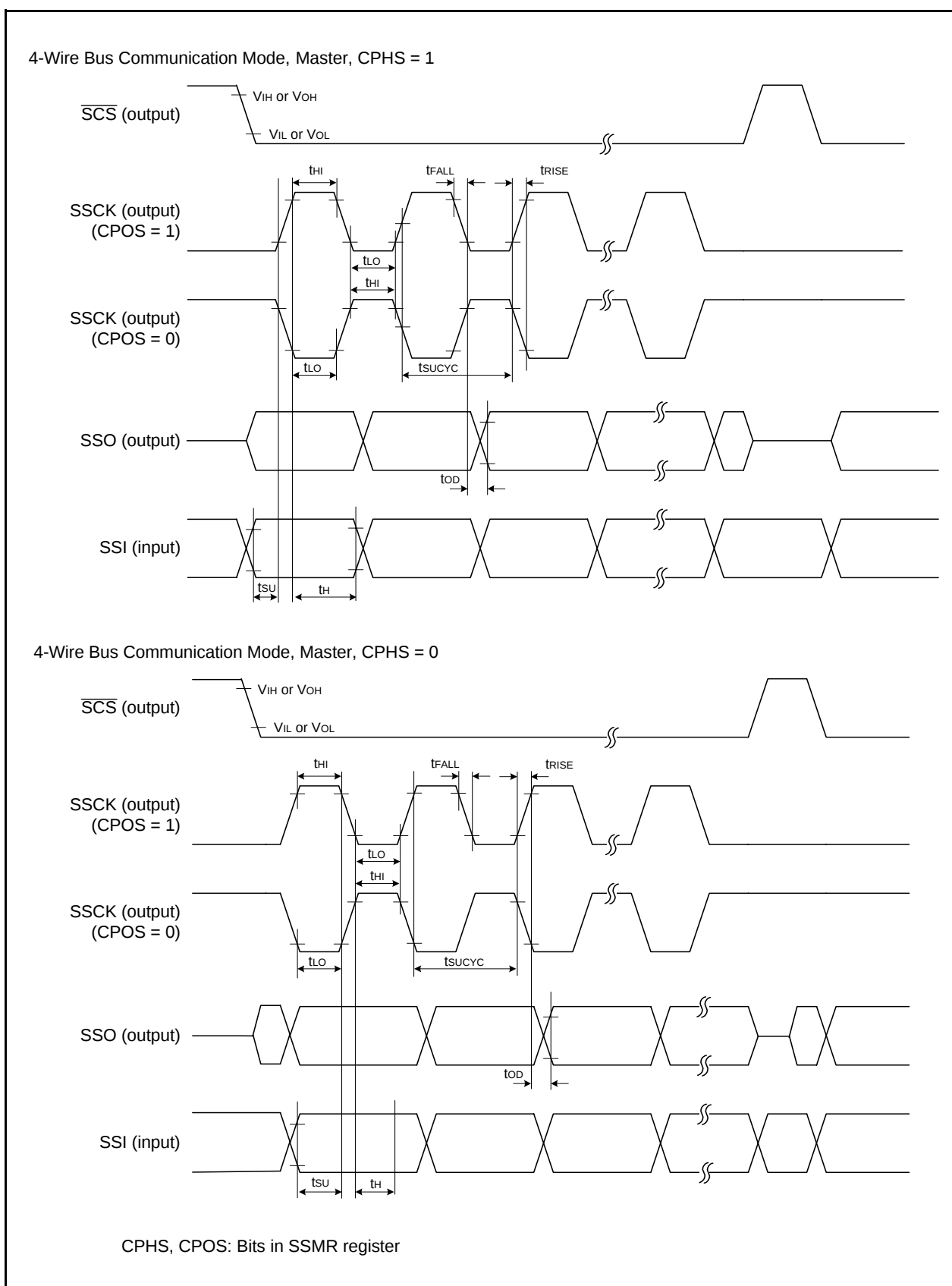


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

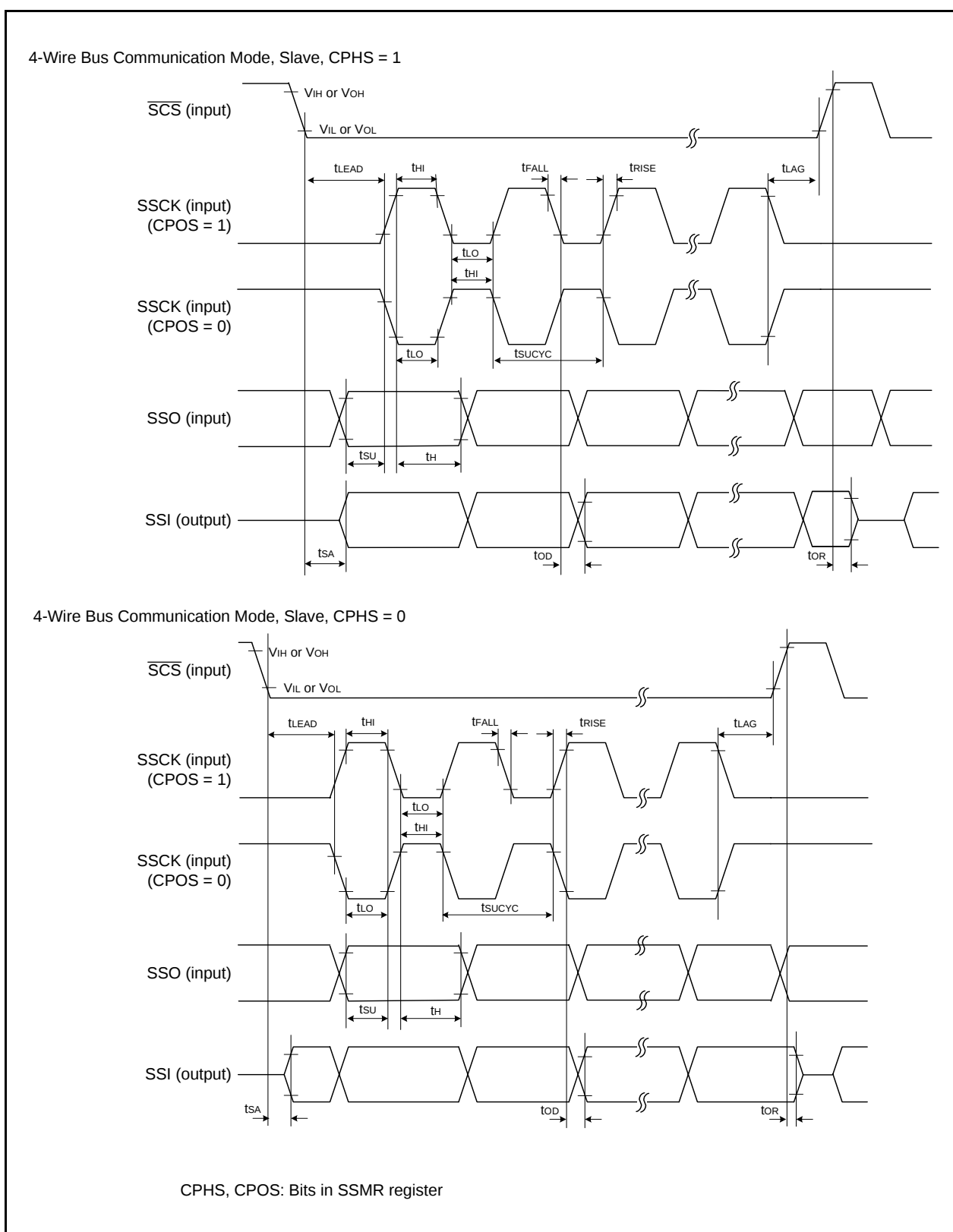


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 5.16 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
tSCL	SCL input cycle time		12tCYC + 600 ⁽²⁾	—	—	ns
tSCLH	SCL input “H” width		3tCYC + 300 ⁽²⁾	—	—	ns
tSCLL	SCL input “L” width		5tCYC + 500 ⁽²⁾	—	—	ns
tSf	SCL, SDA input fall time		—	—	300	ns
tSP	SCL, SDA input spike pulse rejection time		—	—	1tCYC ⁽²⁾	ns
tBUF	SDA input bus-free time		5tCYC ⁽²⁾	—	—	ns
tSTAH	Start condition input hold time		3tCYC ⁽²⁾	—	—	ns
tSTAS	Retransmit start condition input setup time		3tCYC ⁽²⁾	—	—	ns
tSTOP	Stop condition input setup time		3tCYC ⁽²⁾	—	—	ns
tSDAS	Data input setup time		1tCYC + 40 ⁽²⁾	—	—	ns
tSDAH	Data input hold time		10	—	—	ns

Notes:

1. $V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.
2. $1/t_{CYC} = 1/f_1$ (s)

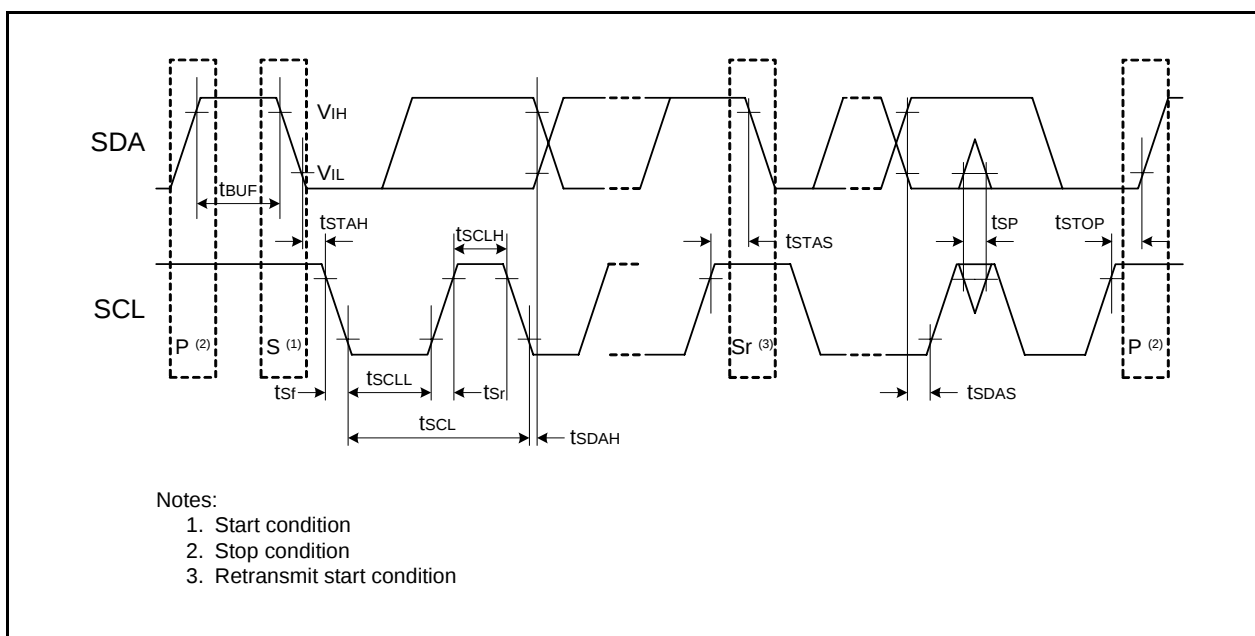
Figure 5.7 I/O Timing of I²C bus Interface

Table 5.17 Electrical Characteristics (1) [4.2 V ≤ V_{CC} ≤ 5.5 V]

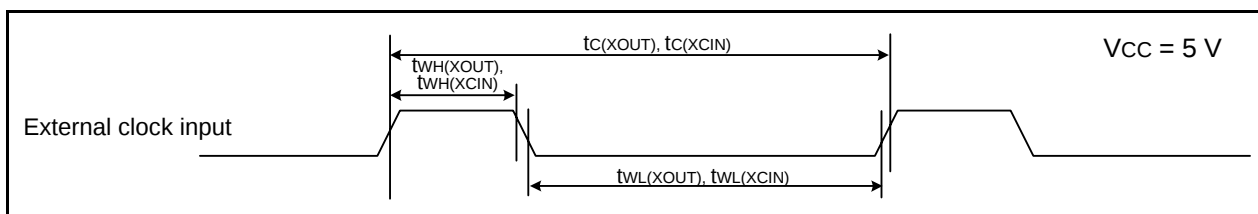
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High V _{CC} = 5 V	I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity Low V _{CC} = 5 V	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		XOUT	V _{CC} = 5 V	I _{OH} = -200 μA	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High V _{CC} = 5 V	I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity Low V _{CC} = 5 V	I _{OL} = 5 mA	—	—	2.0	V
		XOUT	V _{CC} = 5 V	I _{OL} = 200 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, INT4, K10, K11, K12, K13, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, TRGIOA, TRGIOB, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5.0 V		—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5.0 V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5.0 V		25	50	100	kΩ
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

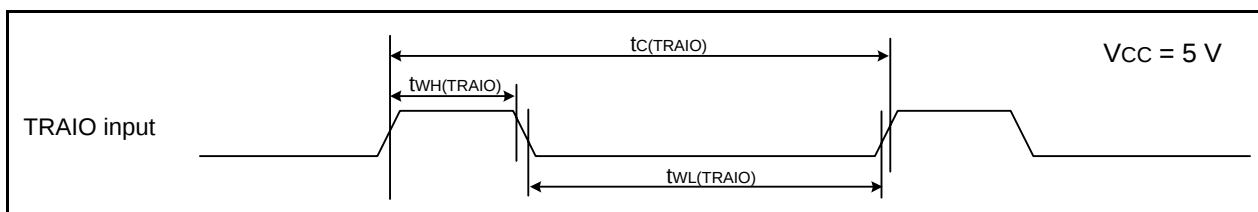
- 4.2 V ≤ V_{CC} ≤ 5.5 V, T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), and f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements (Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_{opr} = 25\text{ }^{\circ}\text{C}$)**Table 5.19 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input "H" width	24	—	ns
$t_{WL(XOUT)}$	XOUT input "L" width	24	—	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	—	μs
$t_{WH(XCIN)}$	XCIN input "H" width	7	—	μs
$t_{WL(XCIN)}$	XCIN input "L" width	7	—	μs

**Figure 5.8 External Clock Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.20 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	—	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	—	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	—	ns

**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.21 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	400 (1)	—	ns
$t_{WH(TRFI)}$	TRFI input "H" width	200 (2)	—	ns
$t_{WL(TRFI)}$	TRFI input "L" width	200 (2)	—	ns

Notes:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

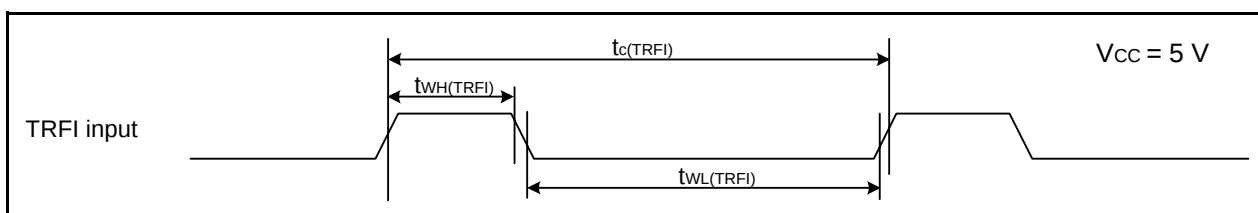
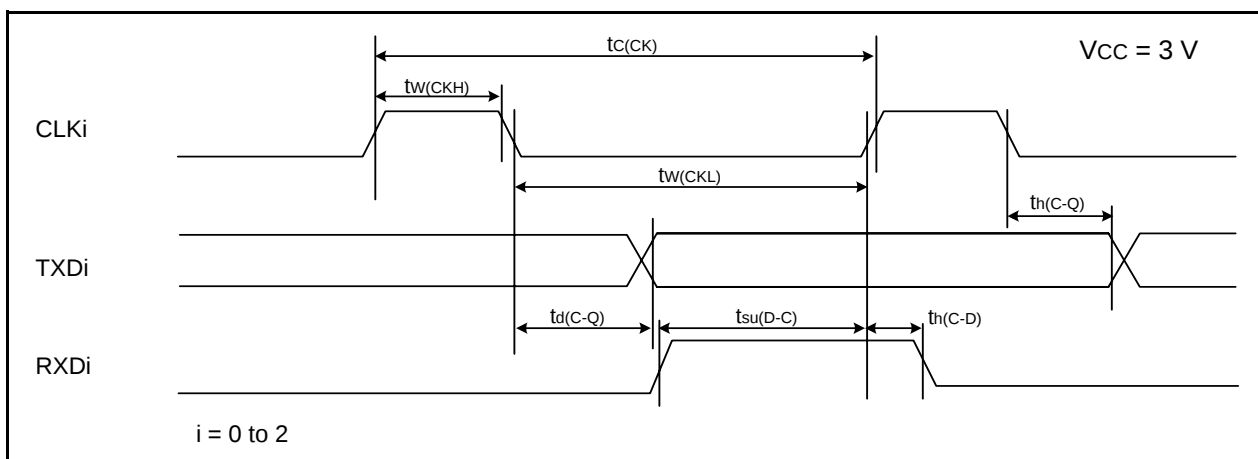
**Figure 5.10 TRFI Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.25 Electrical Characteristics (4) [$2.7\text{ V} \leq V_{CC} \leq 3.3\text{ V}$]
($T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	4.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRD = MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	390	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	—	80	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	—	40	—	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	μA
		Stop mode	XIN clock off, T _{opr} = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	μA
			XIN clock off, T _{opr} = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	μA

Table 5.29 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.16 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.30 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 4$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	380 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	380 (2)	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

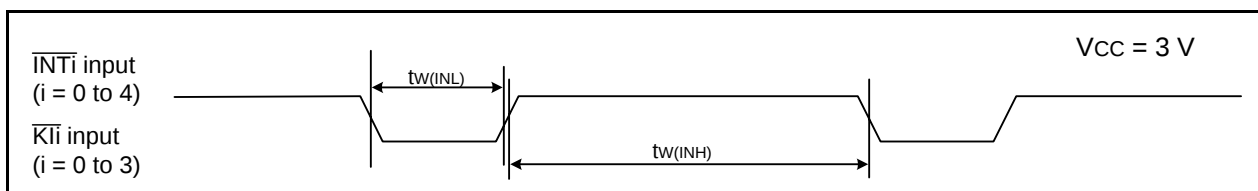
**Figure 5.17 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 3 V**

Table 5.31 Electrical Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]

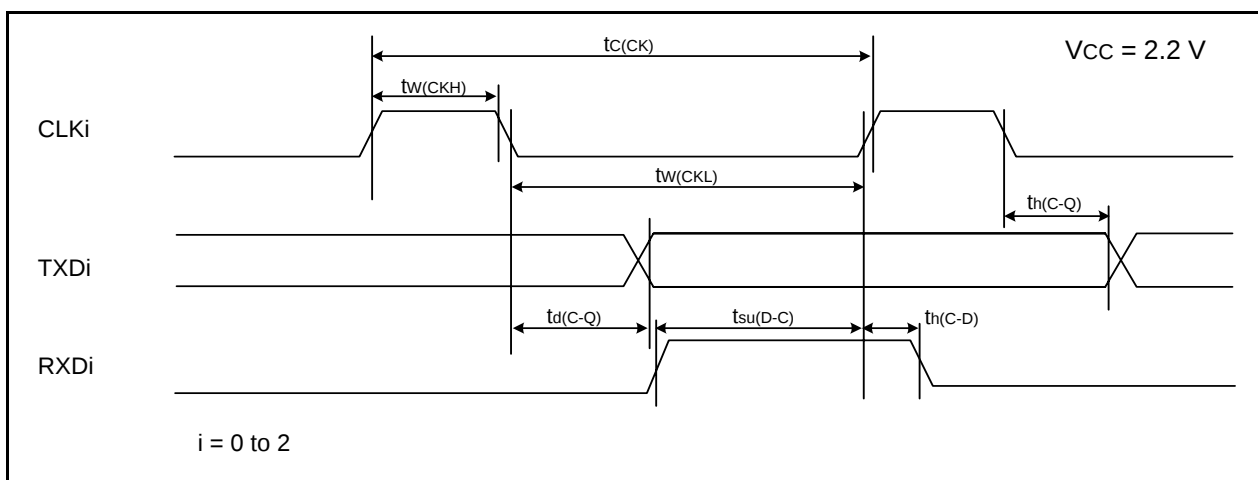
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{NT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT2}}$, $\overline{\text{INT3}}$, $\overline{\text{INT4}}$, $\overline{\text{KI0}}$, $\overline{\text{KI1}}$, $\overline{\text{KI2}}$, $\overline{\text{KI3}}$, $\overline{\text{TRAIO}}$, $\overline{\text{TRBO}}$, $\overline{\text{TRCIOA}}$, $\overline{\text{TRCIOB}}$, $\overline{\text{TRCIOC}}$, $\overline{\text{TRCIOD}}$, $\overline{\text{TRDIOA0}}$, $\overline{\text{TRDIOB0}}$, $\overline{\text{TRDIOC0}}$, $\overline{\text{TRDIOD0}}$, $\overline{\text{TRDIOA1}}$, $\overline{\text{TRDIOB1}}$, $\overline{\text{TRDIOC1}}$, $\overline{\text{TRDIOD1}}$, $\overline{\text{TRCTRG}}$, $\overline{\text{TRCCLK}}$, $\overline{\text{TRFI}}$, $\overline{\text{TRGIOA}}$, $\overline{\text{TRGIOB}}$, $\overline{\text{ADTRG}}$, $\overline{\text{RXD0}}$, $\overline{\text{RXD1}}$, $\overline{\text{RXD2}}$, $\overline{\text{CLK0}}$, $\overline{\text{CLK1}}$, $\overline{\text{CLK2}}$, $\overline{\text{SSI}}$, $\overline{\text{SCL}}$, $\overline{\text{SDA}}$, $\overline{\text{SSO}}$			0.05	0.20	—	V
		$\overline{\text{RESET}}$			0.05	0.20	—	V
I _{IH}	Input "H" current		V _I = 2.2 V, V _{CC} = 2.2 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 2.2 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 2.2 V		70	140	300	k Ω
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$, T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), and f(XIN) = 5 MHz, unless otherwise specified.

Table 5.36 Serial Interface

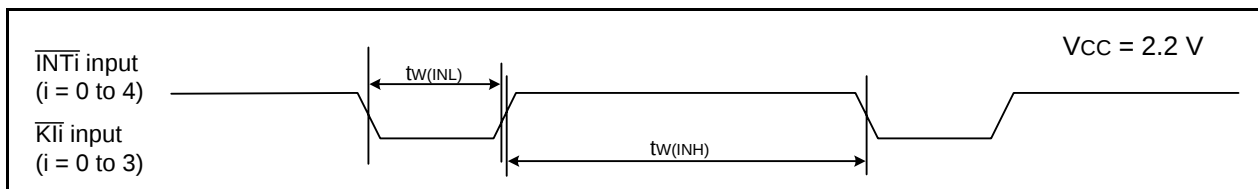
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.21 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.37 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 4$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	1000 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	1000 (2)	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

**Figure 5.22 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 2.2 V**

