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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136acnfa-30

Email: info@E-XFL.COM

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1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/36C Group.

Table 1.1	Specifications for R8C/36C Group (1)
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Item	Function	Specification			
CPU	Central processing	R8C CPU core			
	unit	Number of fundamental instructions: 89			
		Minimum instruction execution time:			
		50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)			
		200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V)			
		• Multiplier: 16 bits \times 16 bits \rightarrow 32 bits			
		• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits \rightarrow 32 bits			
		Operation mode: Single-chip mode (address space: 1 Mbyte)			
Memory	ROM, RAM, Data flash	Refer to Table 1.3 Product List for R8C/36C Group			
Power Supply	Voltage detection	Power-on reset			
Voltage	circuit	Voltage detection 3 (detection level of voltage detection 0 and voltage			
Detection		detection 1 selectable)			
I/O Ports	Programmable I/O	Input-only: 1 pin			
	ports	CMOS I/O ports: 59, selectable pull-up resistor High current drive ports: 59			
Clock	Clock generation	4 circuits: XIN clock oscillation circuit,			
	circuits	XCIN clock oscillation circuit (32 kHz),			
		High-speed on-chip oscillator (with frequency adjustment function),			
		Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function			
		Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16			
		Low power consumption modes:			
		Standard operating mode (high-speed clock, low-speed clock, high-speed on-			
		chip oscillator, low-speed on-chip oscillator), wait mode, stop mode			
		Real-time clock (timer RE)			
Interrupts		Interrupt Vectors: 69			
•		• External: 9 sources (INT × 5, key input × 4)			
		Priority levels: 7 levels			
Watchdog Tim	er	• 14 bits x 1 (with prescaler)			
		Reset start selectable			
		 Low-speed on-chip oscillator for watchdog timer selectable 			
DTC (Data Tra	nsfer Controller)	• 1 channel			
		Activation sources: 39			
	Γ	Transfer modes: 2 (normal mode, repeat mode)			
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler)			
		Timer mode (period timer), pulse output mode (output level inverted every			
		period), event counter mode, pulse width measurement mode, pulse period			
	Timer DD	measurement mode			
	Timer RB	8 bits x 1 (with 8-bit prescaler)			
		Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-			
		shot generation mode			
	Timer RC	16 bits × 1 (with 4 capture/compare registers)			
		Timer mode (input capture function, output compare function), PWM mode			
		(output 3 pins), PWM2 mode (PWM output pin)			
	Timer RD	16 bits x 2 (with 4 capture/compare registers)			
		Timer mode (input capture function, output compare function), PWM mode			
		(output 6 pins), reset synchronous PWM mode (output three-phase			
		waveforms (6 pins), sawtooth wave modulation), complementary PWM mode			
		(output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)			
		mode (F www.output z pins with lixed penod)			



1.3 Block Diagram

Figure 1.2 shows a Block Diagram.





				I/O Pin Functions for Peripheral Modules				
Pin Number	Control Pin	Port	Interrupt	Timer	Serial Interface	SSU	l ² C bus	A/D Converter, D/A Converter, Comparator B
40		P4_5	INT0		(RXD2/SCL2)			ADTRG
41		P1_7	INT1	(TRAIO)				IVCMP1
42		P1_6			(CLK0)			IVREF1
43		P1_5	(INT1)	(TRAIO)	(RXD0)			
44		P1_4		(TRCCLK)	(TXD0)			
45		P1_3	KI3	TRBO (/TRCIOC)				AN11
46		P1_2	KI2	(TRCIOB)				AN10
47		P1_1	KI1	(TRCIOA/TRCTRG)				AN9
48		P1_0	KI0	(TRCIOD)				AN8
49		P0_7		(TRCIOC)				AN0/DA1
50		P0_6		(TRCIOD)				AN1/DA0
51		P0_5		(TRCIOB)				AN2
52		P0_4		TREO(/TRCIOB)				AN3
53		P0_3		(TRCIOB)	(CLK1)			AN4
54		P0_2		(TRCIOA/TRCTRG)	(RXD1)			AN5
55		P0_1		(TRCIOA/TRCTRG)	(TXD1)			AN6
56		P0_0		(TRCIOA/TRCTRG)				AN7
57		P6_4			(RXD1)			
58		P6_3			(TXD1)			
59		P6_2			(CLK1)			
60		P6_1						
61		P6_0		(TREO)				
62		P5_7		(TRGIOB)				
63		P5_6		(TRAO/TRGIOA)				
64		P3_2	(INT1/ INT2)	(TRAIO/TRGCLKB)				

Table 1.6 Pin Name Information by Pin Number (2)

Note:

1. Can be assigned to the pin in parentheses by a program.



1.5 Pin Functions

Tables 1.7 and 1.8 list Pin Functions.

Table 1.7Pin Functions (1)

Item	Pin Name	I/O Type	
Power supply input	VCC, VSS	—	Apply 1.8 to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS		Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input XIN clock output	XIN XOUT	I I/O	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. ⁽¹⁾ To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O.
XCIN clock output	XCOUT	0	Connect a crystal oscillator between the XCIN and XCOUT pins. ⁽¹⁾ To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
INT interrupt input	INT0 to INT4	I	INT interrupt input pins.
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	0	Timer RA output pin.
Timer RB	TRBO	0	Timer RB output pin.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins.
	TRDCLK	I	External clock input pin.
Timer RE	TREO	0	Divided clock output pin.
Timer RF	TRFO00, TRFO10, TRFO01,TRFO11, TRFO02,TRFO12	О	Timer RF output pins.
	TRFI	I	Timer RF input pin.
Timer RG	TRGIOA, TRGIOB	I/O	Timer RG I/O ports.
	TRGCLKA, TRGCLKB	I	External clock input pins.
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins.
	RXD0, RXD1, RXD2	I	Serial data input pins.
	TXD0, TXD1, TXD2	0	Serial data output pins.
	CTS2	I	Transmission control input pin.
	RTS2	0	Reception control output pin.
	SCL2	I/O	I ² C mode clock I/O pin.
	SDA2	I/O	I ² C mode data I/O pin.

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.



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0139hTimer RD PWM Mode RegisterTRDPMR10001000b013AhTimer RD Function Control RegisterTRDFCR1000000b013BhTimer RD Output Master Enable Register 1TRDOER1FFh013ChTimer RD Output Master Enable Register 2TRDOER201111111b013DhTimer RD Output Control RegisterTRDOCR00h013EhTimer RD Digital Filter Function Select Register 0TRDDF000h				
013Ah Timer RD Function Control Register TRDFCR 1000000b 013Bh Timer RD Output Master Enable Register 1 TRDOER1 FFh 013Ch Timer RD Output Master Enable Register 2 TRDOER2 01111111b 013Dh Timer RD Output Control Register TRDOCR 00h 013Eh Timer RD Digital Filter Function Select Register 0 TRDDF0 00h				
013Bh Timer RD Output Master Enable Register 1 TRDOER1 FFh 013Ch Timer RD Output Master Enable Register 2 TRDOER2 0111111b 013Dh Timer RD Output Control Register TRDOCR 00h 013Eh Timer RD Digital Filter Function Select Register 0 TRDDF0 00h				
013Bh Timer RD Output Master Enable Register 1 TRDOER1 FFh 013Ch Timer RD Output Master Enable Register 2 TRDOER2 0111111b 013Dh Timer RD Output Control Register TRDOCR 00h 013Eh Timer RD Digital Filter Function Select Register 0 TRDDF0 00h		Timer RD Function Control Register		1000000b
013Ch Timer RD Output Master Enable Register 2 TRDOER2 0111111b 013Dh Timer RD Output Control Register TRDOCR 00h 013Eh Timer RD Digital Filter Function Select Register 0 TRDDF0 00h	013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Dh Timer RD Output Control Register TRDOCR 00h 013Eh Timer RD Digital Filter Function Select Register 0 TRDDF0 00h				
013Eh Timer RD Digital Filter Function Select Register 0 TRDDF0 00h				
013Fh Imer RD Digital Filter Function Select Register 1 TRDDF1 00h				
	013Fh	וmer אט Digital Filter Function Select Register 1	TRUDF1	UUh

SFR Information (5)⁽¹⁾ Table 4.5

Note: 1. The blank areas are reserved and cannot be accessed by users.



Address	Pogiator	Symbol	After Reset
Address	Register	Symbol	
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h	Timer RF Output Control Register	TRFOUT	00h
		U0SR	
0188h	UARTO Pin Select Register		00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			0011
0190h			
		+	
0192h		0000	44444000
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register ⁽²⁾	SSRDR / ICDRR	FFh
0197h		SSRDRH	FFh
	SS Receive Data Register H ⁽²⁾		
0198h	SS Control Register H / IIC bus Control Register 1 ⁽²⁾	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register ⁽²⁾	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register ⁽²⁾	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			1
01ADh		<u> </u>	
01AEh			
01AEh		+	
01B0h			
		+	
01B1h		FOT	400000000
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			<u> </u>
01BAh			1
01BBh		ļ	
01BCh			
01BDh			
01BEh			
01BFh			
Villadofined			

Table 4.7SFR Information (7) (1)

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.

2. Selectable by the IICSEL bit in the SSUIICSR register.



Table 4.8	SFR Information ((8) (1)
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		<u> </u>	
Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D0h			
01D2h		+	+
01D3h			-
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DBh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h	Pull-Up Control Register 2	PUR2	00h
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh		1	
01EEh			1
01EFh		1	1
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F0h	Port P2 Drive Capacity Control Register	P2DRR	00h
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
	Drive Capacity Control Register 2	DRR2	00h
01F4h			0.01-
01F5h	Input Threshold Control Register 0	VLT0	00h
01F5h 01F6h	Input Threshold Control Register 0 Input Threshold Control Register 1	VLT1	00h
01F5h 01F6h	Input Threshold Control Register 0 Input Threshold Control Register 1		
01F5h 01F6h 01F7h	Input Threshold Control Register 0 Input Threshold Control Register 1 Input Threshold Control Register 2	VLT1	00h
01F5h 01F6h 01F7h 01F8h	Input Threshold Control Register 0 Input Threshold Control Register 1	VLT1 VLT2	00h 00h
01F5h 01F6h 01F7h 01F8h 01F9h	Input Threshold Control Register 0 Input Threshold Control Register 1 Input Threshold Control Register 2 Comparator B Control Register 0	VLT1 VLT2 INTCMP	00h 00h 00h
01F5h 01F6h 01F7h 01F8h 01F9h 01F9h	Input Threshold Control Register 0 Input Threshold Control Register 1 Input Threshold Control Register 2 Comparator B Control Register 0 External Input Enable Register 0	VLT1 VLT2 INTCMP INTEN	00h 00h 00h 00h
01F5h 01F6h 01F7h 01F8h 01F9h 01FAh 01FBh	Input Threshold Control Register 0 Input Threshold Control Register 1 Input Threshold Control Register 2 Comparator B Control Register 0 External Input Enable Register 0 External Input Enable Register 1	VLT1 VLT2 INTCMP INTEN INTEN1	00h 00h 00h 00h 00h 00h
01F5h 01F6h 01F7h 01F8h 01F9h 01FAh 01FBh 01FCh	Input Threshold Control Register 0 Input Threshold Control Register 1 Input Threshold Control Register 2 Comparator B Control Register 0 External Input Enable Register 0 External Input Enable Register 1 INT Input Filter Select Register 0	VLT1 VLT2 INTCMP INTEN INTEN1 INTF	00h 00h 00h 00h 00h 00h 00h
01F5h 01F6h 01F7h 01F8h 01F9h 01FAh 01FBh 01FBh 01FCh 01FDh	Input Threshold Control Register 0 Input Threshold Control Register 1 Input Threshold Control Register 2 Comparator B Control Register 0 External Input Enable Register 0 External Input Enable Register 1 INT Input Filter Select Register 0 INT Input Filter Select Register 1	VLT1 VLT2 INTCMP INTEN INTEN1 INTF INTF1	00h 00h 00h 00h 00h 00h 00h 00h
01F5h 01F6h 01F7h 01F8h 01F9h 01FAh 01FBh 01FCh	Input Threshold Control Register 0 Input Threshold Control Register 1 Input Threshold Control Register 2 Comparator B Control Register 0 External Input Enable Register 0 External Input Enable Register 1 INT Input Filter Select Register 0	VLT1 VLT2 INTCMP INTEN INTEN1 INTF	00h 00h 00h 00h 00h 00h 00h

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.



Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
: 2C3Ah	DTC Transfer Vector Area DTC Transfer Vector Area		XXh XXh
2C3An 2C3Bh	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C3Fii 2C40h	DTC Control Data 0	DTCD0	XXh
2C40n 2C41h			XXh
2C4111 2C42h	4		XXh
2C420 2C43h	4		XXh
2C43h 2C44h	4		XXh
2C440 2C45h	4		XXh
2C45h	•		XXh
2C460 2C47h			XXh
2C47h 2C48h	DTC Control Data 1	DTCD1	XXh
2C40h		ысы	XXh
2C490 2C4Ah			XXh
2C4An 2C4Bh			XXh
2C4Bh 2C4Ch	•		XXh
2C4Ch 2C4Dh	-		XXh
2C4Dh 2C4Eh			XXh
2C4En 2C4Fh			XXh
2C4Fn 2C50h	DTC Control Data 2	DTCD2	XXh
2C50h		DICD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C55h	•		XXh
2C55h			XXh
2C50h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h		DICDS	XXh
2C59h	-		XXh
2C5An 2C5Bh	4		XXh
2C5Bn 2C5Ch	4		XXh
2C5Ch	4		XXh
2C5Dh 2C5Eh	4		XXh
2C5En 2C5Fh	4		XXh
	DTC Control Data 4	DTCD4	
2C60h 2C61h	DTC Control Data 4		XXh XXh
2C61h 2C62h	4		XXh
2C62h	4		XXh
2C63h	4		XXh
2C64h 2C65h	4		XXh
2C65h	4		XXh
2C667h	4		XXh
2C67h 2C68h	DTC Control Data 5	DTCD5	XXh
2C68h 2C69h		60010	XXh
2C69n 2C6Ah	4		XXh
2C6An 2C6Bh	4		XXh
	4		XXn XXh
2C6Ch	4		
2C6Dh	4		XXh
2C6Eh 2C6Fh	4		XXh
	1		XXh

Table 4.9SFR Information (9) (1)

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Autor Reser Option Option Option Autor Reser 202811 202811 209 <td< th=""><th>Address</th><th>Desister</th><th>Cumple al</th><th>After Deset</th></td<>	Address	Desister	Cumple al	After Deset
2281h 2081h 2288h 2084h 2084h 2084h 2084h 2084h 2084h 2084h 2085h DTC Control Data 15 2086h DTC Control Data 16 2000h DTC Control Data 17 2000h DTC Control Data 18 2000h DTC Control Data 18 2000h DTC Control Data 18 2000h ZODH 2000h ZODH	Address	Register	Symbol	After Reset
2281h 2282h Xh Xh 2283h 2284h Xh Xh 2288h 228h Xh Xh 228h 2267h Xh Xh 228h 2267h Xh Xh 228h DTC Control Data 15 Xh Xh 228h 2268h Xh Xh 228h 2268h Xh Xh 228h 2267h Xh Xh 228h 2267h Xh Xh 228h 2267h Xh Xh 228h ZCOh Xh Xh 2260h ZCOh Xh Xh 2200h DTC Control Data 16 DTCD16 Xh 200ch Xh Xh Xh 200ch ZCOh Xh Xh 200ch ZCOh Xh Xh 200ch ZCOh Xh Xh 200ch ZCOh Xh Xh 200ch	2CB0h	DTC Control Data 14	DTCD14	XXh
2282h 228bh 288b 288b				
2283h Xh Xh 2284h Xh Xh 2284h ZCBh Xh 2284h ZCBh Xh 2284h ZCBh Xh 2284h DTC Control Data 15 Xh 2288h ZCBh Xh 2208h ZCCh Xh 2005h DTC Control Data 16 DTCD16 Xh 2005h Xh Xh Xh 2005h ZCCh Xh Xh 2005h </td <td></td> <td></td> <td></td> <td></td>				
228hn XNn 228hn DTC Control Data 15 DTCD15 XXn 228hn ZC8hn XXn XXn 228hn DTC Control Data 15 DTCD15 XXn 228hn ZC8hn XXn XXn 228hn ZC8hn XXn XXn 228hn ZC8hn XXn XXn 228hn ZC8hn XXn XXn 228hn XXn XXn XXn 208hn XXn XXn XXn 208hn XXn XXn XXn 2020hn DTC Control Data 16 DTCD16 XXn 2020hn ZC20hn XXn XXn 2020hn ZC60hn XXn XXn 2020hn DTC Control Data 17 ZXn XXn 2020hn ZC70h XXn XXn 2020hn ZC70h XXn XXn 2020hn ZC70hn XXn XXn 2020hn ZC70hn XXn XXn	2CB2h			XXh
228hn XNn 228hn DTC Control Data 15 DTCD15 XXn 228hn ZC8hn XXn XXn 228hn DTC Control Data 15 DTCD15 XXn 228hn ZC8hn XXn XXn 228hn ZC8hn XXn XXn 228hn ZC8hn XXn XXn 228hn ZC8hn XXn XXn 228hn XXn XXn XXn 208hn XXn XXn XXn 208hn XXn XXn XXn 2020hn DTC Control Data 16 DTCD16 XXn 2020hn ZC20hn XXn XXn 2020hn ZC60hn XXn XXn 2020hn DTC Control Data 17 ZXn XXn 2020hn ZC70h XXn XXn 2020hn ZC70h XXn XXn 2020hn ZC70hn XXn XXn 2020hn ZC70hn XXn XXn	2CB3h			XXh
2285h Xh 2285h Xh 2285h Xh 2285h Xh 2285h Xh 2285h DTC Control Data 15 Xh 2285h Xh Xh 2267h DTC Control Data 15 Xh 2205h ZCCh Xh 2202h Xh Xh 2202h Xh Xh 2020h ZCCh Xh 2020h ZCCh Xh 2020h ZCCh Xh 2020h ZCOh Xh 2020h ZCOh Xh 2020h Xh Xh 2020h Xh Xh 2020h Xh Xh 2020h Xh </td <td></td> <td>-</td> <td></td> <td></td>		-		
2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2267h 2262h 2				
2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2267h 2262h 2	2CB5h			XXh
2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2268h 2266h DTC Control Data 15 Xh 2268h 226bh 2266h DTC Control Data 16 TCD15 Xh 2268h 2266h DTC Control Data 16 TCD16 Xh 2268h 2266h DTC Control Data 16 TCD16 Xh 2266h Xh Xh Xh 2266h TC Control Data 16 TCD16 Xh 2266h Xh Xh Xh 2266h TC Control Data 16 TCD17 Xh 2262h Xh Xh Xh 2262h TC Control Data 17 TCD17 Xh 2262h TC Control Data 17 TCD17 Xh 2262h TXh Xh Xh 2262h TC Control Data 17 TXh Xh 2262h TX Xh Xh 2262h TXh Xh Xh 2262h TXh Xh Xh 220bh TXh Xh Xh 220bh TXh				
2268h DTC Control Data 15 XXh 2268h ZCBAN XXh 2208h DTC Control Data 16 XXh 2202h XXh XXh 2020h DTC Control Data 16 XXh 2020h XXh XXh 2020h XXh <td></td> <td></td> <td></td> <td></td>				
2208h 208h 208h 208h 208h 208h 208h 208h	2CB7h			XXh
2208h 208h 208h 208h 208h 208h 208h 208h	2CB8h	DTC Control Data 15	DTCD15	XXh
2208An 2208Bn 2208Dn 2208Dn 2208Dn 2208Dn 2208Dn 2208Dn 2202Dn			BIODIS	
2288h 2288h 2289h 2289h 2289h Xh Xh 2289h 2209h DTC Control Data 16 Xh Xh 22001 Xh Xh Xh 22001 Xh Xh Xh 2001 Xh Xh Xh 2001 Xh Xh Xh 2001 Xh Xh Xh 2001 Xh Xh Xh 2002h Xh Xh Xh 2005h DTC Control Data 18 DTCD18 Xh 2005h Xh Xh Xh 2005h Xh Xh Xh 2005h Yh Xh Xh 2005h Xh <t< td=""><td></td><td></td><td></td><td></td></t<>				
2288h 2288h 2289h 2289h 2289h Xh Xh 2289h 2209h DTC Control Data 16 Xh Xh 22001 Xh Xh Xh 22001 Xh Xh Xh 2001 Xh Xh Xh 2001 Xh Xh Xh 2001 Xh Xh Xh 2001 Xh Xh Xh 2002h Xh Xh Xh 2005h DTC Control Data 18 DTCD18 Xh 2005h Xh Xh Xh 2005h Xh Xh Xh 2005h Yh Xh Xh 2005h Xh <t< td=""><td>2CBAh</td><td></td><td></td><td>XXh</td></t<>	2CBAh			XXh
2282b7 2282b7 2282b7 2282b7 2282b7 22857 2202b7 22857 2202b7 22010 2202b7 22010 2202b7 22010 2202b7 2202b7 2202b7 2020b7 2020b7				
22000h 22007h				
2288Fn XXh 2208Fn XXh 2208Fn TC Control Data 16 22000 DTC Control Data 16 20000 XXh	2CBCh			XXh
2288Fn XXh 2208Fn XXh 2208Fn TC Control Data 16 22000 DTC Control Data 16 20000 XXh	2CBDh			XXh
22CBFh SXh 22C0h DTC Control Data 16 Xh 2CC2h Xh Xh 2CC2h Xh Xh 2CC3h ZCC4h Xh 2CC4h Xh Xh 2CC5h Xh Xh 2CC6h DTC Control Data 17 Xh 2CC9h DTC Control Data 17 Xh 2CC9h ZCC0h Xh 2CC9h DTC Control Data 17 Xh 2CC9h ZCC0h Xh 2C0Ph DTC Control Data 18 Xh 2C0Ph ZCC0h Xh 2C0Ph ZCCh Xh 2C0Ph ZCCh Xh 2C0Ph ZCCh Xh 2C0Ph ZCCh Xh 2C0Ph ZCAn		-		
22C0h DTC Control Data 16 Xh 22C0h Xh Xh 22C2h Xh Xh 22C3h Xh Xh 22C3h Xh Xh 22C3h Xh Xh 22C5h Xh				
22C0h DTC Control Data 16 Xh 22C0h Xh Xh 22C2h Xh Xh 22C3h Xh Xh 22C3h Xh Xh 22C3h Xh Xh 22C5h Xh	2CBFh			XXh
2CC1h Xh 2CC2h Xh 2CC3h Xh 2CC4h Xh 2CC5h Xh 2CC6h Xh 2CC6h DTC Control Data 17 2CC6h Xh 2CD6h Xh		DTC Control Data 16	DTCD16	
2CC2h Xxh Xxh 2CC3h Xxh Xxh 2CC5h Xxh Xxh 2CC6h Xxh Xxh 2CC6h DTC Control Data 18 DTCD18 Xxh 2C05h Xxh Xxh Xxh 2C05h Xxh Xxh Xxh 2C05h DTC Control Data 19 DTCD19 Xxh 2C05h Xxh Xxh Xxh 2C05h ZC5h Xxh Xxh 2C05h		DTC Control Data To	DICDI6	
2CC3h XXh XXh 2CC5h XXh XXh 2CC6h XXh XXh 2CC6h XXh XXh 2CC8h XXh XXh 2CC9h XXh XXh 2CC9h XXh XXh 2CC9h XXh XXh 2CC9h XXh XXh 2CC0h XXh XXh 2C0h	2CC1h			XXh
2CC3h XXh XXh 2CC5h XXh XXh 2CC6h XXh XXh 2CC6h XXh XXh 2CC8h XXh XXh 2CC9h XXh XXh 2CC9h XXh XXh 2CC9h XXh XXh 2CC9h XXh XXh 2CC0h XXh XXh 2C0h	2CC2h	1		XXh
22C2h Xh Xh 22C5h Xh Xh 22C3h DTC Control Data 17 DTCD17 Xkh 22C3h ZCCAh Xkh Xkh 22C3h DTC Control Data 17 DTCD17 Xkh 22C3h Xxh Xxh Xxh 22C3h Xxh Xxh Xxh 22C5h Xxh Xxh Xxh 22C2h Xxh Xxh Xxh 22C2h Xxh Xxh Xxh 22C5h Xxh Xxh Xxh 22C2h Xxh Xxh Xxh 22C5h Xxh		4		
2CCSh Xxh 2CCSh Xxh 2CCCh Xxh 2CCBh DTC Control Data 17 DTCD17 2CCBh Xxh 2CCBh Xxh 2CCBh Xxh 2CCBh Xxh 2CCBh Xxh 2CCBh Xxh 2CCCh Xxh 2CCh Xxh 2CCbh Xxh 2CDAh Xxh		1		
2CCSh Xxh 2CCSh Xxh 2CCCh Xxh 2CCBh DTC Control Data 17 DTCD17 2CCBh Xxh 2CCBh Xxh 2CCBh Xxh 2CCBh Xxh 2CCBh Xxh 2CCBh Xxh 2CCCh Xxh 2CCh Xxh 2CCbh Xxh 2CDAh Xxh	2CC4h			XXh
2CC8h Xh 2CC7h Xh 2CC8h DTC Control Data 17 Xh 2CC8h DTC Control Data 17 Xh 2CC8h XXh XXh 2CC8h XXh XXh 2CC8h XXh XXh 2CC6h XXh XXh 2CC6h XXh XXh 2CC6h XXh XXh 2CC9h ZCC0h XXh 2CC9h DTC Control Data 18 DTCD18 Xh 2C03h ZC04h Xh Xh 2C04h Xh Xh Xh 2C05h ZC6h Xh Xh 2C05h ZC6h Xh		1		
2CC7h Xh 2CC8h DTC Control Data 17 DTC DTC XXh 2CC8h XXh XXh 2CC9h XXh XXh 2CCPh DTC Control Data 18 XXh 2C09h ZCCPh XXh 2C09h DTC Control Data 18 XXh 2C09h XXh XXh 2C09h ZCOPh XXh 2C00h ZCOPh		4		
2CC7h Xh 2CC8h DTC Control Data 17 DTC DTC XXh 2CC8h XXh XXh 2CC9h XXh XXh 2CCPh DTC Control Data 18 XXh 2C09h ZCCPh XXh 2C09h DTC Control Data 18 XXh 2C09h XXh XXh 2C09h ZCOPh XXh 2C00h ZCOPh	2CC6h			XXh
2CC8h DTC Control Data 17 Xxh 2CC8h Xxh Xxh 2CCAh Xxh Xxh 2CCCh Xxh Xxh 2CCDh DTC Control Data 18 DTCD18 Xxh 2CDh Xxh Xxh Xxh 2CDh Xxh Xxh Xxh 2CDh Xxh Xxh Xxh 2CDh Xxh Xxh Xxh 2CDBh DTC Control Data 18 Xxh Xxh 2CDBh DTC Control Data 19 Xxh Xxh 2CDBh DTC Control Data 19 Xxh Xxh 2CDBh ZCDh Xxh Xxh 2CDBh ZCDh Xxh Xxh 2CDBh ZCC Xxh Xxh 2CDFh DTC Control Data 20 ZCAn Xxh		1		
2CC3h Xh 2CC3h Xh 2CCBh Xh 2CCDh Xh 2CCDh Xh 2CCPh TC Control Data 18 2C02h Xh 2C03h Xh 2C04h Xh 2C05h TC Control Data 18 2C05h TC Control Data 19 2C08h DTC Control Data 19 2C08h TC Control Data 19 2C08h TC Control Data 20 2CE2h Xh 2C05h TC Control Data 20 2CE2h Xh 2CE3h TC Control Data 20 2CE3h Xh 2CE3h Xh 2CE3h Xh 2CE3h Xh 2CE3h TC Control Data 20 2CE3h TC Control Data 21 2C		DTO Ocated Data 47	DT00/7	
2CCAh XXh 2CCCh XXh 2CCDh DTC Control Data 18 2CD3h XXh 2CC2h XXh		DTC Control Data 17	DICD17	
2CCAh XXh 2CCCh XXh 2CCDh DTC Control Data 18 2CD3h XXh 2CC2h XXh	2CC9h			XXh
2CCBh Xh 2CCCh Xh 2CCCh Xh 2CCFh Xh 2CCFh Xh 2CCFh Xh 2CCFh Xh 2CCFh Xh 2CCFh Xh 2CDh Xh 2CEh Xh 2				
2CCCh Xh 2CCFh Xh 2CCFh Xh 2CDDh DTC Control Data 18 2CD3h DTC Control Data 18 2CD3h XXh				
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2CE6hXXh2CE7hXXh2CE8hDTC Control Data 212CE9hZCEAh2CEAhXXh2CEBhXXh2CEChXXh2CEBhXXh2CEBhXXh2CEBhXXh2CEFhXXh	2CE4h			XXh
2CE6hXXh2CE7hXXh2CE8hDTC Control Data 212CE9hZCEAh2CEAhXXh2CEBhXXh2CEChXXh2CEBhXXh2CEBhXXh2CEBhXXh2CEFhXXh		1		
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2CE9h XXh 2CEAh XXh 2CEBh XXh 2CECh XXh 2CEDh XXh 2CEEh XXh 2CEFh XXh		DTC Control Data 21	DTOD04	
2CEAhXXh2CEBhXXh2CEChXXh2CEDhXXh2CEEhXXh2CEFhXXh			DICDZI	
2CEAhXXh2CEBhXXh2CEChXXh2CEDhXXh2CEEhXXh2CEFhXXh	2CE9h			XXh
2CEBhXXh2CEChXXh2CEDhXXh2CEEhXXh2CEFhXXh	2CEAh	1		XXh
2CEChXXh2CEDhXXh2CEEhXXh2CEFhXXh		4		
2CEDh XXh 2CEEh XXh 2CEFh XXh				
2CEDh XXh 2CEEh XXh 2CEFh XXh	2CECh	7		XXh
2CEEh XXh 2CEFh XXh		4		
2CEFh XXh				
2CEFh XXh	2CEEh			XXh
		1		
	And the second sec			7711

Table 4.11SFR Information (11) (1)

X: Undefined Note:

1. The blank areas are reserved and cannot be accessed by users.



Table 4.12SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			

2FFFh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Area Name	ame Symbol				
Address	Alea Naille	Syllibol	After Reset			
:		1				
FFDBh	Option Function Select Register 2	OFS2	(Note 1)			
:						
FFDFh	ID1		(Note 2)			
:			•			
FFE3h	ID2		(Note 2)			
:			•			
FFEBh	ID3		(Note 2)			
:			•			
FFEFh	ID4		(Note 2)			
:						
FFF3h	ID5		(Note 2)			
:			•			
FFF7h	ID6		(Note 2)			
:	·		· ·			
FFFBh	ID7		(Note 2)			
:			•			
FFFFh	Option Function Select Register	OFS	(Note 1)			

Notes:

 The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.

When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh. When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user. When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.



				Standard					
Symbol		P	arameter		Conditions	Min.	Тур.	Max.	Unit
Vcc/AVcc	Supply voltage					1.8	_	5.5	V
Vss/AVss	Supply voltage					_	0	_	V
Vih	Input "H" voltage	Other th	an CMOS ii	nput		0.8 Vcc	_	Vcc	V
		CMOS	Inputlevel	Input level selection:	$4.0 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	0.5 Vcc	_	Vcc	V
		input	switching	0.35 Vcc	$2.7~V \leq Vcc < 4.0~V$	0.55 Vcc	_	Vcc	V
					$1.8 \text{ V} \leq \text{Vcc} < 2.7 \text{ V}$	0.65 Vcc	_	Vcc	V
				Input level selection:	$4.0~V \leq Vcc \leq 5.5~V$	0.65 Vcc	_	Vcc	V
			0.5 Vcc	$2.7~\textrm{V} \leq \textrm{Vcc} < 4.0~\textrm{V}$	0.7 Vcc	_	Vcc	V	
					$1.8~V \leq Vcc < 2.7~V$	0.8 Vcc	_	Vcc	V
				Input level selection:	$4.0 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	0.85 Vcc	_	Vcc	V
				0.7 Vcc	$2.7~\text{V} \leq \text{Vcc} < 4.0~\text{V}$	0.85 Vcc	_	Vcc	V
					$1.8~V \leq Vcc < 2.7~V$	0.85 Vcc	_	Vcc	V
		Externa	l clock input	(XOUT)		1.2	_	Vcc	V
VIL	Input "L" voltage	Other th	an CMOS ii	nput		0	_	0.2 Vcc	V
		CMOS	Input level	Input level selection:	$4.0 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	0	_	0.2 Vcc	V
		input	switching	0.35 Vcc	$2.7 \text{ V} \le \text{Vcc} < 4.0 \text{ V}$	0		0.2 Vcc	V
			function		$1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$	0	_	0.2 Vcc	V
			(I/O port)	Input level selection:	$4.0 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$	0	_	0.4 Vcc	V
				0.5 Vcc	$2.7 \text{ V} \leq \text{Vcc} < 4.0 \text{ V}$	0	_	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	_	0.2 Vcc	V
				Input level selection:	4.0 V ≤ Vcc ≤ 5.5 V	0	_	0.55 Vcc	V
			0.7 Vcc	$2.7 \text{ V} \leq \text{Vcc} < 4.0 \text{ V}$	0	_	0.45 Vcc	V	
					1.8 V ≤ Vcc < 2.7 V	0	_	0.35 Vcc	V
		Externa	l clock input	(XOUT)		0		0.4	V
IOH(sum)			pins IOH(peak)		—		-160	mA	
IOH(sum)	Average sum out current	put "H"	Sum of all	pins IOH(avg)		_	_	-80	mA
IOH(peak)	Peak output "H" o	current	Drive capacity Low			_		-10	mA
			Drive capa	city High		_	_	-40	mA
IOH(avg)	Average output "I	-1"	Drive capa	city Low		_	_	-5	mA
	current		Drive capa	city High		_		-20	mA
IOL(sum)	Peak sum output current	"L"	Sum of all	pins IOL(peak)		—		160	mA
IOL(sum)	Average sum out current	put "L"	Sum of all	pins IOL(avg)		—		80	mA
OL(peak)	Peak output "L" c	urrent	Drive capa	city Low		—	—	10	mA
			Drive capa			—	—	40	mA
IOL(avg)	Average output "I	"	Drive capa			—	—	5	mA
	current		Drive capa	city High		—	—	20	mA
f(XIN)	XIN clock input or	scillation	frequency	-	$2.7 \text{ V} \leq \text{Vcc} \leq 5.5 \text{ V}$		—	20	MHz
					$1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$		—	5	MHz
f(XCIN)	XCIN clock input oscillation frequency			$1.8 \text{ V} \le \text{Vcc} \le 5.5 \text{ V}$	_	32.768	50	kHz	
fOCO40M	When used as the count source for timer RC, timer RD or timer RG $^{(3)}$		$2.7~V \leq Vcc \leq 5.5~V$	32	—	40	MHz		
fOCO-F	fOCO-F frequenc	Ÿ			2.7 V ≤ Vcc ≤ 5.5 V	_		20	MHz
					$1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$	_	_	5	MHz
_	System clock free	quency			$2.7 V \le Vcc \le 5.5 V$		_	20	MHz
	-,	1							MHz
			0.011		$1.8 V \le VCC \le 2.7 V$			5	
f(BCLK)	CPU clock freque	encv			$1.8 V \le Vcc < 2.7 V$ $2.7 V \le Vcc \le 5.5 V$	_	_	5 20	MHz

Table 5.2 Recommended Operating Conditions (1)

Notes:

1. Vcc = 1.8 to 5.5 V and T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.

2. The average output current indicates the average value of current measured during 100 ms.

3. fOCO40M can be used as the count source for timer RC, timer RD or timer RG in the range of Vcc = 2.7 to 5.5 V.





Figure 5.1 Ports P0 to P6, P8 Timing Measurement Circuit



Symbol	Parameter	Condition		Unit		
Symbol	Falameter	Condition	Min.	Тур.	Max.	Unit
Vdet0	Voltage detection level Vdet0_0 ⁽²⁾		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 ⁽²⁾		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
_	Voltage detection 0 circuit response time ⁽⁴⁾	At the falling of Vcc from 5.0 V to (Vdet0_0 - 0.1) V		6	150	μS
_	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V		1.5	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾			—	100	μS

Table 5.8	Voltage Detection 0 Circuit Electrical Characteristics

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version).

2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.

3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.9	Voltage Detection 1 Circuit Electrical Characteristics
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Symbol	Parameter	Condition		Unit		
Symbol	Falalletei	Condition	Min.	Тур.	Max.	Unit
Vdet1	Voltage detection level Vdet1_0 ⁽²⁾	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 ⁽²⁾	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 ⁽²⁾	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 ⁽²⁾	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 ⁽²⁾	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽²⁾	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 ⁽²⁾	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A ⁽²⁾	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B ⁽²⁾	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (2)	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E ⁽²⁾	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F ⁽²⁾	At the falling of Vcc	4.20	4.45	4.75	V
_	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	_	0.07	—	V
		Vdet1_6 to Vdet1_F selected	_	0.10	—	V
—	Voltage detection 1 circuit response time ⁽³⁾	At the falling of Vcc from 5.0 V to (Vdet1_0 - 0.1) V	_	60	150	μS
_	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	_	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		_	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version).

2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.

3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.

4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.





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Symbol		Parameter	Condition		St	tandard		Unit
Symbol		Falameter	Condition		Min.	Тур.	Max.	Offic
Vон	Output "H"	Other than XOUT	Drive capacity High $Vcc = 5 V$	Іон = -20 mA	Vcc - 2.0	_	Vcc	V
	voltage		Drive capacity Low $Vcc = 5 V$	Iон = -5 mA	Vcc - 2.0	_	Vcc	V
		XOUT	Vcc = 5 V	Іон = -200 μА	1.0	_	Vcc	V
Vol	Output "L"	Other than XOUT	Drive capacity High $Vcc = 5 V$	IoL = 20 mA	—	_	2.0	V
	voltage		Drive capacity Low $Vcc = 5 V$	lo∟ = 5 mA	—	_	2.0	V
		XOUT	Vcc = 5 V	IoL = 200 μA	—	_	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOC1, TRDIOD1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, TRGIOA, TRGIOB, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO RESET			0.1	1.2	_	V
Ін	Input "H" cu	irrent	VI = 5 V, Vcc = 5.0 V		—	_	5.0	μA
lı∟	Input "L" current		VI = 0 V, Vcc = 5.0 V		—	_	-5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5.0 V		25	50	100	kΩ
Rfxin	Feedback resistance	XIN			—	0.3	_	MΩ
Rfxcin	Feedback resistance	XCIN			—	8	—	MΩ
Vram	RAM hold v	roltage	During stop mode		1.8	_		V

Table 5.17	Electrical Characteristics (1) [4.2 V \leq Vcc \leq 5.5 V]
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Note:

4.2 V ≤ Vcc ≤ 5.5 V, T_{opr} = −20 to 85 °C (N version)/−40 to 85 °C (D version), and f(XIN) = 20 MHz, unless otherwise specified.



Table 5.18Electrical Characteristics (2) [3.3 V \leq Vcc \leq 5.5 V]
(Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.)

Deservator		Condition		Standard	k	1.1.4.14
Parameter		Condition	Min.	Тур.	Max.	Unit
Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode,	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	6.5	15	mA
output pins are open, other pins are Vss		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	5.3	12.5	mA
		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6		mA
		XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8		3.0		mA
		High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_		_	mA
		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.5		mA
	High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division		7.0	15	mA
		XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	3.0		mA
		XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRD = MSTTRC = 1	_	1		mA
	Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	90	400	μA
	Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1 VCA20 = 0	_	85	400	μΑ
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM	_	47	_	μΑ
	Wait mode	YiN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0. VCA20 = 1	_	15	100	μΑ
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	4	90	μΑ
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	3.5	_	μΑ
	Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	2.0	5.0	μΑ
		XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1		15		μA
	(Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open,	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss High-speed High-speed on-chip oscillator mode Low-speed Low-speed on-chip oscillator mode Low-speed Low-speed clock mode Low-speed Value Wait mode	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, other pins are vss XIN = 20 MHz (square wave) High-speed on-chip oscillator on = 125 kHz No division XIN = 16 MHz (square wave) High-speed on-chip oscillator on = 125 kHz No division XIN = 16 MHz (square wave) High-speed on-chip oscillator on = 125 kHz No division XIN = 20 MHz (square wave) High-speed on-chip oscillator on = 125 kHz No division XIN = 20 MHz (square wave) High-speed on-chip oscillator on = 125 kHz No division XIN = 10 MHz (square wave) High-speed on-chip oscillator on = 125 kHz Divide-by-3 XIN = 10 MHz (square wave) High-speed on-chip oscillator on = 125 kHz Divide-by-3 XIN = 10 MHz (square wave) High-speed on-chip oscillator on = 125 kHz Divide-by-3 XIN = 10 MHz (square wave) High-speed on-chip oscillator on = 125 kHz Divide-by-3 XIN = 10 MHz (square wave) High-speed on-chip oscillator on = 125 kHz Divide-by-3 XIN = 10 MHz (square wave) High-speed on-chip oscillator on = 125 kHz Divide-by-4 XIN clock off High-speed on-chip oscillator on = 125 kHz Divide-by-8 XIN clock off High-speed on-chip oscillator on = 125 kHz Divide-by-76 XIN clock off High-speed on-chip oscillator on = 125 kHz Divide-by-76 XIN clock off High-speed on-chip oscillator on = 125 kHz Divide-by-76 XIN clock off High-speed on-chip oscillator on = 125 kHz Divide-by-76 XIN clock off High-speed on-chip oscillator on = 125 kHz Divide-by-76 XIN clock off High-speed on-chip oscillator on = 125 kHz Divide-by-76 XIN clock off High-speed on-chip oscillator on = 125 kHz Divide-by-76	Parameter Condition Min. Power supply current (Vcc a 3.3 to 5.5 V) High-speed lock mode, output prins are open, other pins are Vss High-speed No division	Parameter Condition Min. Typ. Power supply current High-speed XIN = 10 MHz (square wave) — 6.5 Single-chip mode, output pins are vss XIN = 10 MHz (square wave) — 5.3 XIN = 10 MHz (square wave) — 5.3 XIN = 10 MHz (square wave) — 3.6 XIN = 10 MHz (square wave) — 3.6 XIN = 10 MHz (square wave) — 3.0 XIN = 10 MHz (square wave) — 1.5 Wide by-6 XIN = 10 MHz (square wave) — 1.5 Wide by-9 XIN = 10 MHz (square wave) — 1.5 Wide by-9 XIN = 10 MHz (square wave) — 1.5 Wide by-9 XIN stock off — 3.0 Uowspeed on-chip oscillator on 125 Htz — 1.5 Wide dock off <t< td=""><td>Power supply current High-speed (lock mode) XIN = 20 MHz (square wave) — 6.5 15 Single-chip mode, output pins are open, other pins are Vss XIN = 20 MHz (square wave) — 5.3 12.5 XIN = 16 MHz (square wave) — 5.3 12.5 XIN = 16 MHz (square wave) — 5.3 12.5 XIN = 20 MHz (square wave) — 5.3 12.5 XIN = 16 MHz (square wave) — 3.6 — XIN = 20 MHz (square wave) — 3.6 — XIN = 20 MHz (square wave) — 3.0 — XIN = 16 MHz (square wave) — 1.5 — 1.5 — Visite State of on-thip scalilator on = 125 kHz — 1.5 — 1.5 — Visite State of on-thip scalilator on = 125 kHz — 1.5 — 1.5 — Visite State of on-thip scalilator on = 125 kHz — 1.5 — 1.5 — Visite State of on-thip scalilator on = 125 kHz — 1.5 — 1.5 —</td></t<>	Power supply current High-speed (lock mode) XIN = 20 MHz (square wave) — 6.5 15 Single-chip mode, output pins are open, other pins are Vss XIN = 20 MHz (square wave) — 5.3 12.5 XIN = 16 MHz (square wave) — 5.3 12.5 XIN = 16 MHz (square wave) — 5.3 12.5 XIN = 20 MHz (square wave) — 5.3 12.5 XIN = 16 MHz (square wave) — 3.6 — XIN = 20 MHz (square wave) — 3.6 — XIN = 20 MHz (square wave) — 3.0 — XIN = 16 MHz (square wave) — 1.5 — 1.5 — Visite State of on-thip scalilator on = 125 kHz — 1.5 — 1.5 — Visite State of on-thip scalilator on = 125 kHz — 1.5 — 1.5 — Visite State of on-thip scalilator on = 125 kHz — 1.5 — 1.5 — Visite State of on-thip scalilator on = 125 kHz — 1.5 — 1.5 —



Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Electronics website.





REVISION HISTORY	R8C/36C Group Datasheet
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Rev.	Date		Description
Rev.	Dale	Page	Summary
0.01	Oct 30, 2009	_	First Edition issued
1.00	Nov 02, 2010	All pages	"Preliminary", "Under development" deleted
		4	Table 1.3 revised
		28 to 54	"5. Electrical Characteristics" added
1.10	Nov 02, 2010		TN-R8C-A015A/E reflected
		3	Table 1.2 "Timer RG" and "Package" revised
		4 and 5	Tables 1.3 and 1.4 revised
		6	Figure 1.1 revised
		8	Figure 1.3 "PTQP0064LB-A" added
		17	Figure 3.1 "Part Number" revised
		33	Table 5.3 "tCONV", "tSAMP" revised
		47	Table 5.21 revised
		51	Table 5.28 revised
		55	Table 5.35 revised
		59	Package (PTQP0064LB-A) added

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