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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136ccdfa-x4

Table 1.2 Specifications for R8C/36C Group (2)

Item	Function	Specification
Timer	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 (with 2 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, UART1	Clock synchronous serial I/O/UART × 2 channel
	UART2	Clock synchronous serial I/O, UART, I ² C mode (I ² C bus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 (shared with I ² C bus)
I ² C bus		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function, with sweep mode
D/A Converter		8-bit resolution × 2 circuits
Comparator B		2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)
Current consumption		Typ. 7.0 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 4.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 2.0 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		−20 to 85°C (N version) −40 to 85°C (D version) ⁽¹⁾
Package		64-pin LQFP • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin TQFP • Package code: PTQP0064LB-A

Note:

1. Specify the D version if D version functions are to be used.

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

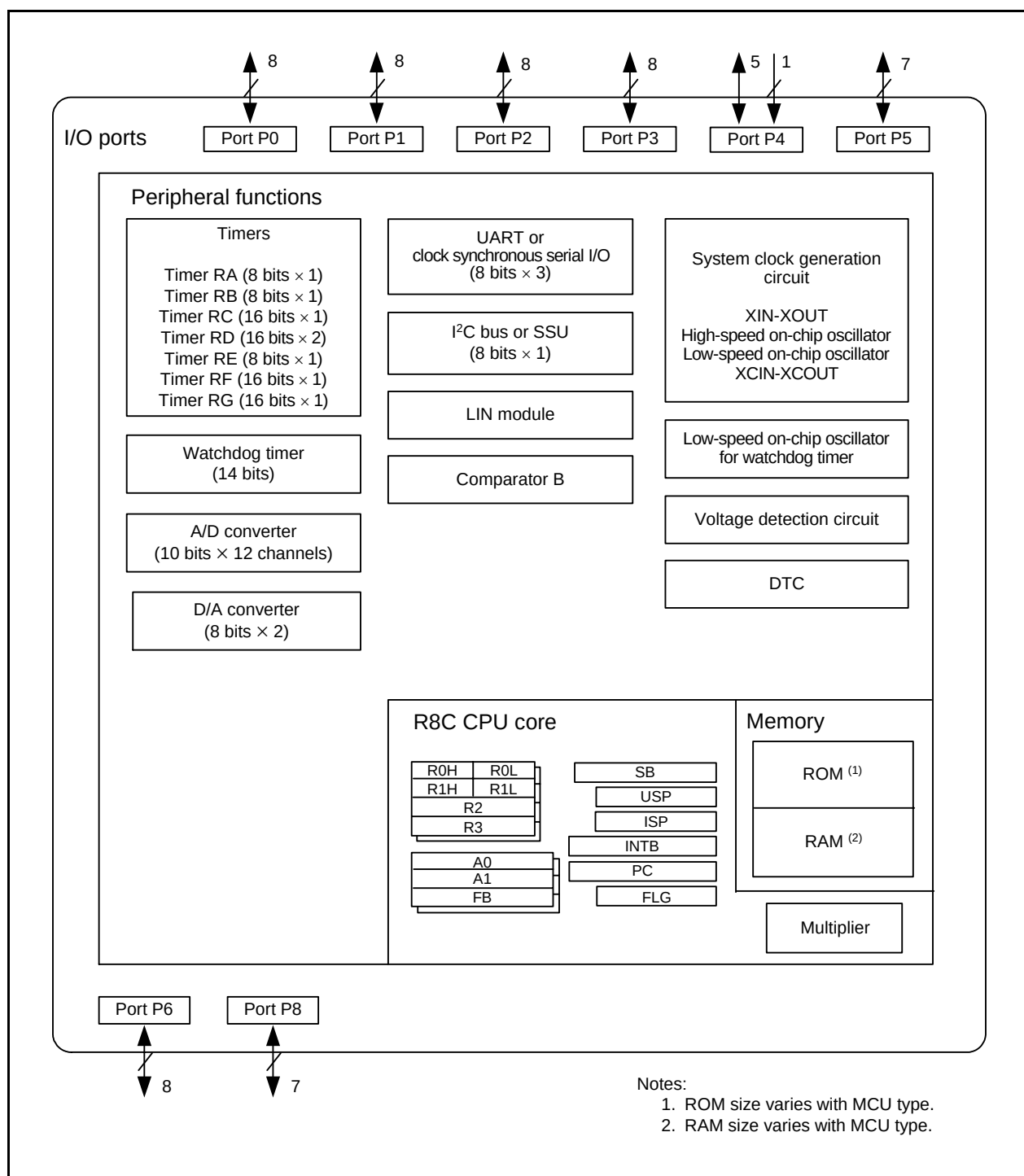


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.5 and 1.6 outline the Pin Name Information by Pin Number.

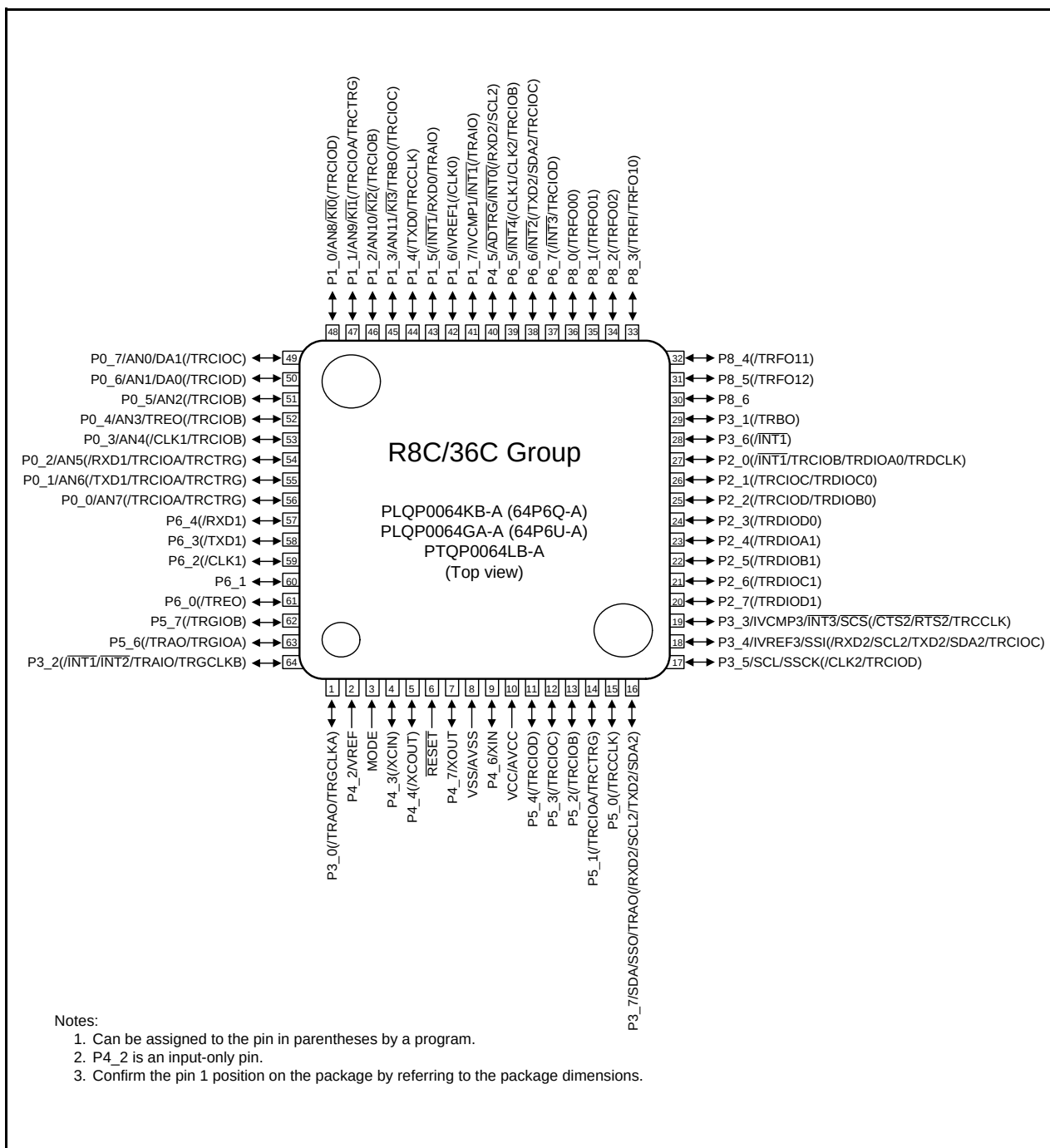


Figure 1.3 Pin Assignment (Top View)

Table 1.8 Pin Functions (2)

Item	Pin Name	I/O Type	Description
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter.
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter.
	$\overline{\text{ADTRG}}$	I	AD external trigger input pin.
D/A converter	DA0, DA1	O	D/A converter output pins.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Input port	P4_2	I	Input-only port.

I: Input O: Output I/O: Input and output

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

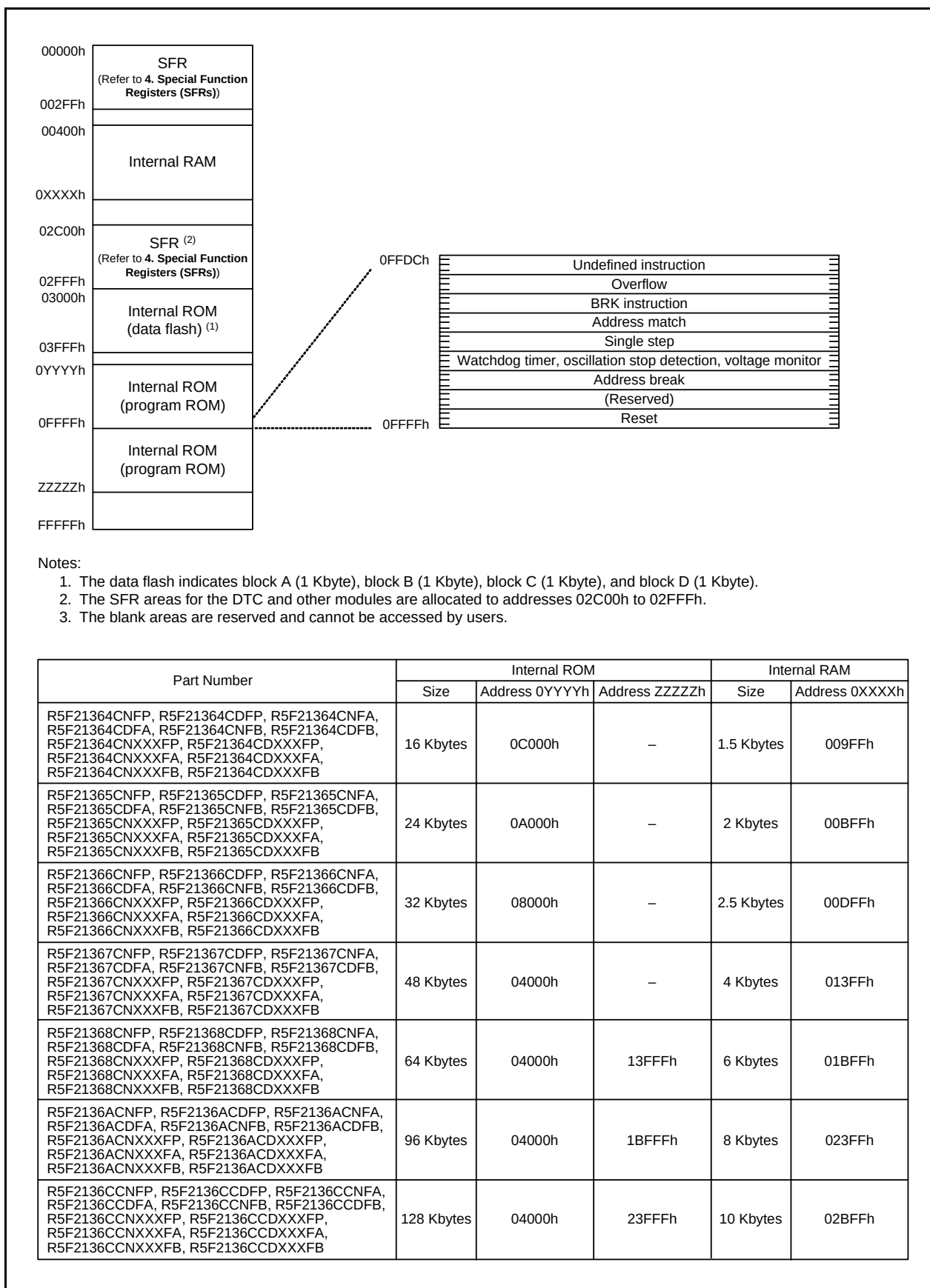


Figure 3.1 Memory Map of R8C/36C Group

Table 4.4 SFR Information (4) ⁽¹⁾

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h			XXh
00C3h	A/D Register 1	AD1	000000XXb
00C4h			XXh
00C5h			000000XXb
00C6h	A/D Register 2	AD2	XXh
00C7h			000000XXb
00C8h			XXh
00C9h	A/D Register 3	AD3	000000XXb
00CAh			XXh
00CBh			000000XXb
00CCh	A/D Register 4	AD4	XXh
00CDh			000000XXb
00CEh			XXh
00CFh	A/D Register 5	AD5	000000XXb
00D0h			XXh
00D1h			000000XXb
00D2h	A/D Register 6	AD6	XXh
00D3h			000000XXb
00D4h			XXh
00D5h	A/D Register 7	AD7	000000XXb
00D6h			XXh
00D7h			000000XXb
00D8h	A/D Mode Register	ADMOD	00h
00D9h			11000000b
00DAh			00h
00DBh	A/D Input Select Register	ADINSEL	00h
00DCh			00h
00DDh			00h
00DEh	A/D Control Register 0	ADCON0	00h
00DFh			00h
00E0h			00h
00E1h	A/D Control Register 1	ADCON1	00h
00E2h			00h
00E3h			00h
00E4h	D/A0 Register	DA0	00h
00E5h			00h
00E6h			00h
00E7h	D/A1 Register	DA1	00h
00E8h			00h
00E9h			00h
00EAh	D/A Control Register	DACON	00h
00EBh			00h
00ECh			00h
00EDh	Port P0 Register	P0	XXh
00EEh			XXh
00EFh			00h
00F0h	Port P1 Register	P1	00h
00F1h			00h
00F2h			00h
00F3h	Port P0 Direction Register	PD0	00h
00F4h			00h
00F5h			00h
00F6h	Port P1 Direction Register	PD1	00h
00F7h			00h
00F8h			00h
00F9h	Port P2 Register	P2	XXh
00FAh			XXh
00FBh			00h
00FCh	Port P2 Direction Register	PD2	00h
00FDh			00h
00FEh			00h
00FFh	Port P3 Register	P3	XXh
			XXh
			00h
	Port P3 Direction Register	PD3	00h
			00h
			00h
	Port P4 Register	P4	XXh
			XXh
			00h
	Port P4 Direction Register	PD4	00h
			00h
			00h
	Port P5 Register	P5	XXh
			XXh
			00h
	Port P5 Direction Register	PD5	00h
			00h
			00h
	Port P6 Register	P6	XXh
			XXh
			00h
	Port P6 Direction Register	PD6	00h
			00h
			00h
	Port P8 Register	P8	XXh
			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIOA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIOA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h	Timer RG Mode Register	TRGMR	01000000b
0171h	Timer RG Count Control Register	TRGCNTC	00h
0172h	Timer RG Control Register	TRGCR	10000000b
0173h	Timer RG Interrupt Enable Register	TRGIER	11110000b
0174h	Timer RG Status Register	TRGSR	11100000b
0175h	Timer RG I/O Control Register	TRGIOR	00h
0176h	Timer RG Counter	TRG	00h
0177h			00h
0178h	Timer RG General Register A	TRGGRA	FFh
0179h			FFh
017Ah	Timer RG General Register B	TRGGRB	FFh
017Bh			FFh
017Ch	Timer RG General Register C	TRGGRC	FFh
017Dh			FFh
017Eh	Timer RG General Register D	TRGGRD	FFh
017Fh			FFh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h	Pull-Up Control Register 2	PUR2	00h
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h	Port P2 Drive Capacity Control Register	P2DRR	00h
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h	Drive Capacity Control Register 2	DRR2	00h
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) ⁽¹⁾

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACH			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) ⁽¹⁾

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V _{CC} /AV _{CC}	Supply voltage					1.8	—	5.5	V
V _{SS} /AV _{SS}	Supply voltage					—	0	—	V
V _{IH}	Input “H” voltage	Other than CMOS input				0.8 V _{CC}	—	V _{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.5 V _{CC}	—	V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0.55 V _{CC}	—	V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0.65 V _{CC}	—	V _{CC}	V
			Input level selection: 0.5 V _{CC}		4.0 V ≤ V _{CC} ≤ 5.5 V	0.65 V _{CC}	—	V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0.7 V _{CC}	—	V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0.8 V _{CC}	—	V _{CC}	V
			Input level selection: 0.7 V _{CC}		4.0 V ≤ V _{CC} ≤ 5.5 V	0.85 V _{CC}	—	V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0.85 V _{CC}	—	V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0.85 V _{CC}	—	V _{CC}	V
	External clock input (XOUT)				1.2	—	V _{CC}	V	
V _{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 V _{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.2 V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0	—	0.2 V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0	—	0.2 V _{CC}	V
			Input level selection: 0.5 V _{CC}		4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.4 V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0	—	0.3 V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0	—	0.2 V _{CC}	V
			Input level selection: 0.7 V _{CC}		4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.55 V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0	—	0.45 V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0	—	0.35 V _{CC}	V
	External clock input (XOUT)				0	—	0.4	V	
I _{OH} (sum)	Peak sum output “H” current	Sum of all pins I _{OH} (peak)		—	—	−160	mA		
I _{OH} (sum)	Average sum output “H” current	Sum of all pins I _{OH} (avg)		—	—	−80	mA		
I _{OH} (peak)	Peak output “H” current	Drive capacity Low		—	—	−10	mA		
		Drive capacity High		—	—	−40	mA		
I _{OH} (avg)	Average output “H” current	Drive capacity Low		—	—	−5	mA		
		Drive capacity High		—	—	−20	mA		
I _{OL} (sum)	Peak sum output “L” current	Sum of all pins I _{OL} (peak)		—	—	160	mA		
I _{OL} (sum)	Average sum output “L” current	Sum of all pins I _{OL} (avg)		—	—	80	mA		
I _{OL} (peak)	Peak output “L” current	Drive capacity Low		—	—	10	mA		
		Drive capacity High		—	—	40	mA		
I _{OL} (avg)	Average output “L” current	Drive capacity Low		—	—	5	mA		
		Drive capacity High		—	—	20	mA		
f _(XIN)	XIN clock input oscillation frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
f _(XCIN)	XCIN clock input oscillation frequency			1.8 V ≤ V _{CC} ≤ 5.5 V	—	32.768	50	kHz	
f _{OCO40M}	When used as the count source for timer RC, timer RD or timer RG ⁽³⁾			2.7 V ≤ V _{CC} ≤ 5.5 V	32	—	40	MHz	
f _{OCO-F}	f _{OCO-F} frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
—	System clock frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
f _(BCLK)	CPU clock frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	

Notes:

- V_{CC} = 1.8 to 5.5 V and T_{opr} = −20 to 85 °C (N version)/−40 to 85 °C (D version), unless otherwise specified.
- The average output current indicates the average value of current measured during 100 ms.
- f_{OCO40M} can be used as the count source for timer RC, timer RD or timer RG in the range of V_{CC} = 2.7 to 5.5 V.

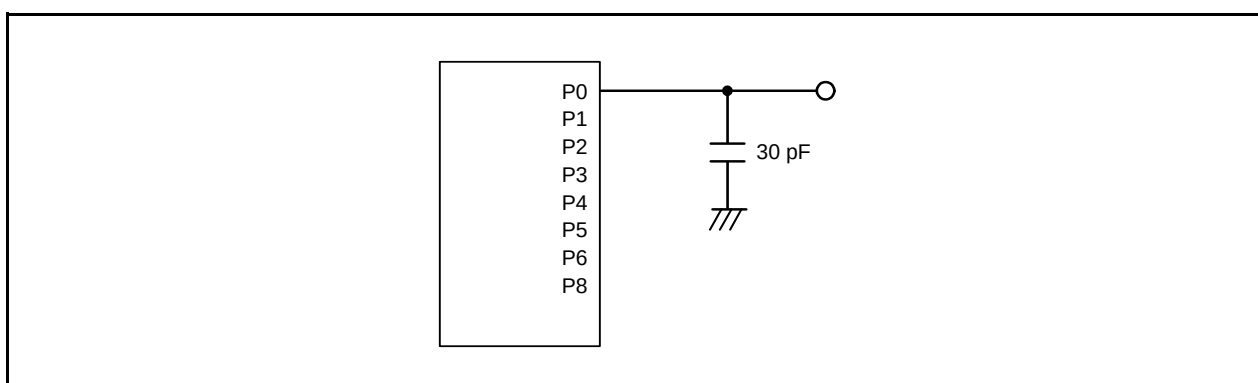


Figure 5.1 Ports P0 to P6, P8 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVCC		—	—	10	Bit
—	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±3	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	20	MHz
			3.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	16	MHz
			2.7 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	10	MHz
			2.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5.0 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				2.2	—	AVCC	V
VIA	Analog input voltage (3)				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_{opr} = -20$ to $85\text{ }^{\circ}\text{C}$ (N version)/ -40 to $85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.6 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

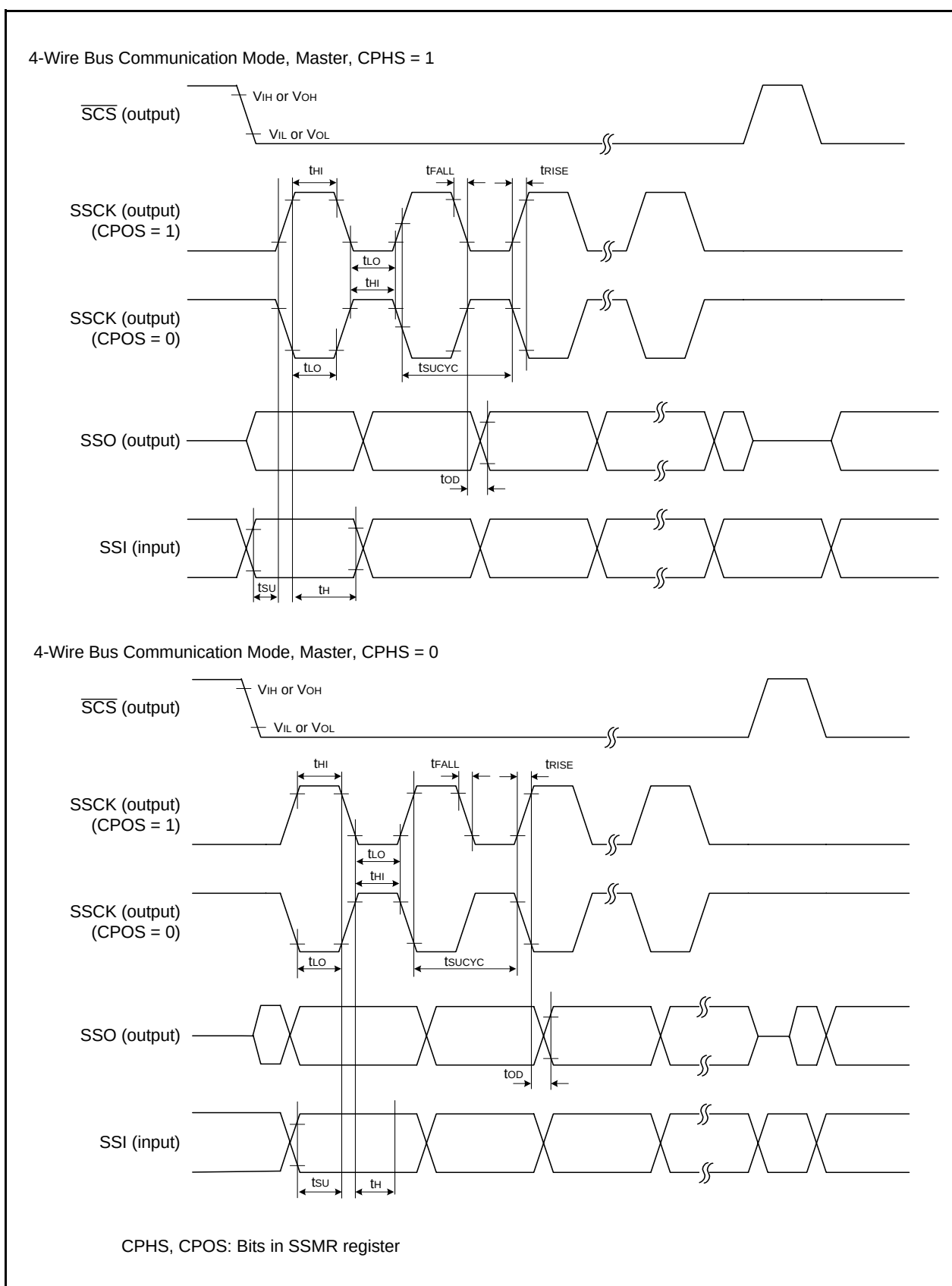
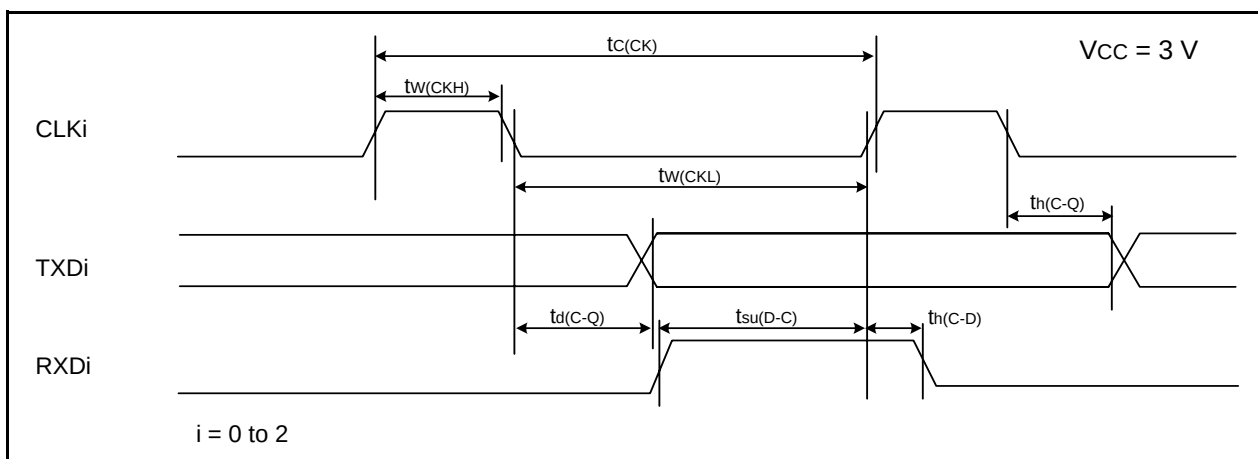


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

Table 5.29 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.16 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.30 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 4$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	380 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	380 (2)	—	ns

Notes:

- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

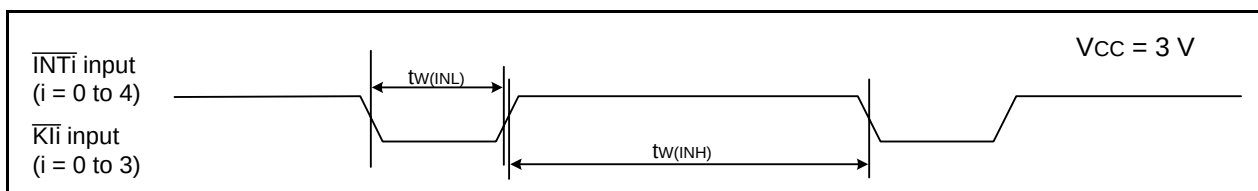
**Figure 5.17 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 3 V**

Table 5.31 Electrical Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]

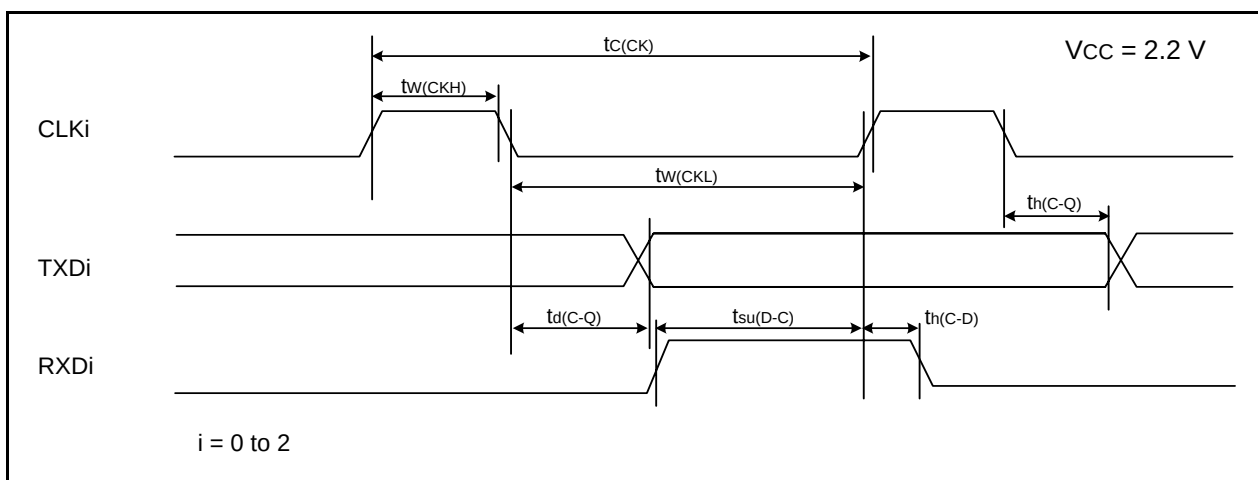
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	NT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, TRGIOA, TRGIOB, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.05	0.20	—	V
		RESET			0.05	0.20	—	V
I _{IH}	Input "H" current		V _I = 2.2 V, V _{CC} = 2.2 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 2.2 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 2.2 V		70	140	300	k Ω
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$, T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), and f(XIN) = 5 MHz, unless otherwise specified.

Table 5.36 Serial Interface

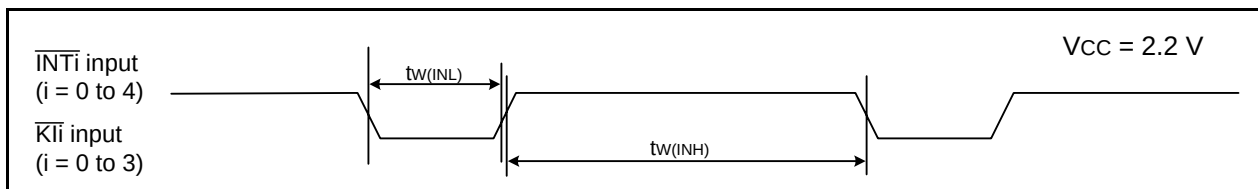
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.21 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.37 External Interrupt $\overline{INTi}$ ($i = 0 \text{ to } 4$) Input, Key Input Interrupt $\overline{Kli}$ ($i = 0 \text{ to } 3$)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	1000 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	1000 (2)	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

**Figure 5.22 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 2.2 V**

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