



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10К х 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2136ccdfp-30

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 1.1 Part Number, Memory Size, and Package of R8C/36C Group



1.3 Block Diagram

Figure 1.2 shows a Block Diagram.





1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.5 and 1.6 outline the Pin Name Information by Pin Number.





Item	Pin Name	I/O Type	Description
SSU	SSI	I/O	Data I/O pin.
	SCS	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter.
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter.
	ADTRG	I	AD external trigger input pin.
D/A converter	DA0, DA1	0	D/A converter output pins.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Input port	P4_2	I	Input-only port.
I: Input O: Out	put I/O: Input an	d output	

Table 1.8Pin Functions (2)



2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.



4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

	()		
Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	0010000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTER	0XXXXXXX (2)
000Ch	Oscillation Ston Detection Register		00000000000000000000000000000000000000
0000h	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Pogister	WDTS	XXh
000Eh	Watchdog Timer Control Pogister	WDTS	001111116
0010h		WDIC	001111110
00101			
0012h			
001211			
00131			
001411	Lligh Chand On Chin Oppillator Control Degister 7		When objection
00150		FRAZ	when shipping
00101			
00171			
00101			
00190			
001AI			
00160	Count Course Distantion Made Degister	CODD	00h
001011		COFK	10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h ⁽⁴⁾
			0010000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h		10120	
0038h	Voltage Monitor 0 Circuit Control Register	V/W/0C	1100X010b (4)
000011		******	
00001		110010	
0039h	voitage Monitor 1 Circuit Control Register	VW1C	10001010b

Table 4.1SFR Information (1) (1)

X: Undefined

Notes:

- 1. The blank areas are reserved and cannot be accessed by users.
- 2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.

3. The CSPROINI bit in the OFS register is set to 0.

4. The LVDAS bit in the OFS register is set to 1.

5. The LVDAS bit in the OFS register is set to 0.



Figure 5.1 Ports P0 to P6, P8 Timing Measurement Circuit



Symbol	Paramotor		Cond	itions	Standard		Linit	
Symbol	Faiaiiielei		Cond	Conditions		Тур.	Max.	Offic
—	Resolution		Vref = AVCC		_		10	Bit
_	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	_	—	±3	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	_	_	±5	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input		—	±5	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input		—	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	_	—	±2	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input		—	±2	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input		—	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	_	—	±2	LSB
φAD	A/D conversion clock		$4.0 \text{ V} \leq \text{Vref} = \text{AVCC} \leq$	≤ 5.5 V ⁽²⁾	2		20	MHz
			$3.2 \text{ V} \leq \text{Vref} = \text{AVCC} \leq$	≤ 5.5 V ⁽²⁾	2		16	MHz
			$2.7 \text{ V} \leq \text{Vref} = \text{AVcc} \leq$	≤ 5.5 V ⁽²⁾	2		10	MHz
			$2.2 \text{ V} \leq \text{Vref} = \text{AVcc} \leq$	≤ 5.5 V ⁽²⁾	2		5	MHz
—	Tolerance level impedance)				3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, c	φAD = 20 MHz	2.2	—		μS
		8-bit mode	Vref = AVCC = 5.0 V, c	φAD = 20 MHz	2.2	—	_	μS
t SAMP	Sampling time		$\phi AD = 20 MHz$		0.8		—	μS
IVref	Vref current		Vcc = 5.0 V, XIN = f1	I = φAD = 20 MHz	_	45	—	μA
Vref	Reference voltage				2.2	—	AVcc	V
Via	Analog input voltage (3)				0	—	Vref	V
OCVREF	On-chip reference voltage		$2 \text{ MHz} \le \phi \text{AD} \le 4 \text{ MHz}$	lz	1.19	1.34	1.49	V

Table 5.3 A/D Converter Characteristics

Notes:

1. Vcc/AVcc = Vref = 2.2 to 5.5 V, Vss = 0 V, and Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.

2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-currentconsumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.

3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.



Symbol	Paramotor	Conditions		Lloit		
Symbol	Falameter	Conditions	Min. Typ. Max.		Unit	
—	Program/erase endurance (2)		1,000 ⁽³⁾	—	—	times
—	Byte program time		_	80	500	μs
—	Block erase time		_	0.3	—	s
td(SR-SUS)	Time delay from suspend request until suspend		—		5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	_	—	μS
—	Time from suspend until erase restart		_	_	30 + CPU clock × 1 cycle	μS
td(CMDRST -READY)	Time from when command is forcibly stopped until reading is enabled		—		30 + CPU clock × 1 cycle	μS
—	Program, erase voltage		2.7	_	5.5	V
—	Read voltage		1.8	-	5.5	V
_	Program, erase temperature		0	_	60	°C
—	Data hold time (7)	Ambient temperature = 55 °C	20	_		year

Table 5.6 Flash Memory (Program ROM) Electrical Characteristics

Notes: 1. Vcc = 2.7 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.

2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)

4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

7. The data hold time includes time that the power supply is off or the clock is not supplied.



Symbol	Paramotor	Conditions		Llnit		
Symbol	Falameter	Conditions	Min.	Тур. Мах.		Unit
—	Program/erase endurance (2)		10,000 (3)	—	—	times
	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	μS
—	Byte program time (program/erase endurance > 1,000 times)		_	300	1500	μS
—	Block erase time (program/erase endurance ≤ 1,000 times)		_	0.2	1	S
	Block erase time (program/erase endurance > 1,000 times)		_	0.3	1	S
td(SR-SUS)	Time delay from suspend request until suspend		_		5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0		—	μS
	Time from suspend until erase restart		—	_	30 + CPU clock × 1 cycle	μS
td(CMDRST -READY)	Time from when command is forcibly stopped until reading is enabled		_		30 + CPU clock × 1 cycle	μS
—	Program, erase voltage		2.7	_	5.5	V
—	Read voltage		1.8	_	5.5	V
_	Program, erase temperature		-20 (7)	—	85	°C
—	Data hold time ⁽⁸⁾	Ambient temperature = 55 °C	20		_	year

Table 5.7 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Notes:

1. Vcc = 2.7 to 5.5 V and Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.

2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)

4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

^{8.} The data hold time includes time that the power supply is off or the clock is not supplied.





^{7. -40 °}C for D version.

Symbol	Parameter	Condition		Linit		
Symbol	Falanetei	Condition	Min.	Тур.	Max.	Offic
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
-	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		_	0.10	_	V
-	Voltage detection 2 circuit response time (2)	At the falling of Vcc from 5.0 V to (Vdet2_0 - 0.1) V	_	20	150	μS
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts $^{\rm (3)}$		_	_	100	μS

Table 5.10 Voltage Detection 2 Circuit Electrical Characteristics

Notes:

- 1. The measurement condition is Vcc = 1.8 to 5.5 V and T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version).
- 2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
- 3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11 Power-on Reset Circuit ⁽²⁾

Symbol	Parameter	Condition		Lloit		
			Min.	Тур.	Max.	Unit
trth	External power Vcc rise gradient	(1)	0	—	50,000	mV/msec

Notes:

- 1. The measurement condition is $T_{opr} = -20$ to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.
- 2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain tw(por) for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics



Symbol	Parameter	Condition	Standard			Linit
Symbol	Falanielei	Condition	Min.	Тур.	Max.	Offic
_	High-speed on-chip oscillator frequency after reset	Vcc = 1.8 V to 5.5 V −20 °C ≤ T _{opr} ≤ 85 °C	38.4	40	41.6	MHz
	Vcc = 1.8 V to 5.5 V -40 °C ≤ T _{opr} ≤ 85 °C	38.0	40	42.0	MHz	
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2)High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the	Vcc = 1.8 V to 5.5 V -20 °C \leq Topr \leq 85 °C	35.389	36.864	38.338	MHz
		Vcc = 1.8 V to 5.5 V -40 °C ≤ Topr ≤ 85 °C	35.020	36.864	38.707	MHz
		Vcc = 1.8 V to 5.5 V −20 °C ≤ Topr ≤ 85 °C	30.72	32	33.28	MHz
FRA1 register and the FRA7 register correction value into the FRA3 register	Vcc = 1.8 V to 5.5 V -40 °C ≤ T _{opr} ≤ 85 °C	30.40	32	33.60	MHz	
—	Oscillation stability time	VCC = 5.0 V, Topr = 25 $^{\circ}$ C	—	0.5	3	ms
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25 °C	—	400	_	μA

Table 5.12	High-speed On-Chip Oscillator Circuit Electrical Characteristics

Notes:

1. Vcc = 1.8 to 5.5 V and Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.

2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.13 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition		Lloit		
Symbol	Falanetei	ter Condition $\begin{tabular}{ c c c c c } \hline Standard \\ \hline Min. & Typ. & Max. \\ \hline requency & 60 & 125 & 250 \\ \hline Vcc = 5.0 \ V, \ T_{opr} = 25 \ ^{\circ}C & & 30 & 100 \\ \hline cillation & Vcc = 5.0 \ V, \ T_{opr} = 25 \ ^{\circ}C & & 2 & \\ \hline \end{array}$	Onit			
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	VCC = 5.0 V, Topr = 25 °C	_	30	100	μS
—	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25 °C	—	2	_	μΑ

Note:

1. Vcc = 1.8 to 5.5 V and Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.

Table 5.14 Power Supply Circuit Timing Characteristics

Symbol	Paramator	Condition		Lloit		
	Falameter	Condition	Min.	Тур.	Max.	Onit
td(P-R)	Time for internal power supply stabilization during		—		2,000	μS
	power-on ⁽²⁾					

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and T_opr = 25 $^\circ\text{C}.$

2. Waiting time until the internal power supply generation circuit stabilizes during power-on.





RENESAS

Table 5.25Electrical Characteristics (4) $[2.7 V \le VCC \le 3.3 V]$
(Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard	4	Llnit
Cymbol	T arameter		Condition	Min.	Тур.	Max.	Onit
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode,	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	3.5	10	mA
	other pins are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	3.0	_	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	4.0	_	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	_	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRD = MSTTRC = 1	—	1		mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	390	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	_	80	400	μΑ
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	_	40		μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	3.5	_	μA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	2.0	5.0	μĀ
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	_	μA



Timing requirements (Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V, Topr = 25 °C)

Table 5.26 External Clock Input (XOUT, XCIN)

Symbol	Daramatar	Stan	ndard	Llpit
	Falantelei	Min.	Max.	Unit
tc(XOUT)	XOUT input cycle time	50	—	ns
twh(xout)	XOUT input "H" width	24	—	ns
twl(xout)	XOUT input "L" width	24	—	ns
tc(XCIN)	XCIN input cycle time	14	—	μS
twh(xcin)	XCIN input "H" width	7	—	μS
twl(xcin)	XCIN input "L" width	7	—	μS



Figure 5.13 External Clock Input Timing Diagram when VCC = 3 V

Table 5.27 TRAIO Input

Symbol	Daramatar	Stan	dard	Unit
Symbol		Min.	Max.	Unit
tc(TRAIO)	TRAIO input cycle time	300	—	ns
twh(traio)	TRAIO input "H" width	120	—	ns
twl(traio)	TRAIO input "L" width	120	—	ns



Figure 5.14 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.28 TRFI Input

Symbol	Parameter	Stan	dard	Unit ns ns
	Falameter	Min.	Max.	
tc(TRFI)	TRFI input cycle time	1200 ⁽¹⁾	_	ns
twh(trfi)	TRFI input "H" width	600 (2)	_	ns
twl(trfi)	TRFI input "L" width	600 (2)	_	ns

Notes:

1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency \times 3) or above.

2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

	← tc(TRFI)	Vcc = 3 V
TRFI input		

Figure 5.15 TRFI Input Timing Diagram when Vcc = 3 V



Table 5.29 Seria	I Interface
------------------	-------------

Symbol	Decomptor	Stan	dard	Linit
	Falameter	Min. Max.	Unit	
tc(CK)	CLKi input cycle time	300	—	ns
tw(CKH)	CLKi input "H" width	150	—	ns
tW(CKL)	CLKi Input "L" width	150	—	ns
td(C-Q)	TXDi output delay time	—	80	ns
th(C-Q)	TXDi hold time	0	—	ns
tsu(D-C)	RXDi input setup time	70	—	ns
th(C-D)	RXDi input hold time	90	_	ns

i = 0 to 2



Figure 5.16 Serial Interface Timing Diagram when Vcc = 3 V

External Interrupt \overline{INTi} (i = 0 to 4) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3) **Table 5.30**

Symbol	Parameter	Stan	dard	Lloit
Symbol		Min.	Max.	Unit
tw(INH)	INTi input "H" width, Kli input "H" width	380 (1)		ns
tw(INL)	$\overline{\text{INTi}}$ input "L" width, $\overline{\text{Kli}}$ input "L" width		_	ns

Notes:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.



Input Timing Diagram for External Interrupt INTi and Key Input Interrupt Kli Figure 5.17 when Vcc = 3 V



Table 5.32Electrical Characteristics (6) [1.8 V \leq Vcc < 2.7 V]
(Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard		d	Unit
Symbol	i arameter		Condition	Min.	Тур.	Max.	Onit
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	2.2	_	mA
	other pins are Vss		XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	0.8	_	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	2.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.7	_	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRD = MSTTRC = 1	—	1	_	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	300	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	_	80	350	μΑ
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0		40		μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	15	90	μΑ
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	4	80	μΑ
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	3.5	_	μА
		Stop mode	XIN clock off, $T_{opr} = 25 \text{ °C}$ High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0		2.0	5	μA
			XIN clock off, Topr = $85 ^{\circ}$ C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0		15	—	μΑ



Symbol	Deromotor	Stan	Standard Min. Max.	Linit
Symbol	Farameter	Min.		Unit
tc(CK)	CLKi input cycle time	800	_	ns
tw(CKH)	CLKi input "H" width	400	_	ns
tw(CKL)	CLKi input "L" width	400	_	ns
td(C-Q)	TXDi output delay time	_	200	ns
th(C-Q)	TXDi hold time	0	_	ns
tsu(D-C)	RXDi input setup time	150	_	ns
th(C-D)	RXDi input hold time	90	_	ns

i = 0 to 2



Serial Interface Timing Diagram when Vcc = 2.2 V Figure 5.21

External Interrupt \overline{INTi} (i = 0 to 4) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3) **Table 5.37**

Symbol Parameter	Parameter	Stan	dard	Lloit
	Falameter	Min.	Max.	Offic
tw(INH)	INTi input "H" width, Kli input "H" width	1000 (1)	-	ns
tw(INL)	INTi input "L" width, Kli input "L" width	1000 (2)	_	ns

Notes:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



Input Timing Diagram for External Interrupt INTi and Key Input Interrupt Kli Figure 5.22 when Vcc = 2.2 V



General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
 - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do
 not access these addresses; the correct operation of LSI is not guaranteed if they are
 accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.