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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2238bfa13iv

(5) Pin Arrangement of H8S/2227 Group

Figures 1.15 and 1.16 show the pin arrangement of the H8S/2227 Group.

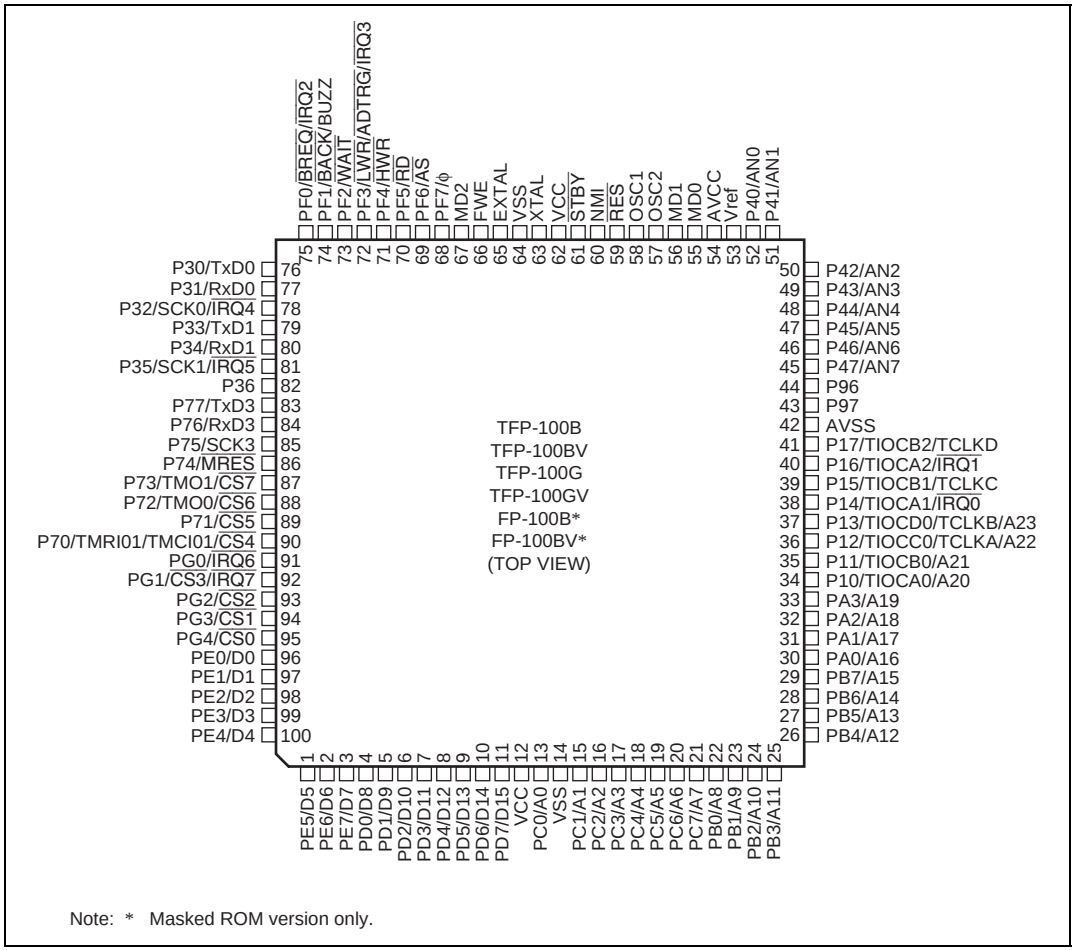


Figure 1.15 Pin Arrangement of H8S/2227 Group
(TFP-100B, TFP-100BV, TFP-100G, TFP-100GV, FP-100B*, FP-100BV*: Top View)

Pin No.		Pin Name				
TFP-100B FP-100B	FP-100A	Mode 4	Mode 5	Mode 6	Mode 7	Flash Memory Programmable Mode*
78	81	P32/SCK0/ SDA1/$\overline{\text{IRQ4}}$	P32/SCK0/ SDA1/$\overline{\text{IRQ4}}$	P32/SCK0/ SDA1/$\overline{\text{IRQ4}}$	P32/SCK0/ SDA1/$\overline{\text{IRQ4}}$	NC
79	82	P33/TxD1/ SCL1	P33/TxD1/ SCL1	P33/TxD1/ SCL1	P33/TxD1/ SCL1	NC
80	83	P34/RxD1/ SDA0	P34/RxD1/ SDA0	P34/RxD1/ SDA0	P34/RxD1/ SDA0	NC
81	84	P35/SCK1/ SCL0/$\overline{\text{IRQ5}}$	P35/SCK1/ SCL0/$\overline{\text{IRQ5}}$	P35/SCK1/ SCL0/$\overline{\text{IRQ5}}$	P35/SCK1/ SCL0/$\overline{\text{IRQ5}}$	NC
82	85	P36	P36	P36	P36	NC
83	86	P77/TxD3	P77/TxD3	P77/TxD3	P77/TxD3	NC
84	87	P76/RxD3	P76/RxD3	P76/RxD3	P76/RxD3	NC
85	88	P75/TMO3/ SCK3	P75/TMO3/ SCK3	P75/TMO3/ SCK3	P75/TMO3/ SCK3	NC
86	89	P74/TMO2/ $\overline{\text{MRES}}$	P74/TMO2/ $\overline{\text{MRES}}$	P74/TMO2/ $\overline{\text{MRES}}$	P74/TMO2/ $\overline{\text{MRES}}$	NC
87	90	P73/TMO1/$\overline{\text{CS7}}$	P73/TMO1/$\overline{\text{CS7}}$	P73/TMO1/$\overline{\text{CS7}}$	P73/TMO1	NC
88	91	P72/TMO0/$\overline{\text{CS6}}$	P72/TMO0/$\overline{\text{CS6}}$	P72/TMO0/$\overline{\text{CS6}}$	P72/TMO0	NC
89	92	P71/TMRI23/ TMCI23/$\overline{\text{CS5}}$	P71/TMRI23/ TMCI23/$\overline{\text{CS5}}$	P71/TMRI23/ TMCI23/$\overline{\text{CS5}}$	P71/TMRI23/ TMCI23	NC
90	93	P70/TMRI01/ TMCI01/$\overline{\text{CS4}}$	P70/TMRI01/ TMCI01/$\overline{\text{CS4}}$	P70/TMRI01/ TMCI01/$\overline{\text{CS4}}$	P70/TMRI01/ TMCI01	NC
91	94	PG0/$\overline{\text{IRQ6}}$	PG0/$\overline{\text{IRQ6}}$	PG0/$\overline{\text{IRQ6}}$	PG0/$\overline{\text{IRQ6}}$	NC
92	95	PG1/$\overline{\text{CS3}}$/$\overline{\text{IRQ7}}$	PG1/$\overline{\text{CS3}}$/$\overline{\text{IRQ7}}$	PG1/$\overline{\text{CS3}}$/$\overline{\text{IRQ7}}$	PG1/$\overline{\text{IRQ7}}$	NC
93	96	PG2/$\overline{\text{Tx}}$/$\overline{\text{CS2}}$	PG2/$\overline{\text{Tx}}$/$\overline{\text{CS2}}$	PG2/$\overline{\text{Tx}}$/$\overline{\text{CS2}}$	PG2/$\overline{\text{Tx}}$	NC
94	97	PG3/$\overline{\text{Rx}}$/$\overline{\text{CS1}}$	PG3/$\overline{\text{Rx}}$/$\overline{\text{CS1}}$	PG3/$\overline{\text{Rx}}$/$\overline{\text{CS1}}$	PG3/$\overline{\text{Rx}}$	NC
95	98	PG4/$\overline{\text{CS0}}$	PG4/$\overline{\text{CS0}}$	PG4/$\overline{\text{CS0}}$	PG4	NC
96	99	PE0/D0	PE0/D0	PE0/D0	PE0	NC
97	100	PE1/D1	PE1/D1	PE1/D1	PE1	NC
98	1	PE2/D2	PE2/D2	PE2/D2	PE2	NC
99	2	PE3/D3	PE3/D3	PE3/D3	PE3	VCC
100	3	PE4/D4	PE4/D4	PE4/D4	PE4	VSS

Note: * The NC should be left open.

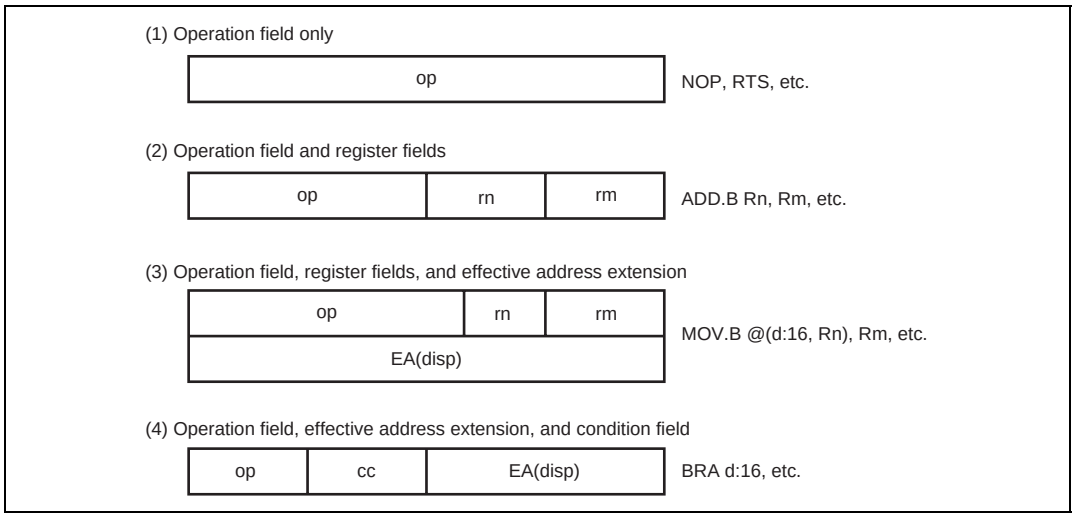


Figure 2.11 Instruction Formats (Examples)

2.7 Addressing Modes and Effective Address Calculation

The H8S/2000 CPU supports the eight addressing modes listed in table 2.11. Each instruction uses a subset of these addressing modes. Arithmetic and logic instructions can use the register direct and immediate modes. Data transfer instructions can use all addressing modes except program-counter relative and memory indirect. Bit manipulation instructions use register direct, register indirect, or the absolute addressing mode to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST instructions) or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.11 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:32,ERn)
4	Register indirect with post-increment Register indirect with pre-decrement	@ERn+ @–ERn
5	Absolute address	@aa:8/@aa:16/@aa:24/@aa:32
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

Bit	Bit Name	Initial Value	R/W	Description
11	DTA1B	0	R/W	Data Transfer Acknowledge 1B
10	DTA1A	0	R/W	Data Transfer Acknowledge 1A
9	DTA0B	0	R/W	Data Transfer Acknowledge 0B
8	DTA0A	0	R/W	Data Transfer Acknowledge 0A These bits enable or disable clearing when DMA transfer is performed for the internal interrupt source selected by the DTF3 to DTF0 bits in DMACR. It the DTA bit is set to 1 when DTE = 1, the internal interrupt source is cleared automatically by DMA transfer. When DTE = 1 and DTA = 1, the internal interrupt source does not issue an interrupt request to the CPU or DTC. If the DTA bit is cleared to 0 when DTE = 1, the internal interrupt source is not cleared when a transfer is performed, and can issue an interrupt request to the CPU or DTC in parallel. In this case, the interrupt source should be cleared by the CPU or DTC transfer. When DTE = 0, the internal interrupt source issues an interrupt request to the CPU or DTC regardless of the DTA bit setting. 0: Clearing is disabled when DMA transfer is performed for the selected internal interrupt source 1: Clearing is enabled when DMA transfer is performed for the selected internal interrupt source

- DMABCRL

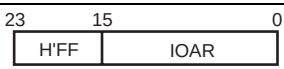
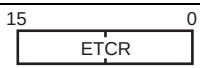
Bit	Bit Name	Initial Value	R/W	Description
7	DTE1B	0	R/W	Data Transfer Enable 1B
6	DTE1A	0	R/W	Data Transfer Enable 1A
5	DTE0B	0	R/W	Data Transfer Enable 0B
4	DTE0A	0	R/W	Data Transfer Enable 0A If the DTE bit is cleared to 0 when DTIE = 1, the DMAC regards this as indicating the end of a transfer, and issues a transfer end interrupt request to the CPU or DTC. When DTE = 0, data transfer is disabled and the DMAC ignores the activation source selected by the DTF3 to DTF0 bits in DMACR. When DTE = 1, data transfer is enabled and the DMAC waits for a request by the activation source selected by the DTF3 to DTF0 bits in DMACR. When a request is issued by the activation source, DMA transfer is executed. 0: Data transfer is disabled 1: Data transfer is enabled [Clearing conditions] • When initialization is performed • When the specified number of transfers have been completed in a transfer mode other than repeat mode • When 0 is written to the DTE bit to forcibly suspend the transfer, or for a similar reason [Setting condition] When 1 is written to the DTE bit after reading DTE = 0

8.5.2 Sequential Mode

Sequential mode can be specified by clearing the RPE bit in DMACR to 0. In sequential mode, MAR is updated after each byte or word transfer in response to a single transfer request, and this is executed the number of times specified in ETCR. One address is specified by MAR, and the other by IOAR. The transfer direction can be specified by the DTDIR bit in DMACR.

Table 8.5 summarizes register functions in sequential mode.

Table 8.5 Register Functions in Sequential Mode

	Function			
Register	**DTDIR = 0**	**DTDIR = 1**	**Initial Setting**	**Operation**
	Source address register	Destination address register	Start address of transfer destination or transfer source	Incremented/ decremented every transfer
	Destination address register	Source address register	Start address of transfer source or transfer destination	Fixed
	Transfer counter		Number of transfers	Decremented every transfer; transfer ends when count reaches H'0000

MAR specifies the start address of the transfer source or transfer destination as 24 bits. MAR is incremented or decremented by 1 or 2 each time a byte or word is transferred. IOAR specifies the lower 16 bits of the other address. The 8 bits above IOAR have a value of H'FF.

Figure 8.3 illustrates operation in sequential mode.

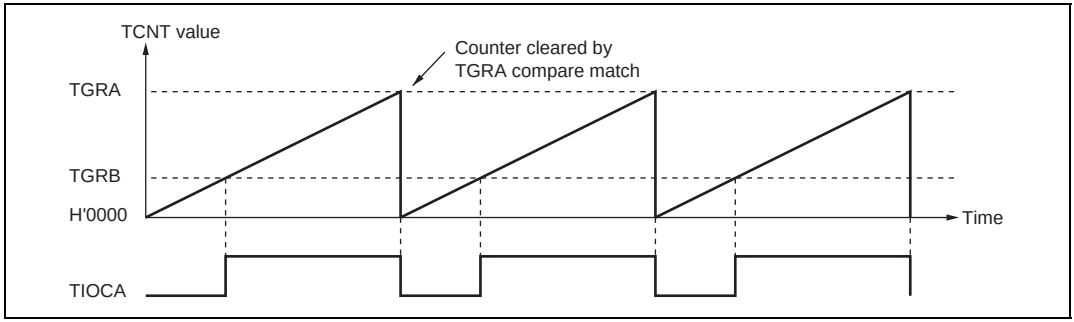


Figure 11.22 Example of PWM Mode Operation (1)

Figure 11.23 shows an example of PWM mode 2 operation.

In this example, synchronous operation is designated for channels 0 and 1, TGRB_1 compare match is set as the TCNT clearing source, and 0 is set for the initial output value and 1 for the output value of the other TGR registers (TGRA_0 to TGRD_0, TGRA_1), to output a 5-phase PWM waveform.

In this case, the value set in TGRB_1 is used as the cycle, and the values set in the other TGRs as the duty cycle.

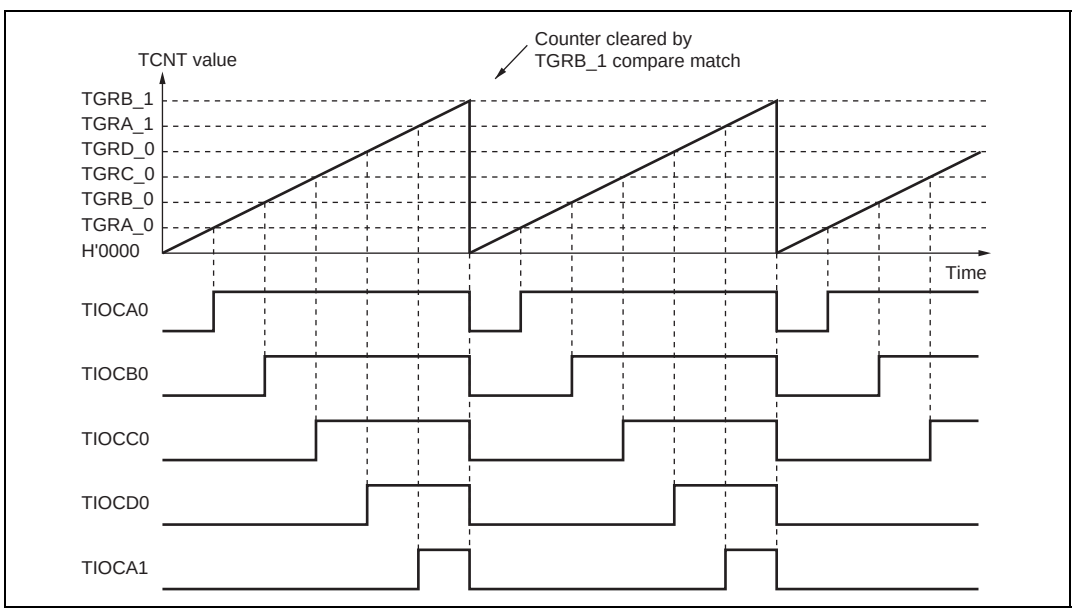


Figure 11.23 Example of PWM Mode Operation (2)

acknowledgement. The master unit reads in the subsequent data if the number of data does not exceed the maximum number of transfer bytes in one frame.

(7) Parity Bit

The parity bit is used to confirm that transfer data has no error.

The parity bit is added to respective data of the master address, slave address, control, message length, and data bits.

The even parity is used. When the number of one bits in data is odd, the parity bit is 1. When the number of one bits in data is even, the parity bit is 0.

(8) Acknowledge Bit

In normal communications (a single unit to a single unit communications), the acknowledge bit is added to the following position in order to confirm that data is correctly accepted.

- At the end of the slave address field
- At the end of the control field
- At the end of the message length field
- At the end of the data field

The acknowledge bit is defined below.

- 0: indicates that the transfer data is acknowledged. (ACK)
- 1: indicates that the transfer data is not acknowledged. (NAK)

Note that the acknowledge bit is ignored in the case of broadcast communications.

(a) Acknowledge bit at the End of the Slave Address Field

The acknowledge bit at the end of the slave address field becomes NAK in the following cases and transfer is stopped.

— When the parity of the master address or slave address bits is incorrect

— When a timing error (an error in bit format) occurs

— When there is no slave unit

(b) Acknowledge bit at the End of the Control Field

The acknowledge bit at the end of the control field becomes NAK in the following cases and transfer is stopped.

— When the parity of the control bits is incorrect

Bit	Bit Name	Initial Value	R/W	Description
5	SRQ	0	R	Slave Transmission Request Indicates whether or not the unit is in transmit request status as a slave unit. 1: The unit is in transmit request status as a slave unit [Setting condition] When the CMX flag is cleared to 0 after the slave transmit request command is issued. 0: The unit is not in transmit request status as a slave unit [Clearing condition] When a slave transmission has been completed.
4	SRE	0	R	Slave Receive Status Indicates the execution status in slave/broadcast reception. 1: Slave/broadcast reception is being executed [Setting condition] When the slave/broadcast reception is started while the RE bit in IECTR is set to 1. 0: Slave/broadcast reception is not being executed [Clearing condition] When the slave/broadcast reception has been completed.
3	LCK	0	R	Lock Status Indication Set to 1 when a unit is locked by a lock request from the master unit. IELA1 and IELA2 values are valid only when this flag is set to 1. 1: A unit is locked [Setting condition] When data for the number of bytes specified by the message length is not received after the control bits that make the unit locked are received from the master unit. (The LCK flag is set to 1 only when the message length exceeds the maximum number of transfer bytes in one frame. This flag is not set by completion of other errors.) 0: A unit is unlocked [Clearing condition] When an unlock condition is satisfied or when an unlock command is issued.

Bit	Bit Name	Initial Value	R/W	Description
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (enabled only when the MP bit in SMR is 1 in asynchronous mode) Write 0 to this bit in Smart Card interface mode. When receive data including MPB = 0 is received, receive data transfer from RSR to RDR, receive error detection, and setting of the RERF, FER, and ORER flags in SSR, are not performed. When receive data including MPB = 1 is received, the MPB bit in SSR is set to 1, the MPIE bit is cleared to 0 automatically, and generation of RXI and ERI interrupts (when the TIE and RIE bits in SCR are set to 1) and FER and ORER flag setting are enabled.
2	TEIE	0	R/W	Transmit End Interrupt Enable Write 0 to this bit in Smart Card interface mode. TEI cancellation can be performed by reading 1 from the TDRE flag in SSR, then clearing it to 0 and clearing the TEND flag to 0, or clearing the TEIE bit to 0.
1	CKE1	0	R/W	Clock Enable 0 and 1
0	CKE0	0		Enables or disables clock output from the SCK pin. The clock output can be dynamically switched in GSM mode. For details, refer to section 15.7.8, Clock Output Control. When the GM bit in SMR is 0: 00: Output disabled (SCK pin can be used as an I/O port pin) 01: Clock output 1×: Reserved When the GM bit in SMR is 1: 00: Output fixed low 01: Clock output 10: Output fixed high 11: Clock output

Legend:

×: Don’t care

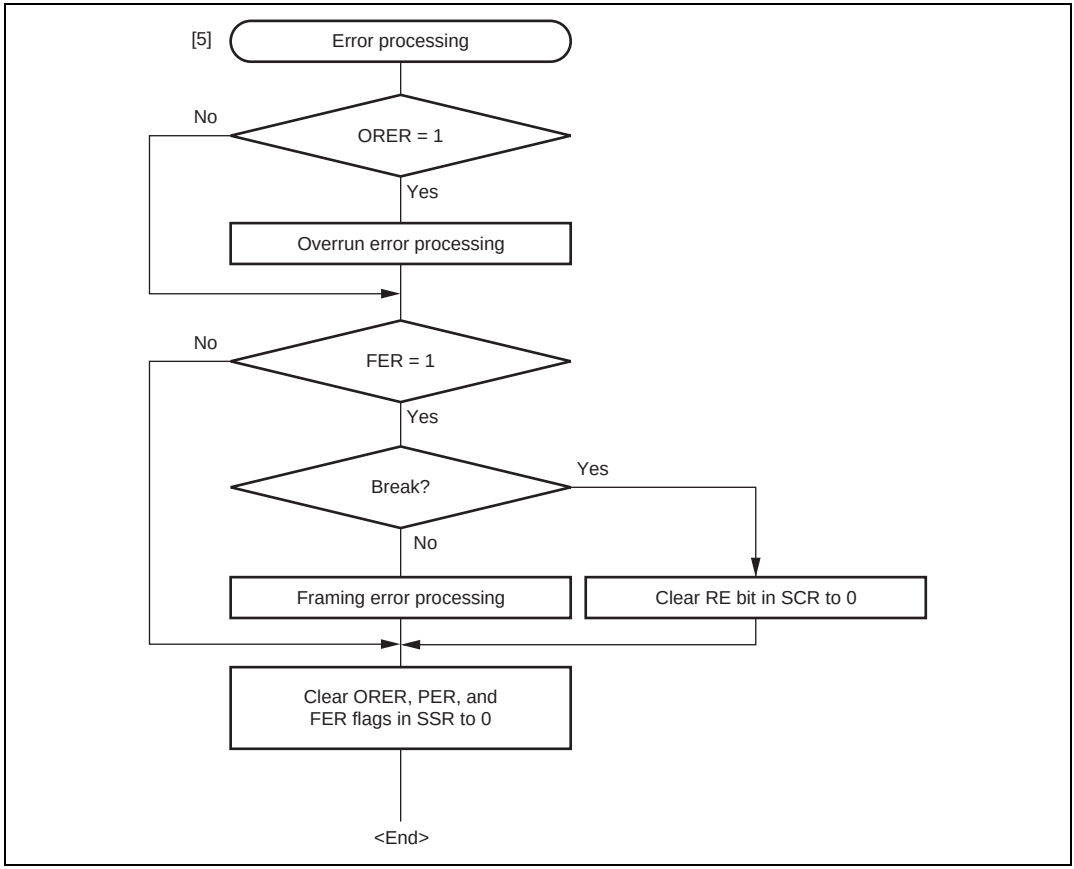


Figure 15.16 Sample Multiprocessor Serial Reception Flowchart (2)

In slave transmit mode, the slave device outputs the transmit data, while the master device outputs the receive clock and returns an acknowledge signal. The transmission procedure and operations in slave transmit mode are described below.

1. Initialize slave receive mode and wait for slave address reception.
   When making initial settings for slave receive mode, set the ACKE bit in ICCR to 1. This is necessary in order to enable reception of the acknowledge bit after entering slave transmit mode.
2. When the slave address matches in the first frame following detection of the start condition, the slave device drives SDA low at the 9th clock pulse and returns an acknowledge signal. If the 8th data bit (R/$\overline{W}$) is 1, the TRS bit in ICCR is set to 1, and the mode changes to slave transmit mode automatically. The IRIC flag is set to 1 at the rise of the 9th clock. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU. At the same time, the TDRE internal flag is set to 1. The slave device drives SCL low from the fall of the transmit 9th clock until ICDR data is written, to disable the master device to output the next transfer clock.
3. After clearing the IRIC flag to 0, write data to ICDR. At this time, the TDRE internal flag is cleared to 0. The written data is transferred to ICDRS, and the TDRE internal flag and IRIC flag are set to 1 again. The slave device sequentially sends the data written into ICDRS in accordance with the clock output by the master device.

   The IRIC flag is cleared to 0 to detect the end of transmission. Processing from the ICDR register writing to the IRIC flag clearing should be performed continuously. Prevent any processing that includes interrupt processing during this period. If a duration sufficient for one byte of data to be transferred elapses before the IRIC flag is cleared, it will not be possible to determine that the transfer has completed.
4. The master device drives SDA low at the 9th clock pulse, and returns an acknowledge signal. When the value of the ACKE bit in ICSR is 1, the acknowledge signal state is stored in the ACKB bit, so the ACKB bit can be used to determine whether the transfer operation was performed successfully. When one frame of data has been transmitted, the IRIC flag in ICCR is set to 1 at the rise of the 9th transmit clock pulse. When the TDRE internal flag is 0, the data written into ICDR is transferred to ICDRS, transmission starts, and the TDRE internal flag and IRIC flag are set to 1 again. If the TDRE internal flag has been set to 1, this slave device drives SCL low from the fall of the 9th transmit clock until data is written to ICDR.
5. To continue transmission, write the next data to be transmitted into ICDR. The TDRE internal flag is cleared to 0. The IRIC flag is cleared to 0 to detect the end of transmission. Processing from the ICDR writing to the IRIC flag clearing should be performed continuously. Prevent any processing that includes interrupt processing during this period.

Transmit operations can be performed continuously by repeating steps [4] and [5].

17.2 Input/Output Pins

Table 17.1 summarizes the input pins used by the A/D converter. The eight analog input pins are divided into two groups each of which consists of four channels; analog input pins 0 to 3 (AN0 to AN3) comprising group 0 and analog input pins 4 to 7 (AN4 to AN7) comprising group 1. The AVcc and AVss pins are the power supply pins for the analog block in the A/D converter. The Vref pin is the A/D conversion reference voltage pin.

Table 17.1 Pin Configuration

Pin Name	Symbol	I/O	Function
Analog power supply pin	AV_{CC}	Input	Analog block power supply and reference voltage
Analog ground pin	AV_{SS}	Input	Analog block ground and reference voltage
Reference voltage pin	Vref	Input	Reference voltage for A/D conversion
Analog input pin 0	AN0*	Input	Group 0 analog input pins
Analog input pin 1	AN1*	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 4	AN4	Input	Group 1 analog input pins
Analog input pin 5	AN5	Input	
Analog input pin 6	AN6	Input	
Analog input pin 7	AN7	Input	
A/D external trigger input pin	$\overline{\text{ADTRG}}$	Input	External trigger input pin for starting A/D conversion

Note: * In the case of the H8S/2239 Group, H8S/2227 Group, H8S/2238R, and H8S/2236R, AN0 and AN1 may be used only when Vcc = AVcc.

Table 22.2 Socket Adapters

		Socket Adapter	
Product Name	**Package**	**Minato Electronics**	**Data IO Japan**
H8S/2237	100-pin TQFP (TFP-100B)	ME2237ESNS1H	H7223BT100D3201
	100-pin TQFP (TFP-100G)	ME2237ESMS1H	H7223GT100D3201
	100-pin QFP (FP-100A)	ME2237ESFS1H	H7223AQ100D3201
	100-pin QFP (FP-100B)	ME2237ESHS1H	H7223BQ100D3201

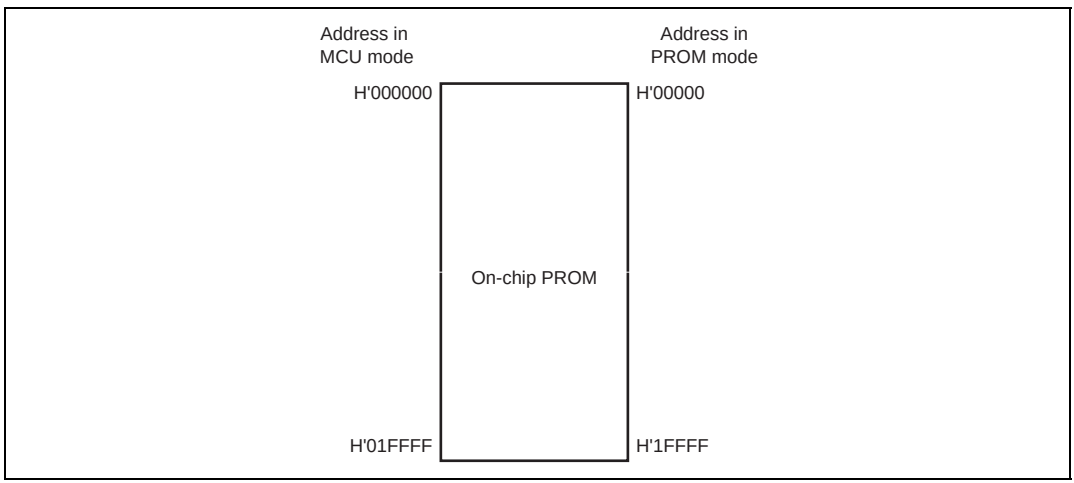


Figure 22.3 Memory Map in PROM Mode

Section 24 Power-Down Modes

In addition to the normal program execution state, this LSI has nine power-down modes in which operation of the CPU and oscillator is halted and power dissipation is reduced. Low-power operation can be achieved by individually controlling the CPU, on-chip peripheral modules, and so on.

This LSI operating modes are as follows:

1. High-speed mode
2. Medium-speed mode
3. Subactive mode
4. Sleep mode
5. Subsleep mode
6. Watch mode
7. Module stop mode
8. Software standby mode
9. Hardware standby mode

2. to 9. are low power dissipation states. Sleep mode and subsleep mode are CPU states, medium-speed mode is a CPU and bus master state, subactive mode is a CPU and bus master and internal peripheral function state, and module stop mode is an internal peripheral function (including bus masters other than the CPU) state. Some of these states can be combined.

After a reset, the LSI is in high-speed mode with modules other than the DTC in module stop mode.

Table 24.1 shows the internal state of the LSI in the respective modes. Table 24.2 shows the conditions for shifting between the low power dissipation modes.

Figure 24.1 is a mode transition diagram.

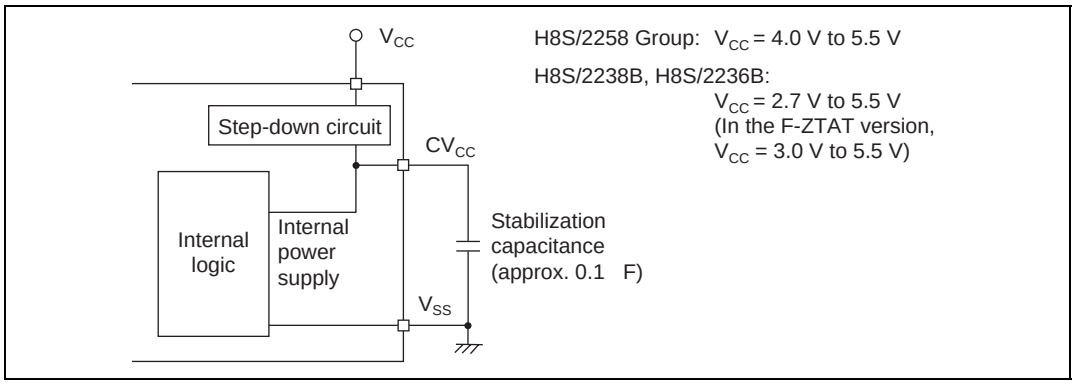


Figure 25.1 Power Supply Connection for H8S/2258 Group, H8S/2238B, and H8S/2236B (On-Chip Internal Power Supply Step-Down Circuit)

25.3 Power Supply Connection for H8S/2239 Group, H8S/2238R, H8S/2236R, H8S/2237 Group, and H8S/2227 Group (No Internal Power Supply Step-Down Circuit)

The H8S/2239 Group, H8S/2238R, H8S/2236R, H8S/2237 Group, and H8S/2227 Group do not have an on-chip internal power supply voltage step-down circuit. Connect the external power supply to the V_{CC} pin and CV_{CC} pin, as shown in figure 25.2. The external power supply is then input directly to the internal power supply.

Note: The permissible range for the power supply voltage is 2.2 V to 3.6 V (in the F-ZTAT version, 2.7 V to 3.6 V). Operation cannot be guaranteed if a voltage outside this range (less than 2.2 V or more than 3.6 V) is input.

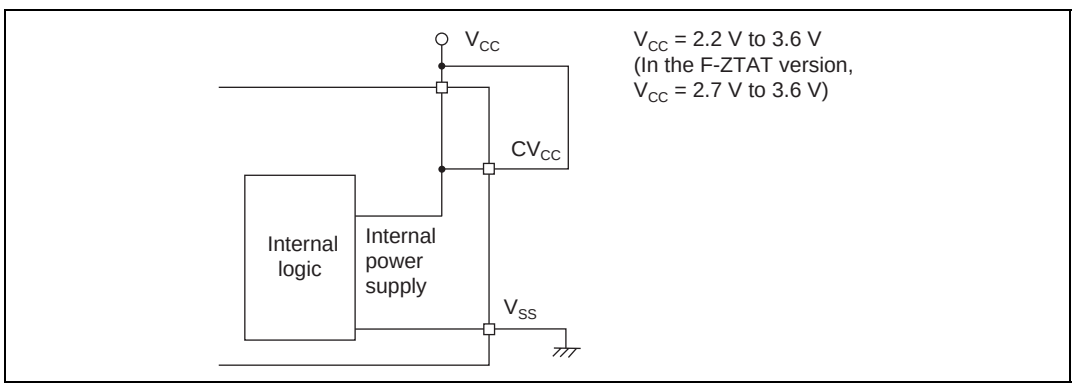


Figure 25.2 Power Supply Connection for H8S/2239 Group, H8S/2238R, H8S/2236R, H8S/2237 Group, and H8S/2227 Group (No Internal Power Supply Step-Down Circuit)

25.4 Note on Bypass Capacitor

A laminated ceramic capacitor of 0.01 μF to 0.1 μF should be inserted as a bypass capacitor in each pair of V_{SS} and V_{CC}.

The bypass capacitor should be placed as close as possible to the power supply pin of this LSI.

The capacitance value and frequency characteristics should be used according to the operating frequency of this LSI.

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Output high voltage	All output pins*4 except P34 and P35	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA*2
	P34 and P35*3		V_{CC} – 2.0	—	—	V	I_{OH} = –100 µA (reference value)
Output low voltage	All output pins*4	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA
			—	—	0.4	V	I_{OL} = 0.8 mA*2
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0.2 to V_{CC} – 0.2 V
	$\overline{STBY}$, NMI, FWE, MD2 to MD0		—	—	1.0	µA	
	Ports 4, 9		—	—	1.0	µA	V_{in} = 0.2 to AV_{CC} – 0.2 V
Three states leakage current (off)	Ports 1, 3, 7, and A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.2 to V_{CC} – 0.2 V
Input pull-up MOS current	Ports A to E	$-I_P$	10	—	300	µA	V_{in} = 0V

Notes:
1. If the A/D or D/A converter is not used, the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Even if the A/D or D/A converter is not used, connect the AV_{CC} and V_{ref} pins to V_{CC} and supply 2.0 V to 3.6 V. In this case, $V_{ref} \leq AV_{CC}$.
2. V_{CC} = 2.7 V to 3.6 V
3. P35/SCK1 and P34 function as NMOS push-pull output. To output the high voltage, connect an external pull-up resistor.
4. In the case when ICE = 0. Low voltage output with bus driving function is specified in table 27.41.
5. When $V_{CC} < AV_{CC}$, the maximum value for P40 and P41 is V_{CC} + 0.3 V.

Table 27.51 DC Characteristics (4)

Conditions (Masked ROM version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V,
V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)*1

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	$\overline{RES}$	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25 °C
	NMI		—	—	50	pF	
	All input pins other than above ones		—	—	15	pF	
Current consumption*2	Normal operation	I_{CC}*4	—	20 V_{CC} = 3.0 V	37 V_{CC} = 3.6 V	mA	f = 13.5 MHz
			—	10 V_{CC} = 3.0 V	18 V_{CC} = 3.6 V	mA	f = 6.25 MHz
	Sleep mode		—	15 V_{CC} = 3.0 V	29 V_{CC} = 3.6 V	mA	f = 13.5 MHz
			—	7.5 V_{CC} = 3.0 V	14 V_{CC} = 3.6 V	mA	f = 6.25 MHz
	All modules stopped		—	15	—	mA	f = 13.5 MHz, V_{CC} = 3.0 V (reference value)
	Medium-speed mode (ϕ/32)		—	11	—	mA	f = 13.5 MHz, V_{CC} = 3.0 V (reference value)
	Subactive mode		—	60	160	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used

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Hardware Manual
H8S/2258, H8S/2239, H8S/2238, H8S/2237,
H8S/2227 Groups

Publication Date: 1st Edition, September 2002
Rev.6.00, March 18, 2010
Published by: Sales Strategic Planning Div.
Renesas Technology Corp.
Edited by: Customer Support Department
Global Strategic Communication Div.
Renesas Solutions Corp.