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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2238bfa13v

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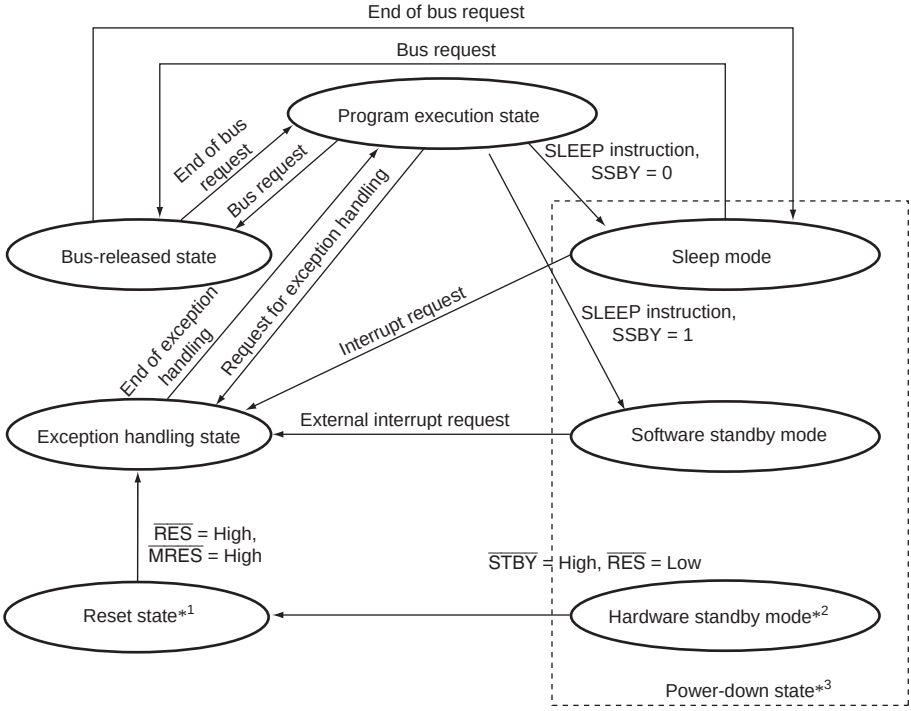
1.3.2 Pin Arrangements in Each Mode

Tables 1.1 to 1.5 show the pin arrangements in each mode.

Table 1.1 Pin Arrangements in Each Mode of H8S/2258 Group

Pin No.		Pin Name				
TFP-100B FP-100B	FP-100A	Mode 4	Mode 5	Mode 6	Mode 7	Flash Memory Programmable Mode*
1	4	PE5/D5	PE5/D5	PE5/D5	PE5	$\overline{OE}$
2	5	PE6/D6	PE6/D6	PE6/D6	PE6	$\overline{WE}$
3	6	PE7/D7	PE7/D7	PE7/D7	PE7	$\overline{CE}$
4	7	D8	D8	D8	PD0	D0
5	8	D9	D9	D9	PD1	D1
6	9	D10	D10	D10	PD2	D2
7	10	D11	D11	D11	PD3	D3
8	11	D12	D12	D12	PD4	D4
9	12	D13	D13	D13	PD5	D5
10	13	D14	D14	D14	PD6	D6
11	14	D15	D15	D15	PD7	D7
12	15	CVCC	CVCC	CVCC	CVCC	VCC
13	16	A0	A0	PC0/A0	PC0	A0
14	17	VSS	VSS	VSS	VSS	VSS
15	18	A1	A1	PC1/A1	PC1	A1
16	19	A2	A2	PC2/A2	PC2	A2
17	20	A3	A3	PC3/A3	PC3	A3
18	21	A4	A4	PC4/A4	PC4	A4
19	22	A5	A5	PC5/A5	PC5	A5
20	23	A6	A6	PC6/A6	PC6	A6
21	24	A7	A7	PC7/A7	PC7	A7
22	25	PB0/A8/TIOCA3	PB0/A8/TIOCA3	PB0/A8/TIOCA3	PB0/TIOCA3	A8
23	26	PB1/A9/TIOCB3	PB1/A9/TIOCB3	PB1/A9/TIOCB3	PB1/TIOCB3	A9
24	27	PB2/A10/ TIOCC3	PB2/A10/ TIOCC3	PB2/A10/ TIOCC3	PB2/TIOCC3	A10
25	28	PB3/A11/ TIOCD3	PB3/A11/ TIOCD3	PB3/A11/ TIOCD3	PB3/TIOCD3	A11



Notes: 1. From any state except hardware standby mode, a transition to the reset state occurs whenever $\overline{RES}$ goes low. A transition can also be made to the reset state when the watchdog timer overflows. From any state except hardware standby mode and power-on reset state, a transition to the manual reset state occurs whenever $\overline{MRES}$ goes low.
2. From any state, a transition to hardware standby mode occurs when $\overline{STBY}$ goes low.
3. Apart from these states, there are also the watch mode, subactive mode, and the subsleep mode. See section 24, Power-Down Modes.

Figure 2.13 State Transitions

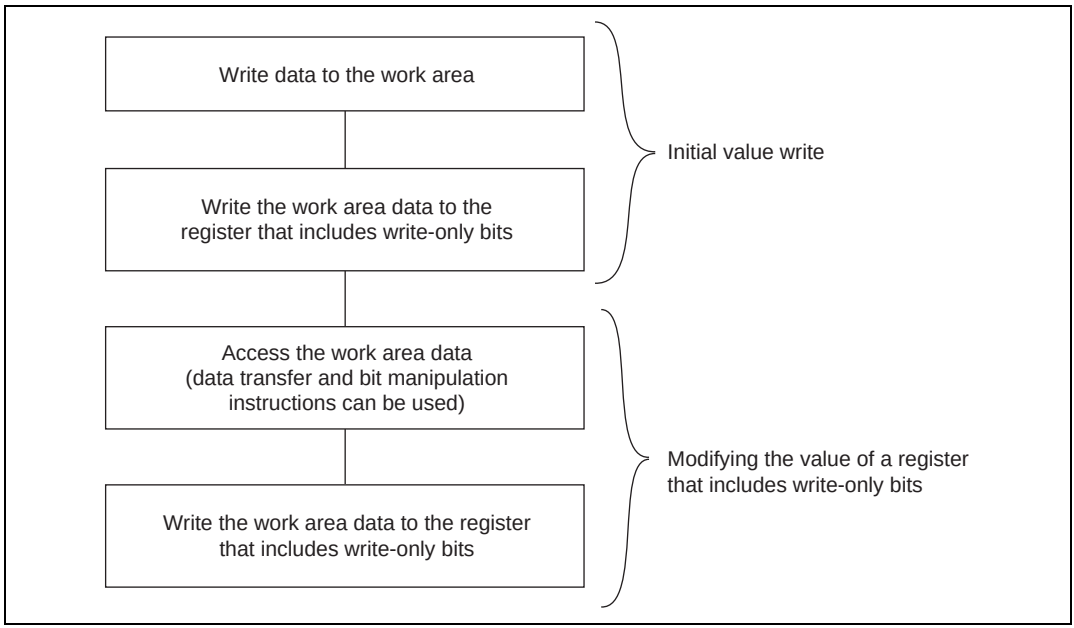


Figure 2.14 Flowchart for Access Methods for Registers That Include Write-Only Bits

Example: To clear only bit 4 in the port 1 P1DDR

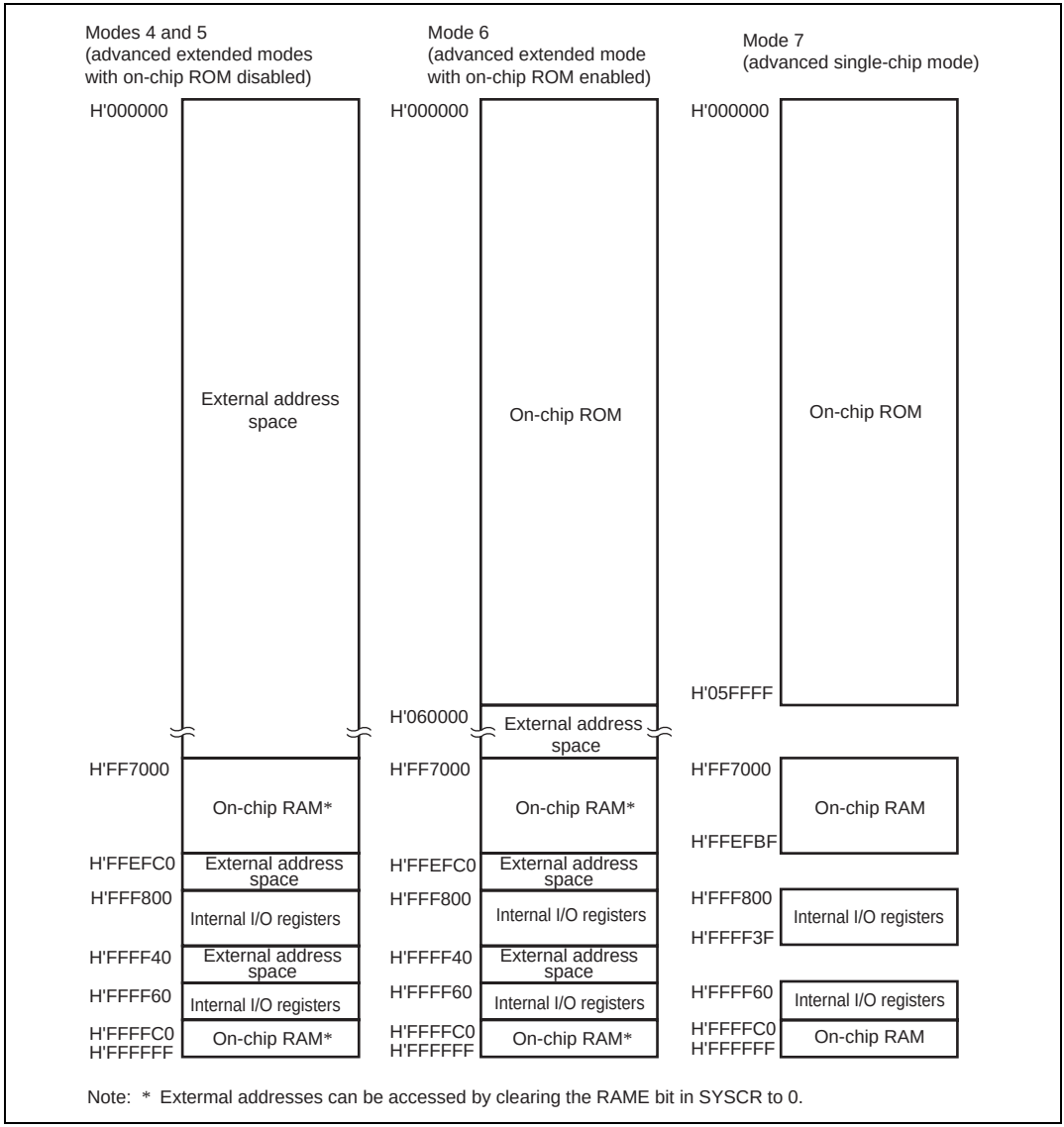
The P1DDR register consists of 8 write-only bits and sets the I/O direction of the port 1 pins. Reading this register is invalid. When read, the values returned are undefined.

Here we present an example in which P14 is specified to be an input port using the BCLR instruction. First, we write the initial value H'F0 written to P1DDR to the work area in RAM (RAM0).

```
MOV.B   #H'F0,   R0L
MOV.B   R0L,     @PAM0
MOV.B   R0L,     @P1DDR
```

	P17	P16	P15	P14	P13	P12	P11	P10
I/O	Output	Output	Output	Output	Input	Input	Input	Input
P1DDR	1	1	1	1	0	0	0	0

RAM0	1	1	1	1	0	0	0	0



Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 3.3 H8S/2239 Memory Map in Each Operating Mode

(2) Write after Read

If an external write occurs after an external read while the ICIS0 bit in BCRH is set to 1, an idle cycle is inserted at the start of the write cycle.

Figure 7.22 shows an example of the operation in this case. In this example, bus cycle A is a read cycle from ROM with a long output floating time, and bus cycle B is a CPU write cycle. In (a), an idle cycle is not inserted, and a collision occurs in cycle B between the read data from ROM and the CPU write data. In (b), an idle cycle is inserted, and a data collision is prevented.

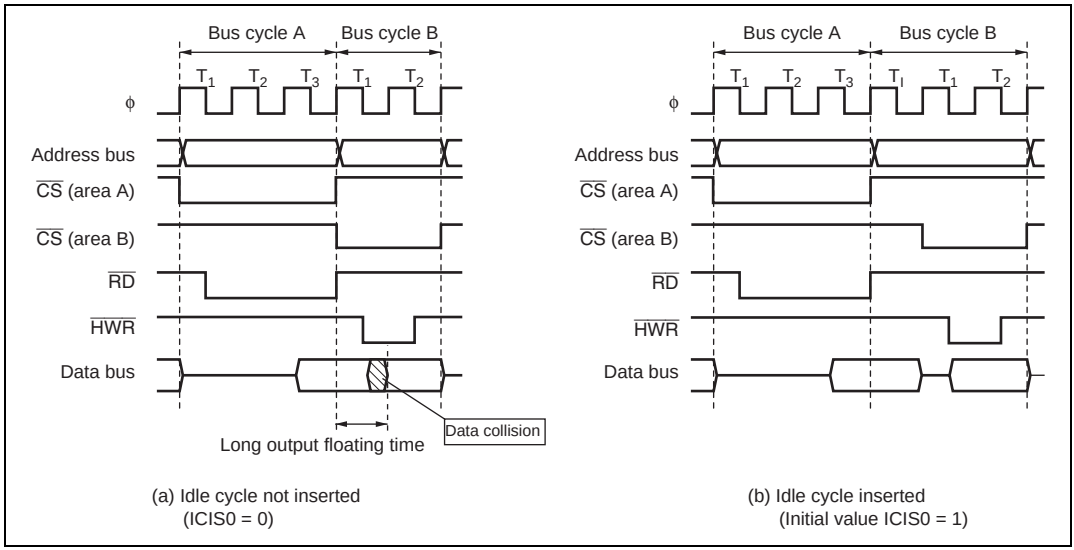


Figure 7.22 Example of Idle Cycle Operation (2)

(3) Relationship between Chip Select ($\overline{CS}$) Signal and Read ($\overline{RD}$) Signal

Depending on the system's load conditions, the $\overline{RD}$ signal may lag behind the $\overline{CS}$ signal. An example is shown in figure 7.23.

In this case, with the setting for no idle cycle insertion (a), there may be a period of overlap between the bus cycle A $\overline{RD}$ signal and the bus cycle B $\overline{CS}$ signal.

Setting idle cycle insertion, as in (b), however, will prevent any overlap between the $\overline{RD}$ and $\overline{CS}$ signals.

In the initial state after reset release, idle cycle insertion (b) is set.

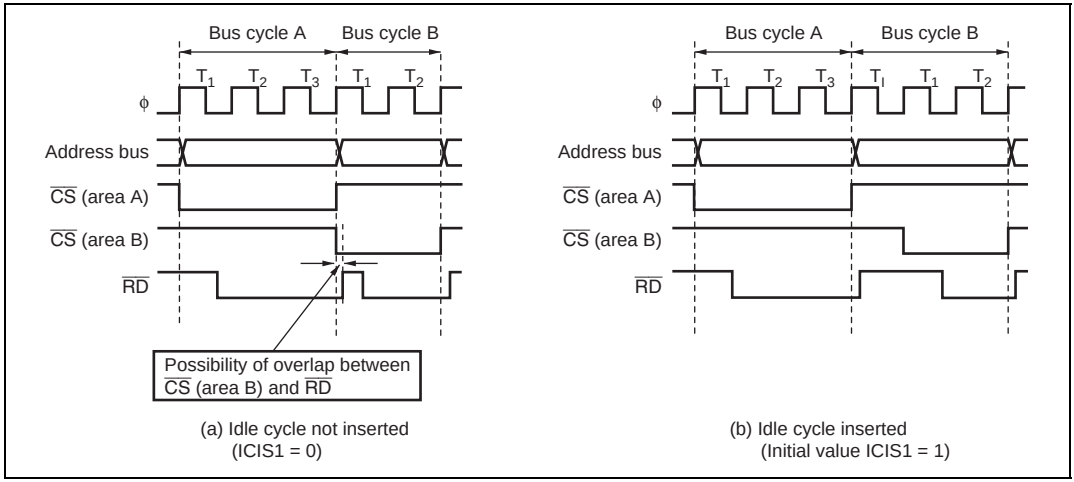


Figure 7.23 Relationship between Chip Select ($\overline{CS}$) and Read ($\overline{RD}$)

Table 7.4 shows pin states in an idle cycle.

Table 7.4 Pin States in Idle Cycle

Pins	Pin State
A23 to A0	Contents of next bus cycle
D15 to D0	High impedance
$\overline{CSn}$	High
$\overline{AS}$	High
$\overline{RD}$	High
$\overline{HWR}$	High
$\overline{LWR}$	High

9.2.7 DTC Enable Registers A to G, and I (DTCERA to DTCERG, and DTCERI)

DTCER is a set of registers to specify the DTC activation interrupt source, and comprised of eight registers; DTCERA to DTCERG, and DTCERI. The correspondence between interrupt sources and DTCE bits, and vector numbers generated by the interrupt controller are shown in table 9.2. For DTCE bit setting, use bit manipulation instructions such as BSET and BCLR for reading and writing. When multiple activation sources are to be set at one time, only at the initial setting, writing data is enabled after executing a dummy read on the relevant register with all the interrupts being masked.

Bit	Bit Name	Initial Value	R/W	Description
7	DTCEn7	0	R/W	DTC Activation Enable
6	DTCEn6	0	R/W	0: Disables an interrupt for DTC activation.
5	DTCEn5	0	R/W	1: Specifies a relevant interrupt source as a DTC activation source.
4	DTCEn4	0	R/W	[Clearing conditions]
3	DTCEn3	0	R/W	• When the DISEL bit in MRB is 1 and the data transfer has ended
2	DTCEn2	0	R/W	• When the specified number of transfers have ended
1	DTCEn1	0	R/W	[Retaining condition]
0	DTCEn0	0	R/W	When the DISEL bit is 0 and the specified number of transfers have not been completed

Note: n = A to G, and I

10.2 Port 3

Port 3 is a general 7-bit I/O port and has the following registers.

The P34, P35, and SCK1 function as NMOS push/pull outputs.*

- Port 3 data direction register (P3DDR)
- Port 3 data register (P3DR)
- Port 3 register (PORT3)
- Port 3 open drain control register (P3ODR)

Note: * Function as CMOS outputs in the H8S/2237 Group and H8S/2227 Group.

10.2.1 Port 3 Data Direction Register (P3DDR)

P3DDR specifies input or output of the port 3 pins using the individual bits.

P3DDR cannot be read; if it is, an undefined value will be read.

This register is a write-only register, and cannot be written by bit manipulation instruction. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7	—	Undefined	—	Reserved These bits are always read as undefined value.
6	P36DDR	0	W	When a pin is specified as a general purpose I/O port, setting this bit to 1 makes the corresponding port 3 pin an output port. Clearing this bit to 0 makes the pin an input port.
5	P35DDR	0	W	
4	P34DDR	0	W	
3	P33DDR	0	W	
2	P32DDR	0	W	
1	P31DDR	0	W	
0	P30DDR	0	W	

- PA0/A16

  The pin functions are switched as shown below according to the combination of operating mode, AE3 to AE0 bits in PFCR and the PA0DDR bit.

Operating mode	Modes 4 to 6			Mode 7	
AE3 to AE0	Other than (B'0xxx or B'1000)	B'0xxx or B'1000		—	
PA0DDR	—	0	1	0	1
Pin functions	A16 output pin	PA0 input pin	PA0 output pin*	PA0 input pin	PA0 output pin*

Note: * When PA0ODR in PAODR is set to 1, the corresponding pin functions as NMOS open drain output.

10.6.7 Input Pull-Up MOS States in Port A

Port A has a built-in input pull-up MOS function that can be controlled by software. Input pull-up MOS can be specified as on or off on an individual bit basis.

Table 10.2 summarizes the input pull-up MOS states.

Table 10.2 Input Pull-Up MOS States in Port A

Pin States	Power-on Reset	Hardware Standby Mode	Manual Reset	Software Standby Mode	In Other Operations
Address output, Port output, SCI output	OFF	OFF	OFF	OFF	OFF
Port input, SCI input			ON/OFF	ON/OFF	ON/OFF

Legend:

OFF: Input pull-up MOS is always off.

ON/OFF: On when PADDR = 0 and PAPCR = 1; otherwise off.

10.7 Port B

Port B is a 8-bit I/O port. Port B has the following registers.

- Port B data direction register (PBDDR)
- Port B data register (PBDR)
- Port B register (PORTB)

Example of Phase Counting Mode Setting Procedure: Figure 11.25 shows an example of the phase counting mode setting procedure.

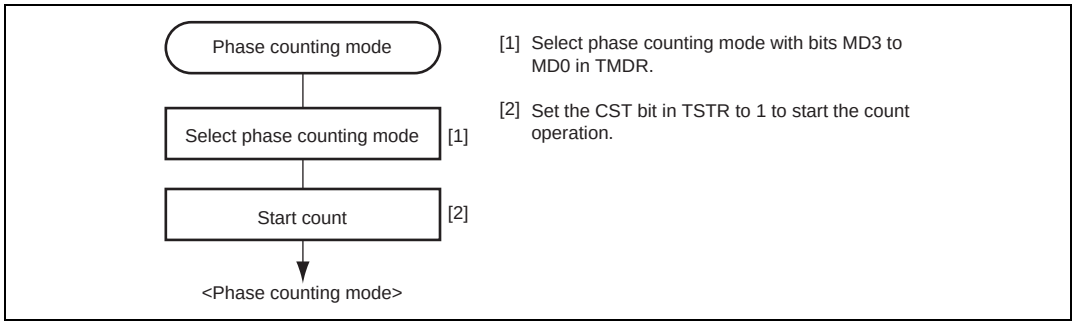


Figure 11.25 Example of Phase Counting Mode Setting Procedure

Examples of Phase Counting Mode Operation: In phase counting mode, TCNT counts up or down according to the phase difference between two external clocks. There are four modes, according to the count conditions.

1. Phase counting mode 1

   Figure 11.26 shows an example of phase counting mode 1 operation, and table 11.32 summarizes the TCNT up/down-count conditions.

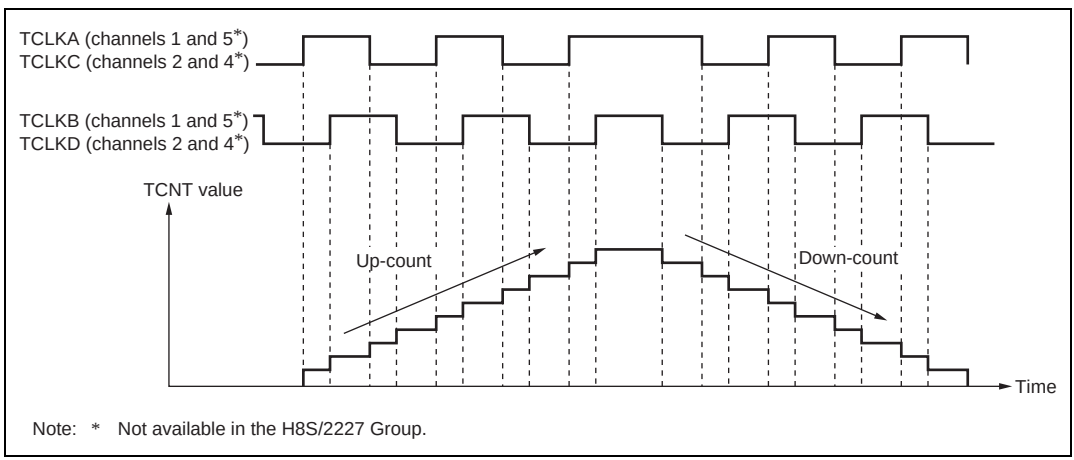


Figure 11.26 Example of Phase Counting Mode 1 Operation

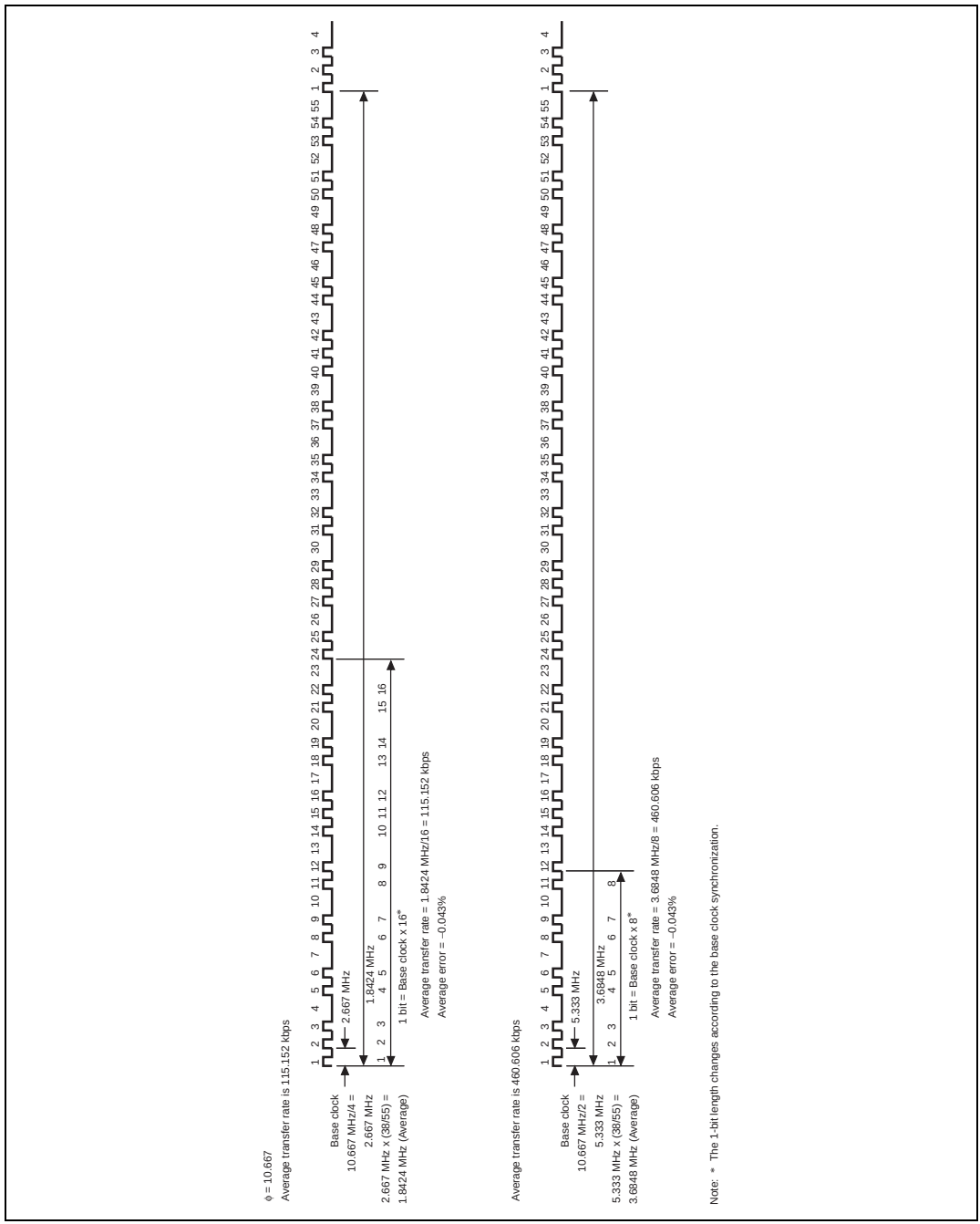


Figure 15.3 Example of the Internal Base Clock When the Average Transfer Rate Is Selected (1)

15.4.6 Serial Data Reception (Asynchronous Mode)

Figure 15.11 shows an example of operation for reception in asynchronous mode. In serial reception, the SCI operates as described below.

1. The SCI monitors the communication line. If a start bit is detected, the SCI performs internal synchronization, receives receive data in RSR, and checks the parity bit and stop bit.
2. If an overrun error occurs (when reception of the next data is completed while the RDRF flag is still set to 1), the ORER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR. The RDRF flag remains to be set to 1.
3. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated.
4. If a framing error is detected (when the stop bit is 0), the FER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated.
5. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt request is generated. Continuous reception is possible because the RXI interrupt routine reads the receive data transferred to RDR before reception of the next receive data has been completed.

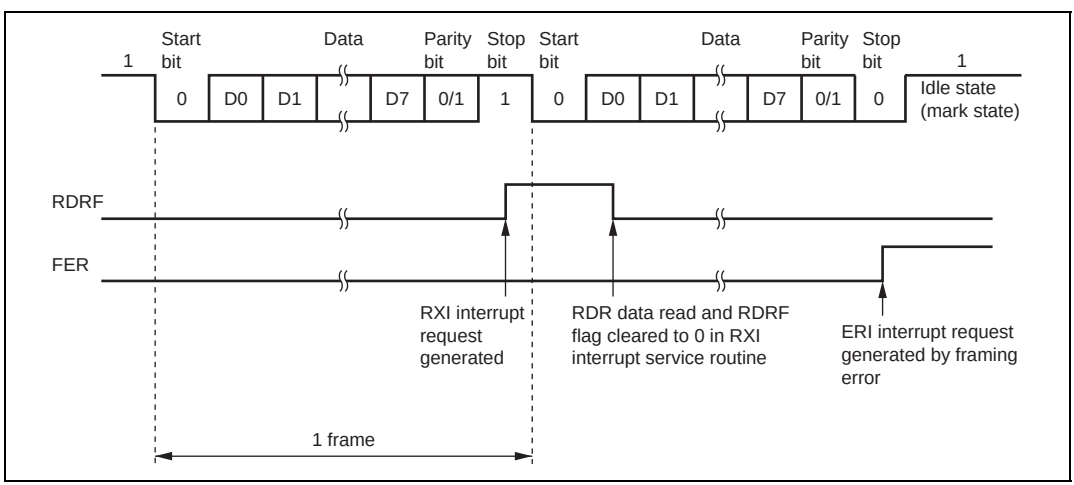


Figure 15.11 Example of SCI Operation in Reception (Example with 8-Bit Data, Parity, One Stop Bit)

16.4.4 Master Receive Operation

In I²C bus format master receive mode, the master device outputs the receive clock, receives data, and returns an acknowledge signal. The slave device transmits data.

The master device transmits the data containing the slave address + R/$\overline{W}$ (0: read) in the 1st frame after a start condition is generated in the master transmit mode. After the slave device is selected the switch to receive operation takes place.

(1) Receive Operation Using Wait States

Figures 16.10 and 16.11 are flowcharts showing examples of the master receive mode (WAIT = 1).

23.1.2 Low-Power Control Register (LPWRCR)

LPWRCR performs down-mode control, selects sampling frequency for eliminating noise, performs subclock generation control, and specifies multiplication factor.

Bit	Bit Name	Initial Value	R/W	Description
7	DTON	0	R/W	Direct Transfer ON Flag 0: When the SLEEP instruction is executed in high-speed mode or medium-speed mode, operation shifts to sleep mode, software standby mode, or watch mode*. When the SLEEP instruction is executed in sub-active mode, operation shifts to sub-sleep mode or watch mode. 1: When the SLEEP instruction is executed in high-speed mode or medium-speed mode, operation shifts directly to sub-active mode*, or shifts to sleep mode or software standby mode. When the SLEEP instruction is executed in sub-active mode, operation shifts directly to high-speed mode, or shifts to sub-sleep mode.
6	LSON	0	R/W	Low Speed ON Fag 0: When the SLEEP instruction is executed in high-speed mode or medium-speed mode, operation shifts to sleep mode, software standby mode, or watch mode*. When the SLEEP instruction is executed in sub-active mode, operation shifts to watch mode* or shifts directly to high-speed mode. Operation shifts to high-speed mode when watch mode is cancelled. 1: When the SLEEP instruction is executed in high-speed mode, operation shifts to watch mode or sub-active mode. When the SLEEP instruction is executed in sub-active mode, operation shifts to sub-sleep mode or watch mode. Operation shifts to sub-active mode when watch mode is cancelled.

23.3 Duty Adjustment Circuit

The duty adjustment circuit is valid when oscillation frequency is more than 5 MHz. The duty adjustment circuit adjusts clock output fr/m the system clock oscillator to generate the system clock (ϕ).

23.4 Medium-Speed Clock Divider

The medium-speed clock divider divides the system clock to generate ϕ/2, ϕ/4, ϕ/8, ϕ/16, and ϕ/32.

23.5 Bus Master Clock Selection Circuit

The bus master clock selection circuit selects the clock supplied to the bus master by setting the bits SCK2 to SCK0 in SCKCR. The bus master clock can be selected from system clock (ϕ), or medium-speed clocks (ϕ/2, ϕ/4, ϕ/8, ϕ/16, ϕ/32).

23.6 System Clock when Using IEBus

When using the IEBus, the system clock must be set to either 12 MHz or 12.58 MHz. When the IEBus is not used, the system clock can be set to an arbitrary frequency between 10 MHz to 13.5 MHz.

Note: IEBus is supported only by the H8S/2258 Group.

Table 27.4 Bus Driving Characteristics

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{ref} = 4.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)*

Objective pins: SCL1, SCL0, SDA1, and SDA0

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	VT^-	$V_{CC} \times 0.3$	—	—	V	V_{CC} = 4.0 V to 5.5 V
	VT^+	—	—	$V_{CC} \times 0.7$		V_{CC} = 4.0 V to 5.5 V
	$VT^+ - VT^-$	0.4	—	—		V_{CC} = 4.0 V to 5.5 V
Input high voltage	V_{IH}	$V_{CC} \times 0.7$	—	V_{CC} + 0.5	V	V_{CC} = 4.0 V to 5.5 V
Input low voltage	V_{IL}	–0.5	—	$V_{CC} \times 0.3$	V	V_{CC} = 4.0 V to 5.5 V
Output low voltage	V_{OL}	—	—	0.5	V	I_{OL} = 8 mA
		—	—	0.4		I_{OL} = 3 mA
Input capacitance	C_{in}	—	—	20	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
Three states leakage current (off)	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
SCL, SDA output falling time	t_{of}	20 + 0.1 Cb	—	250	ns	V_{CC} = 4.0 V to 5.5 V

Note: * If the A/D or D/A converter is not used, the AVCC, V_{ref}, and AVSS pins should not be open. Even if the A/D or D/A converter is not used, connect the AVCC and V_{ref} pins to V_{CC} and supply 4.0 V to 5.5 V. In this case, $V_{ref} \leq AV_{CC}$.

27.6.5 D/A Conversion Characteristics

Table 27.58 lists the D/A conversion characteristics.

Table 27.58 D/A Conversion Characteristics

Condition A (ZTAT version): V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 10 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B (Masked ROM version): V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 13.5MHz, T_a = –20°C to +75°C (regular specifications)

Condition C (Masked ROM version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V, V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 6.25 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

	Condition A			Condition B			Condition C				
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
Resolution	8	8	8	8	8	8	8	8	8	bits	
Conversion time	—	—	10	—	—	10	—	—	10	µs	Load capacitance = 20 pF
Absolute accuracy*	—	±2.0	±3.0	—	±2.0	±3.0	—	±3.0	±4.0	LSB	Load resistance = 2 MΩ
	—	—	±2.0	—	—	±2.0	—	—	±3.0	LSB	Load resistance = 4 MΩ

Note: * Does not apply in module stop mode, software standby mode, watch mode, subactive mode, or subsleep mode.

Port Name / Pin Name	MCU Operating Mode	Power-On Reset	Manual Reset	Hardware Standby Mode	Software Standby Mode, Watch Mode	Bus Mastership Release State	Program Execution State, Sleep Mode, Subsleep Mode
Port 3	4 to 7	T	keep	T	keep	keep	I/O port
Port 4	4 to 7	T	T	T	T	T	Input port
P77 to P74	4 to 7	T	keep	T	keep	keep	I/O port
P73/TMO1/ $\overline{\text{TEND1}}$*3/$\overline{\text{CS7}}$	7	T	keep	T	keep	keep	I/O port
P73/TMO1/ $\overline{\text{TEND1}}$*3/$\overline{\text{CS7}}$ P72/TMO0/ $\overline{\text{TEND0}}$*3/$\overline{\text{CS6}}$ P71/TMRI23*2/ TMCI23*2/ $\overline{\text{DREQ1}}$*3/$\overline{\text{CS5}}$ P70/TMRI01/ TMCI01/ $\overline{\text{DREQ0}}$*3/$\overline{\text{CS4}}$	4 to 6	T	keep	T	[DDR · OPE = 0] T [DDR · OPE = 1] H	T	[DDR = 0] Input port [DDR = 1] $\overline{\text{CS7}}$ to $\overline{\text{CS4}}$
P97/DA1*4 P96/DA0*4	4 to 7	T	T	T	[DAOEn = 1] keep [DAOEn = 0] T	keep	Input port
Port A	7	T	keep	T	keep	keep	I/O port
When the address output is selected by the AEn bit	4, 5	L	keep	T	[OPE = 0] T [OPE = 1] keep	T	Address output
	6	T					
When a port is selected	4 to 6	T*1	keep	T	keep	keep	I/O port