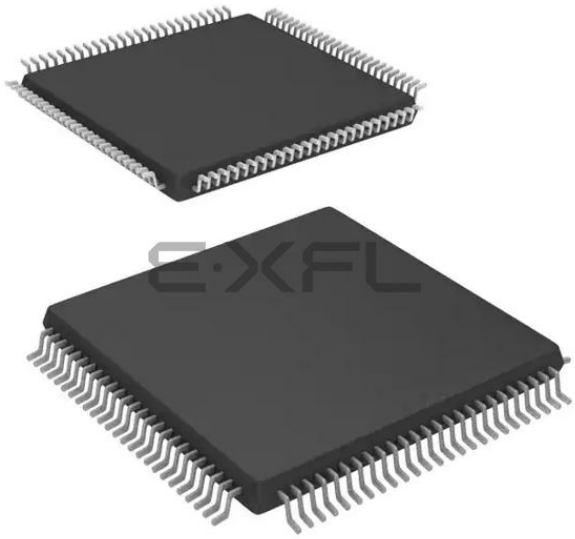

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Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2238bte13v

Pin No.		Pin Name				
TFP-100B TFP-100BV TFP-100G TFP-100GV FP-100B FP-100BV	TBP-112A*1 TBP-112AV*1	Mode 4	Mode 5	Mode 6	Mode 7	Flash Memory Programmable Mode*2
48	J8	P44/AN4	P44/AN4	P44/AN4	P44/AN4	NC
49	K9	P43/AN3	P43/AN3	P43/AN3	P43/AN3	NC
50	L10	P42/AN2	P42/AN2	P42/AN2	P42/AN2	NC
51	K10	P41/AN1	P41/AN1	P41/AN1	P41/AN1	NC
52	K11	P40/AN0	P40/AN0	P40/AN0	P40/AN0	NC
53	H8	Vref	Vref	Vref	Vref	VCC
54	J10	AVCC	AVCC	AVCC	AVCC	VCC
55	J11	MD0	MD0	MD0	MD0	VSS
56	H9	MD1	MD1	MD1	MD1	VSS
57	H10	OSC2	OSC2	OSC2	OSC2	NC
58	H11	OSC1	OSC1	OSC1	OSC1	VSS
59	G8	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
60	G9	NMI	NMI	NMI	NMI	VCC
61	G11	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	VCC
62	F9, G10	VCC	VCC	VCC	VCC	VCC
63	F11	XTAL	XTAL	XTAL	XTAL	XTAL
64	F8, F10	VSS	VSS	VSS	VSS	VSS
65	E11	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL
66	E10	FWE	FWE	FWE	FWE	FWE
67	E9	MD2	MD2	MD2	MD2	VSS
68	D11	PF7/ϕ	PF7/ϕ	PF7/ϕ	PF7/ϕ	NC
69	E8	$\overline{\text{AS}}$	$\overline{\text{AS}}$	$\overline{\text{AS}}$	PF6	NC
70	D10	$\overline{\text{RD}}$	$\overline{\text{RD}}$	$\overline{\text{RD}}$	PF5	NC
71	C11	$\overline{\text{HWR}}$	$\overline{\text{HWR}}$	$\overline{\text{HWR}}$	PF4	NC
72	D9	PF3/$\overline{\text{LWR}}$/ $\overline{\text{ADTRG}}$/ $\overline{\text{IRQ3}}$	PF3/$\overline{\text{LWR}}$/ $\overline{\text{ADTRG}}$/ $\overline{\text{IRQ3}}$	PF3/$\overline{\text{LWR}}$/ $\overline{\text{ADTRG}}$/ $\overline{\text{IRQ3}}$	PF3/ $\overline{\text{ADTRG}}$/ $\overline{\text{IRQ3}}$	NC
73	C10	PF2/$\overline{\text{WAIT}}$	PF2/$\overline{\text{WAIT}}$	PF2/$\overline{\text{WAIT}}$	PF2	NC
74	B11	PF1/$\overline{\text{BACK}}$/ BUZZ	PF1/$\overline{\text{BACK}}$/ BUZZ	PF1/$\overline{\text{BACK}}$/ BUZZ	PF1/BUZZ	NC
75	C9	PF0/$\overline{\text{BREQ}}$/ $\overline{\text{IRQ2}}$	PF0/$\overline{\text{BREQ}}$/ $\overline{\text{IRQ2}}$	PF0/$\overline{\text{BREQ}}$/ $\overline{\text{IRQ2}}$	PF0/$\overline{\text{IRQ2}}$	VCC

2.4.1 General Registers

The H8S/2000 CPU has eight 32-bit general registers. These general registers are all functionally alike and can be used as both address registers and data registers. When a general register is used as a data register, it can be accessed as a 32-bit, 16-bit, or 8-bit register. Figure 2.7 illustrates the usage of the general registers.

When the general registers are used as 32-bit registers or address registers, they are designated by the letters ER (ER0 to ER7).

The ER registers divide into 16-bit general registers designated by the letters E (E0 to E7) and R (R0 to R7). These registers are functionally equivalent, providing a maximum sixteen 16-bit registers. The E registers (E0 to E7) are also referred to as extended registers.

The R registers divide into 8-bit general registers designated by the letters RH (R0H to R7H) and RL (R0L to R7L). These registers are functionally equivalent, providing a maximum sixteen 8-bit registers.

The usage of each register can be selected independently.

General register ER7 has the function of stack pointer (SP) in addition to its general-register function, and is used implicitly in exception handling and subroutine calls. Figure 2.8 shows the stack.

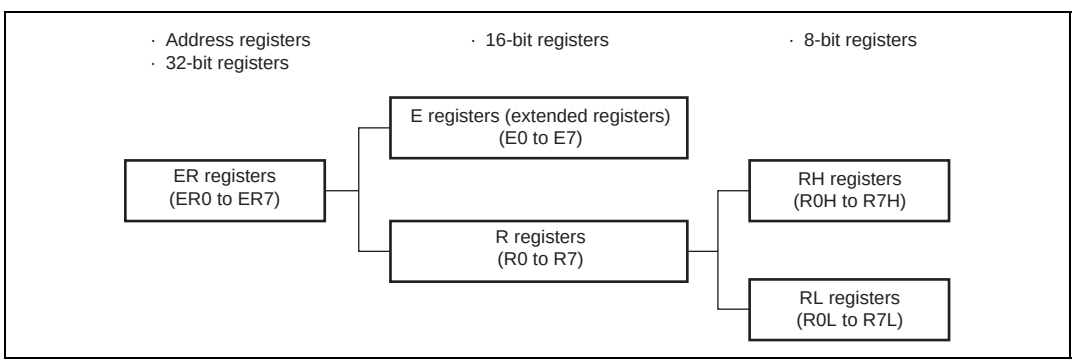

Figure 2.7 Usage of General Registers

7.3.6 Pin Function Control Register (PFCR)

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R/W	Reserved The write value should always be 0.
5	BUZZE	0	R/W	BUZZ Output Enable: This bit selects enabling or disabling of BUZZ output from pin PF1. WDT_1 input clock that is selected by PSS, and CKS2 to CKS0 bits is output as BUZZ signal. 0: PF1 input/output pin 1: BUZZ output pin
4	—	0	R/W	Reserved The write value should always be 0.
3	AE3	1/0*	R/W	Address Output Enable 3 to 0 These bits select enabling or disabling of address outputs A23 to A8 in ROMless extended mode and modes with ROM. When a pin is enabled for address output, the address is output regardless of the corresponding DDR setting. When a pin is disabled for address output, it becomes an output port when the corresponding DDR bit is set to 1. 0000: A23 to A8 output disabled 0001: A8 output enabled; A23 to A9 output disabled 0010: A9, A8 output enabled; A23 to A10 output disabled 0011: A10 to A8 output enabled; A23 to A11 output disabled 0100: A11 to A8 output enabled; A23 to A12 output disabled 0101: A12 to A8 output enabled; A23 to A13 output disabled 0110: A13 to A8 output enabled; A23 to A14 output disabled 0111: A14 to A8 output enabled; A23 to A15 output disabled 1000: A15 to A8 output enabled; A23 to A16 output disabled 1001: A16 to A8 output enabled; A23 to A17 output disabled 1010: A17 to A8 output enabled; A23 to A18 output disabled 1011: A18 to A8 output enabled; A23 to A19 output disabled 1100: A19 to A8 output enabled; A23 to A20 output disabled 1101: A20 to A8 output enabled; A23 to A21 output disabled 1110: A21 to A8 output enabled; A23, A22 output disabled 1111: A23 to A8 output enabled
2	AE2	1/0*	R/W	
1	AE1	0	R/W	
0	AE0	1/0*	R/W	

Note: * In modes 4 and 5, initial value of each bit is 1. In modes 6 and 7, initial value of each bit is 0.

16-Bit 3-State Access Space: Figures 7.15 to 7.17 show bus timings for a 16-bit 3-state access space. When a 16-bit access space is accessed , the upper half (D15 to D8) of the data bus is used for the even address, and the lower half (D7 to D0) for the odd address.

Wait states can be inserted.

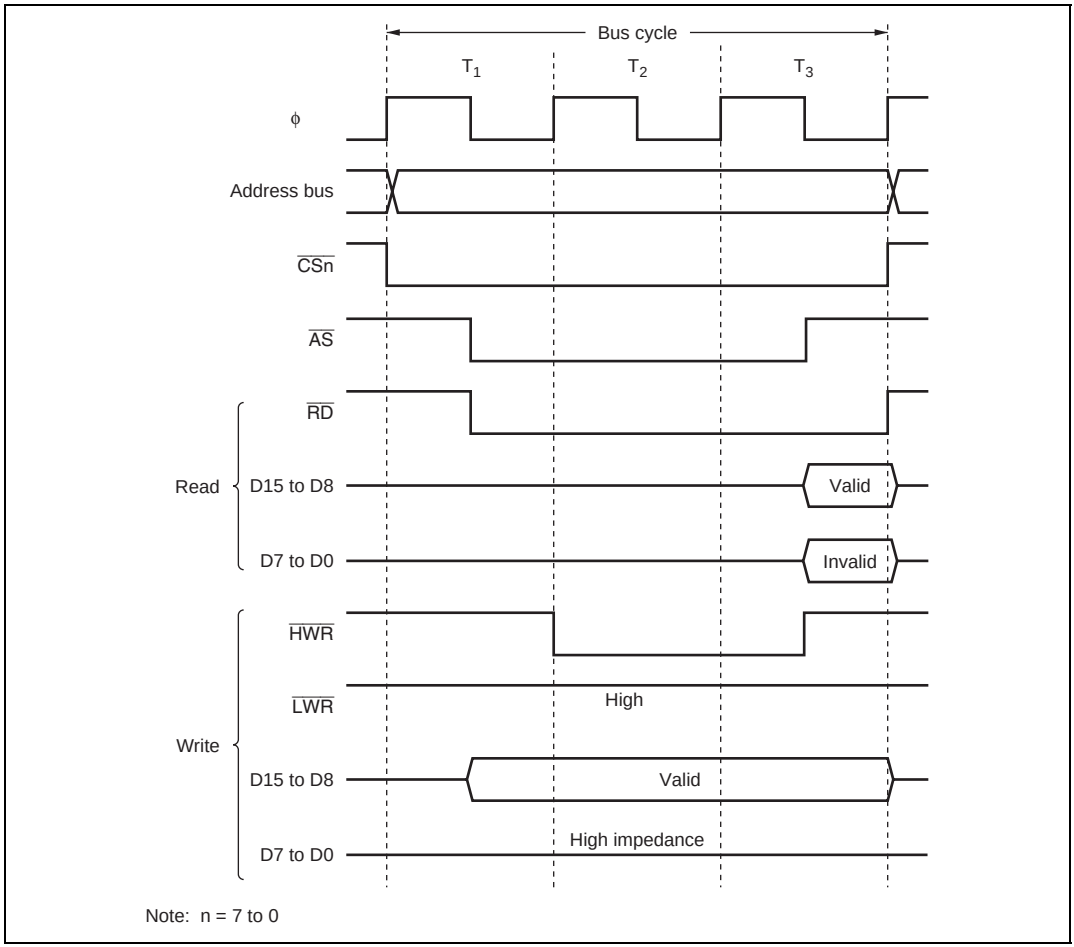

Figure 7.15 Bus Timing for 16-Bit 3-State Access Space (1) (Even Address Byte Access)

$\overline{\text{DREQ}}$ pin sampling is performed every cycle, with the rising edge of the next ϕ cycle after the end of the DMABCR write cycle for setting the transfer enabled state as the starting point.

When the $\overline{\text{DREQ}}$ pin low level is sampled while acceptance by means of the $\overline{\text{DREQ}}$ pin is possible, the request is held in the DMAC. Then, when activation is initiated in the DMAC, the request is cleared. After the end of the single cycle, acceptance resumes, $\overline{\text{DREQ}}$ pin low level sampling is performed again, and this operation is repeated until the transfer ends.

8.5.11 Multi-Channel Operation

The DMAC channel priority order is: channel 0 > channel 1, and channel A > channel B. Table 8.11 summarizes the priority order for DMAC channels.

Table 8.11 DMAC Channel Priority Order

Short Address Mode	Full Address Mode	Priority
Channel 0A	Channel 0	High
Channel 0B		↑
Channel 1A	Channel 1	
Channel 1B		Low

If transfer requests are issued simultaneously for more than one channel, or if a transfer request for another channel is issued during a transfer, when the bus is released, the DMAC selects the highest-priority channel from among those issuing a request according to the priority order shown in table 8.11. During burst transfer, or when one block is being transferred in block transfer, the channel will not be changed until the end of the transfer. Figure 8.33 shows a transfer example in which transfer requests are issued simultaneously for channels 0A, 0B, and 1.

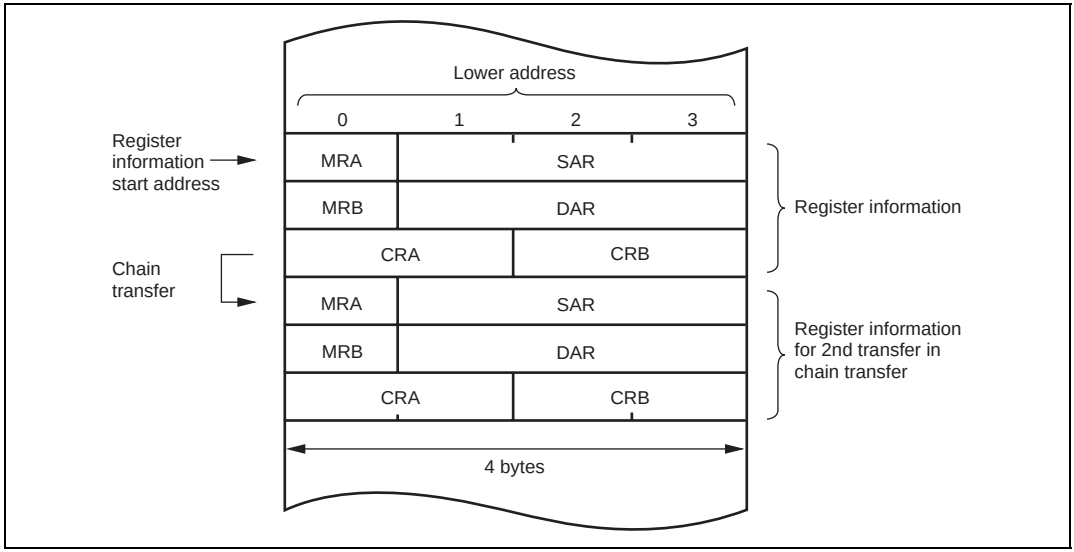

Figure 9.3 The Location of the DTC Register Information in the Address Space

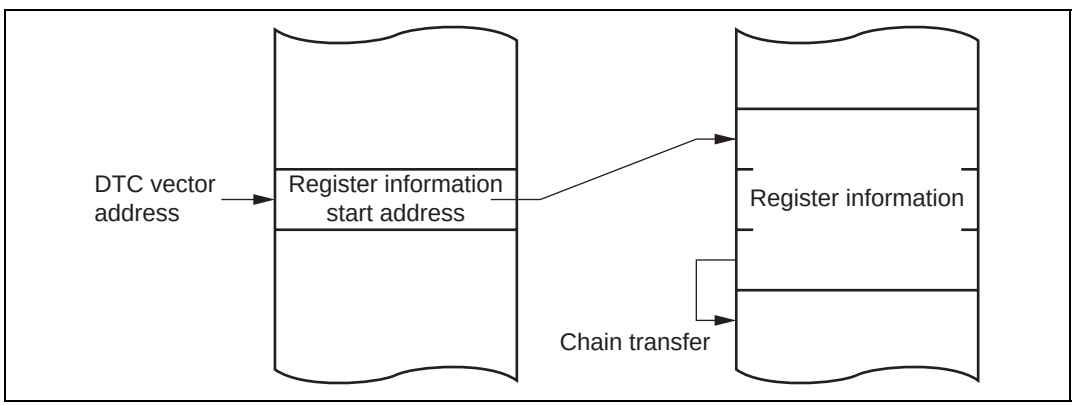

Figure 9.4 Correspondence between DTC Vector Address and Register Information

- P71/TMRI23/TMCI23/$\overline{\text{DREQ1}}$/$\overline{\text{CS5}}$

  The pin functions are switched as shown below according to the combination of operating mode and the P71DDR bit.

Operating mode	Modes 4 to 6		Mode 7	
P71DDR	0	1	0	1
Pin functions	P71 input pin	$\overline{\text{CS5}}$ output pin	P71 input pin	P71 output pin
	TMRI23*1, TMCI23*1, $\overline{\text{DREQ1}}$*2 input pin	—	TMRI23*1, TMCI23*1, $\overline{\text{DREQ1}}$*2 input pin	

Notes: 1. Not available in the H8S/2237 Group and H8S/2227 Group.
2. Supported only by the H8S/2239 Group.

- P70/TMRI01/TMCI01/$\overline{\text{DREQ0}}$/$\overline{\text{CS4}}$

  The pin functions are switched as shown below according to the combination of operating mode and the P70DDR bit.

Operating mode	Modes 4 to 6		Mode 7	
P70DDR	0	1	0	1
Pin functions	P70 input pin	$\overline{\text{CS4}}$ output pin	P70 input pin	P70 output pin
	TMRI01,TMCI01, $\overline{\text{DREQ0}}$* input pin	—	TMRI01,TMCI01, $\overline{\text{DREQ0}}$* input pin	

Note: * Supported only by the H8S/2239 Group.

- PA0/A16

  The pin functions are switched as shown below according to the combination of operating mode, AE3 to AE0 bits in PFCR and the PA0DDR bit.

Operating mode	Modes 4 to 6			Mode 7	
AE3 to AE0	Other than (B'0xxx or B'1000)	B'0xxx or B'1000		—	
PA0DDR	—	0	1	0	1
Pin functions	A16 output pin	PA0 input pin	PA0 output pin*	PA0 input pin	PA0 output pin*

Note: * When PA0ODR in PAODR is set to 1, the corresponding pin functions as NMOS open drain output.

10.6.7 Input Pull-Up MOS States in Port A

Port A has a built-in input pull-up MOS function that can be controlled by software. Input pull-up MOS can be specified as on or off on an individual bit basis.

Table 10.2 summarizes the input pull-up MOS states.

Table 10.2 Input Pull-Up MOS States in Port A

Pin States	Power-on Reset	Hardware Standby Mode	Manual Reset	Software Standby Mode	In Other Operations
Address output, Port output, SCI output	OFF	OFF	OFF	OFF	OFF
Port input, SCI input			ON/OFF	ON/OFF	ON/OFF

Legend:

OFF: Input pull-up MOS is always off.

ON/OFF: On when PADDR = 0 and PAPCR = 1; otherwise off.

10.7 Port B

Port B is a 8-bit I/O port. Port B has the following registers.

- Port B data direction register (PBDDR)
- Port B data register (PBDR)
- Port B register (PORTB)

- PB5/A13/TIOCB4

  The pin functions are switched as shown below according to the combination of operating mode, the TPU channel 4[*3] setting, AE3 to AE0 bits in PFCR, and the PB5DDR bit.

Operating mode	Modes 4 to 6				Mode 7		
AE3 to AE0	B'011x or B'1xxx	Other than (B'011x or B'1xxx)			—		
TPU channel 4 setting[*1*3]	—	Output	Input or initial value		Output	Input or initial value	
PB5DDR	—	—	0	1	—	0	1
Pin functions	A13 output pin	TIOCB4[*3] output pin	PB5 input pin	PB5 output pin	TIOCB4[*3] output pin	PB5 input pin	PB5 output pin
			TIOCB4[*3] input pin[*2]			TIOCB4[*3] input pin[*2]	

Notes: 1. For the setting of the TPU channel, see section 11, 16-Bit Timer Pulse Unit (TPU).
2. This pin functions as TIOCB4 input when TPU channel 4 timer operating mode is set to normal operating or phase counting mode and IOB3 to IOB0 in TIOR_4 are set to 10xx.
3. Not available in the H8S/2227 Group.

- PB4/A12/TIOCA4

  The pin functions are switched as shown below according to the combination of operating mode, the TPU channel 4[*3] setting, AE3 to AE0 bits in PFCR, and the PB4DDR bit.

Operating mode	Modes 4 to 6				Mode 7		
AE3 to AE0	Other than (B'0100 or B'00xx)	B'0100 or B'00xx			—		
TPU channel 4 setting[*1*3]	—	Output	Input or initial value		Output	Input or initial value	
PB4DDR	—	—	0	1	—	0	1
Pin functions	A12 output pin	TIOCA4[*3] output pin	PB4 input pin	PB4 output pin	TIOCA4[*3] output pin	PB4 input pin	PB4 output pin
			TIOCA4[*3] input pin[*2]			TIOCA4[*3] input pin[*2]	

Notes: 1. For the setting of the TPU channel, see section 11, 16-Bit Timer Pulse Unit (TPU).
2. This pin functions as TIOCA4 input when TPU channel 4 timer operating mode is set to normal operating or phase counting mode and IOA3 to IOA0 in TIOR_4 are set to 10xx.
3. Not available in the H8S/2227 Group.

Example of PWM Mode Setting Procedure: Figure 11.21 shows an example of the PWM mode setting procedure.

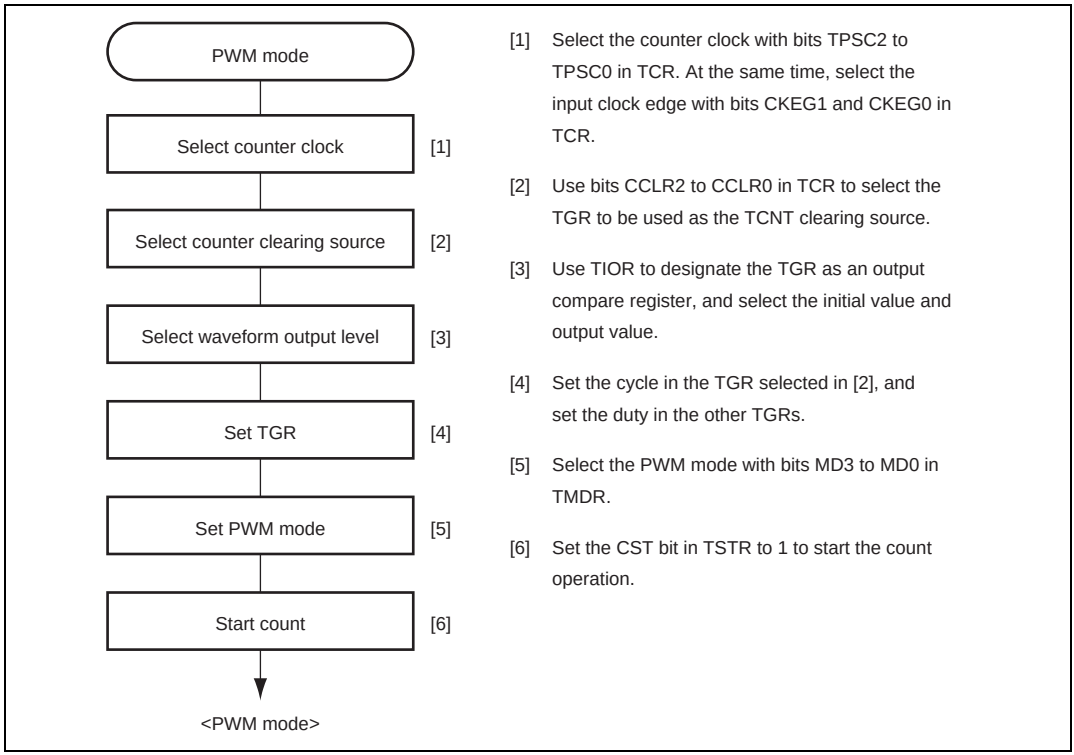

Figure 11.21 Example of PWM Mode Setting Procedure

Examples of PWM Mode Operation: Figure 11.22 shows an example of PWM mode 1 operation.

In this example, TGRA compare match is set as the TCNT clearing source, 0 is set for the TGRA initial output value and output value, and 1 is set as the TGRB output value.

In this case, the value set in TGRA is used as the cycle, and the values set in TGRB registers as the duty cycle.

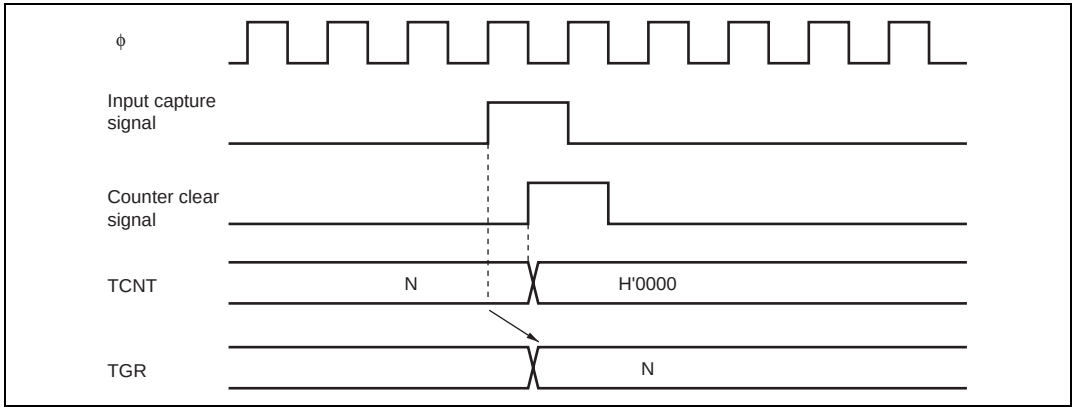

Figure 11.36 Counter Clear Timing (Input Capture)

Buffer Operation Timing: Figures 11.37 and 11.38 show the timings in buffer operation.

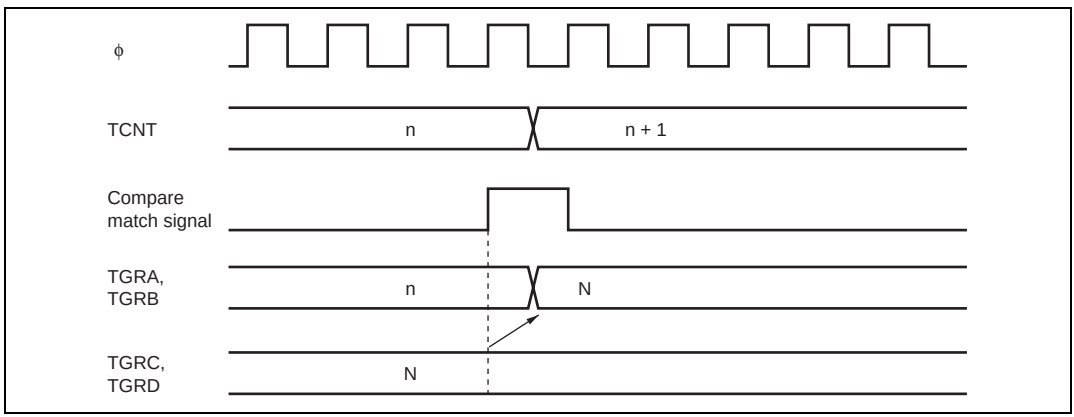

Figure 11.37 Buffer Operation Timing (Compare Match)

13.6.3 Changing Value of PSS or CKS2 to CKS0

If the PSS or CKS0 to CKS2 bits in TCSR are written to while the WDT is operating, errors could occur in the incrementation. Software must be used to stop the watchdog timer (by clearing the TME bit to 0) before changing the value of the PSS or CKS0 to CKS2 bits.

13.6.4 Switching between Watchdog Timer Mode and Interval Timer Mode

If the mode is switched from watchdog timer to interval timer while the WDT is operating, errors could occur in the incrementation. Software must be used to stop the watchdog timer (by clearing the TME bit to 0) before switching the mode.

13.6.5 Internal Reset in Watchdog Timer Mode

This LSI is not reset internally if TCNT overflows while the RSTE bit is cleared to 0 during watchdog timer operation, however TCNT_0 and TCSR_0 of the WDT_0 are reset.

TCNT, TCSR, or RSTCR cannot be written to for 132 states following an overflow. During this period, any attempt to read the WOVF flag is not acknowledged. Accordingly, wait 132 states after overflow to write 0 to the WOVF flag for clearing.

13.6.6 OVF Flag Clearing in Interval Timer Mode

When the OVF flag setting conflicts with the OVF flag reading in interval timer mode, writing 0 to the OVF bit may not clear the flag even though the OVF bit has been read while it is 1. If there is a possibility that the OVF flag setting and reading will conflict, such as when the OVF flag is polled with the interval timer interrupt disabled, read the OVF bit while it is 1 at least twice before writing 0 to the OVF bit to clear the flag.

13.6.7 Notes on Initializing TCNT by Using the TME Bit

When the ϕSUB (subckock) division clock is selected as the TCNT input clock (PSS in TCSR set to 1) and, after TME in TCSR is cleared to 0 to initialize the counter (TCNT) while the counter (TCNT) is operating in the high-speed mode or medium-speed mode, TCNT is restarted by setting TME to 1 once again, TCNT may not be correctly initialized.

In such cases, use either of the following methods to initialize TCNT:

(1) Write H'00 to TCNT.

(2) In subactive mode, clear the TME bit to 0.

Table 15.5 Maximum Bit Rate with External Clock Input (Asynchronous Mode)

ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (kbps)	ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (kbps)
2[*2]	0.5000	31.25	9.8304[*2]	2.4576	153.6
2.097152[*2]	0.5243	32.768	10	2.5000	156.25
2.4576[*2]	0.6144	38.4	12	3.0000	187.5
3[*2]	0.7500	46.875	12.288	3.0720	192.0
3.6864[*2]	0.9216	57.6	14[*1]	3.5000	218.75
4[*2]	1.0000	62.5	14.7456[*1]	3.6864	230.4
4.9152[*2]	1.2288	76.8	16[*1]	4.0000	250.0
5[*2]	1.2500	78.125	17.2032[*1]	4.3008	268.8
6[*2]	1.5000	93.75	18[*1]	4.5000	281.3
6.144[*2]	1.5360	96.0	19.6608[*1]	4.9152	307.2
7.3728[*2]	1.8432	115.2	20[*1]	5.0000	312.5
8[*2]	2.0000	125.0			

Notes: 1. Supported only by the H8S/2239 Group.
2. The H8S/2258 Group is out of operation.

15.6.5 Simultaneous Serial Data Transmission and Reception (Clocked Synchronous Mode)

Figure 15.23 shows a sample flowchart for simultaneous serial transmit and receive operations. The following procedure should be used for simultaneous serial data transmit and receive operations. To switch from transmit mode to simultaneous transmit and receive mode, after checking that the SCI has finished transmission and the TDRE and TEND flags are set to 1, clear TE to 0. Then simultaneously set TE and RE to 1 with a single instruction. To switch from receive mode to simultaneous transmit and receive mode, after checking that the SCI has finished reception, clear RE to 0. Then after checking that the RDRF and receive error flags (ORER, FER, and PER) are cleared to 0, simultaneously set TE and RE to 1 with a single instruction.

17.5.4 External Trigger Input Timing

A/D conversion can be externally triggered. When the TRGS0 and TRGS1 bits are set to 11 in ADCR, external trigger input is enabled at the $\overline{\text{ADTRG}}$ pin. A falling edge at the $\overline{\text{ADTRG}}$ pin sets the ADST bit to 1 in ADCSR, starting A/D conversion. Other operations, in both single and scan modes, are the same as when the bit ADST has been set to 1 by software. Figure 17.6 shows the timing.

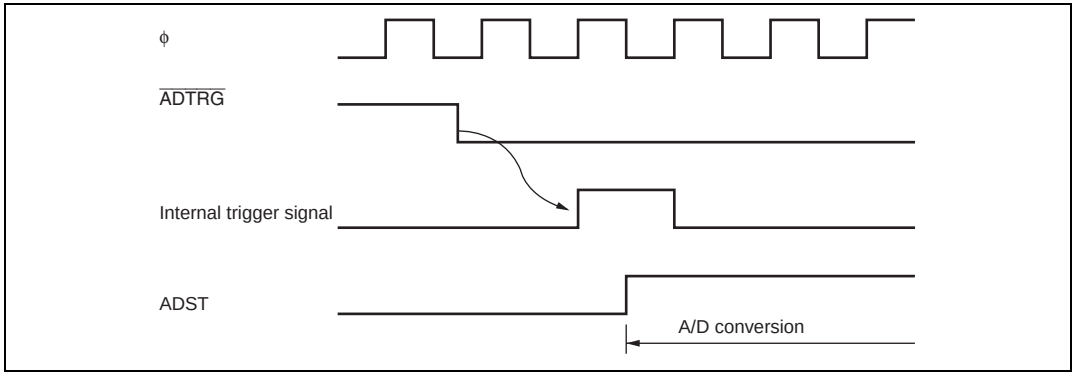

Figure 17.6 External Trigger Input Timing

17.6 Interrupt Source

The A/D converter generates an A/D conversion end interrupt (ADI) at the end of A/D conversion. Setting the ADIE bit to 1 enables ADI interrupt requests while the bit ADF in ADCSR is set to 1 after A/D conversion is completed. The DMAC* and the DTC can be activated by an ADI interrupt. Having the converted data read by the DMAC* or the DTC in response to an ADI interrupt enables continuous conversion without imposing a load on software.

Note: * Supported only by the H8S/2239 Group.

Table 17.5 A/D Converter Interrupt Source

Name	Interrupt Source	Interrupt Source Flag	DTC Activation	DMAC* Activation
ADI	A/D conversion completed	ADF	Possible	Possible

Note: * Supported only by the H8S/2239 Group.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TGRB_2	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	TPU_2
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
DMAWER	—	—	—	—	WE1B	WE1A	WE0B	WE0A	DMAC
DMATCR	—	—	TEE1	TEE0	—	—	—	—	
DMACR_0A*2	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	
DMACR_0A*3	DTSZ	SAID	SAIDE	BLKDIR	BLKE	—	—	—	
DMACR_0B*2	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	
DMACR_0B*3	—	DAID	DAIDE	—	DTF3	DTF2	DTF1	DTF0	
DMACR_1A*2	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	
DMACR_1A*3	DTSZ	SAID	SAIDE	BLKDIR	BLKE	—	—	—	
DMACR_1B*2	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	
DMACR_1B*3	—	DAID	DAIDE	—	DTF3	DTF2	DTF1	DTF0	
DMABCRH*2	FAE1	FAE0	SAE1	SAE0	DTA1B	DTA1A	DTA0B	DTA0A	
DMABCRH*3	FAE1	FAE0	—	—	DTA1	—	DTA0	—	
DMABCRL*2	DTE1B	DTE1A	DTE0B	DTE0A	DTIE1B	DTIE1A	DTIE0B	DTIE0A	
DMABCRL*3	DTME1	DTE1	DTME0	DTE0	DTIE1B	DTIE1A	DTIE0B	DTIE0A	
TCR_0	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR_0
TCR_1	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR_1
TCSR_0	CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0	TMR_0
TCSR_1	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0	TMR_1
TCORA_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	TMR_0
TCORA_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	TMR_1
TCORB_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	TMR_0
TCORB_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	TMR_1
TCNT_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	TMR_0
TCNT_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	TMR_1
TCSR_0	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0	WDT_0
TCNT_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
RSTCSR	WOVF	RSTE	RSTS	—	—	—	—	—	
SMR_0*1	C/$\overline{A}$ (GM)	CHR (BLK)	PE (PE)	O/$\overline{E}$ (O/$\overline{E}$)	STOP (BCP1)	MP (BCP0)	CKS1 (CKS1)	CKS0 (CKS0)	SCI_0

26.3 Register States in Each Operating Mode

Register Name	Reset	Manual Reset	High-speed	Medium-speed	Sleep	Module Stop	Watch	Sub-active	Sub-sleep	Software Standby	Hardware Standby	Module
MRA	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	DTC
SAR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
MRB	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
DAR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
CRA	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
CRB	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IECTR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	IEB
IECMR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IEMCR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IEAR1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IEAR2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IESA1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IESA2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IETBFL	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IETBR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IEMA1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IEMA2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IERCTL	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IERBFL	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IERBR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IELA1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IELA2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IEFLG	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IETSR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IEIET	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IETEF	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IERSR	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IEIER	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IEREF	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	

Table 27.3 Permissible Output Current

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{ref} = 4.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	SCL1, SCL0, SDA1, SDA0	V_{CC} = 4.0 V to 5.5 V	I_{OL}	—	—	10	mA
	Output pins other than above ones			—	—	1.0	
Permissible output low current (total)	Total of all output pins*	V_{CC} = 4.0 V to 5.5 V	$\sum I_{OL}$	—	—	60	mA
Permissible output high current (per pin)	All output pins	V_{CC} = 4.0 V to 5.5 V	$-I_{OH}$	—	—	1.0	mA
Permissible output high current (total)	Total of all output pins	V_{CC} = 4.0 V to 5.5 V	$\sum -I_{OH}$	—	—	30	mA

Note: * To protect chip reliability, do not exceed the output current values in table 27.3.

Table B.2 Product Codes of H8S/2239 Group

Product Type			Product Code	Mark Code	Package (Package Code)
H8S/2239	Flash memory version	Standard product	HD64F2239	HD64F2239TE20	100-pin TQFP (TFP-100B)
				HD64F2239TF20	100-pin TQFP (TFP-100G)
				HD64F2239FA20	100-pin QFP (FP-100B)
				HD64F2239BQ20	112-pin TFBGA (TBP-112A)
				HD64F2239TE16	100-pin TQFP (TFP-100B)
				HD64F2239TF16	100-pin TQFP (TFP-100G)
				HD64F2239FA16	100-pin QFP (FP-100B)
				HD64F2239BQ16	112-pin TFBGA (TBP-112A)
	Masked ROM version	Standard product	HD6432239	HD6432239(***)TE	100-pin TQFP (TFP-100B)
				HD6432239(***)TF	100-pin TQFP (TFP-100G)
				HD6432239(***)FA	100-pin QFP (FP-100B)
		On-chip I^2C bus interface product	HD6432239W	HD6432239W(***)TE	100-pin TQFP (TFP-100B)
				HD6432239W(***)TF	100-pin TQFP (TFP-100G)
				HD6432239W(***)FA	100-pin QFP (FP-100B)

Legend:

(***): ROM code

Note: A standard product of F-ZTAT version includes an I^2C bus interface.
Please contact Renesas Technology agency to confirm the current status of each product.