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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2238rbr13v

Pin No.		Pin Name				
TFP-100B FP-100B	FP-100A	Mode 4	Mode 5	Mode 6	Mode 7	Flash Memory Programmable Mode*
49	52	P43/AN3	P43/AN3	P43/AN3	P43/AN3	NC
50	53	P42/AN2	P42/AN2	P42/AN2	P42/AN2	NC
51	54	P41/AN1	P41/AN1	P41/AN1	P41/AN1	NC
52	55	P40/AN0	P40/AN0	P40/AN0	P40/AN0	NC
53	56	Vref	Vref	Vref	Vref	VCC
54	57	AVCC	AVCC	AVCC	AVCC	VCC
55	58	MD0	MD0	MD0	MD0	VSS
56	59	MD1	MD1	MD1	MD1	VSS
57	60	OSC2	OSC2	OSC2	OSC2	NC
58	61	OSC1	OSC1	OSC1	OSC1	VSS
59	62	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
60	63	NMI	NMI	NMI	NMI	VCC
61	64	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	VCC
62	65	VCC	VCC	VCC	VCC	VCC
63	66	XTAL	XTAL	XTAL	XTAL	XTAL
64	67	VSS	VSS	VSS	VSS	VSS
65	68	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL
66	69	FWE	FWE	FWE	FWE	FWE
67	70	MD2	MD2	MD2	MD2	VSS
68	71	PF7/ϕ	PF7/ϕ	PF7/ϕ	PF7/ϕ	NC
69	72	$\overline{\text{AS}}$	$\overline{\text{AS}}$	$\overline{\text{AS}}$	PF6	NC
70	73	$\overline{\text{RD}}$	$\overline{\text{RD}}$	$\overline{\text{RD}}$	PF5	NC
71	74	$\overline{\text{HWR}}$	$\overline{\text{HWR}}$	$\overline{\text{HWR}}$	PF4	NC
72	75	PF3/$\overline{\text{LWR}}$/ $\overline{\text{ADTRG}}$/$\overline{\text{IRQ3}}$	PF3/$\overline{\text{LWR}}$/ $\overline{\text{ADTRG}}$/$\overline{\text{IRQ3}}$	PF3/$\overline{\text{LWR}}$/ $\overline{\text{ADTRG}}$/$\overline{\text{IRQ3}}$	PF3/$\overline{\text{ADTRG}}$/ $\overline{\text{IRQ3}}$	NC
73	76	PF2/$\overline{\text{WAIT}}$	PF2/$\overline{\text{WAIT}}$	PF2/$\overline{\text{WAIT}}$	PF2	NC
74	77	PF1/$\overline{\text{BACK}}$/ BUZZ	PF1/$\overline{\text{BACK}}$/ BUZZ	PF1/$\overline{\text{BACK}}$/ BUZZ	PF1/BUZZ	NC
75	78	PF0/$\overline{\text{BREQ}}$/ $\overline{\text{IRQ2}}$	PF0/$\overline{\text{BREQ}}$/ $\overline{\text{IRQ2}}$	PF0/$\overline{\text{BREQ}}$/ $\overline{\text{IRQ2}}$	PF0/$\overline{\text{IRQ2}}$	VCC
76	79	P30/TxD0	P30/TxD0	P30/TxD0	P30/TxD0	NC
77	80	P31/RxD0	P31/RxD0	P31/RxD0	P31/RxD0	NC

A block diagram of the interrupt controller is shown in figure 5.1.

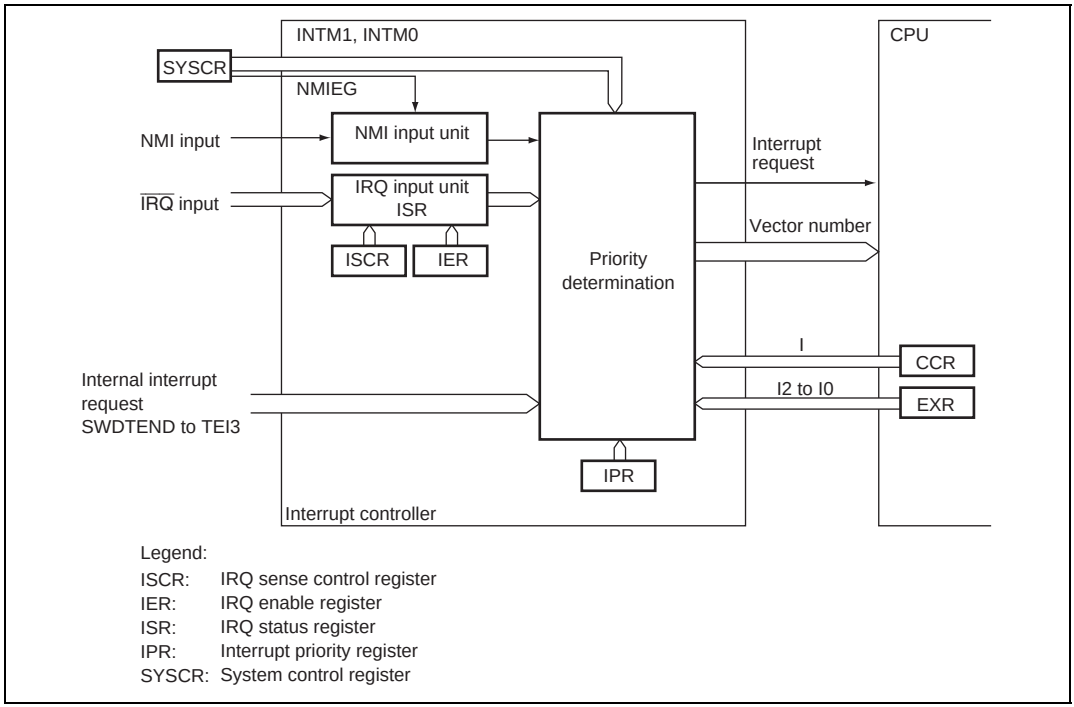

Figure 5.1 Block Diagram of Interrupt Controller

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*1 Advanced Mode	IPR*2	Priority
8-bit timer channel 3*4	CMIA3 (compare-match A3)	96	H'0180	IPRL6 to IPRL4	High
	CMIB3 (compare-match B3)	97	H'0184		
	OVI3 (overflow 3)	98	H'0188		
—	Reserved	99	H'018C		
IIC channel 0*4 (option)	IICI0 (1-byte transmission/ reception completion)	100	H'0190	IPRL2 to IPRL0	
	Reserved	101	H'0194		
IIC channel 1*4 (option)	IICI1 (1-byte transmission/ reception completion)	102	H'0198	IPRL2 to IPRL0	
	Reserved	103	H'019C		
IEB*6	IEBSI (receive status)	104	H'01A0	IPRM6 to IPRM4	
	IERxI (RxRDY)	105	H'01A4		
	IETxI (TxRDY)	106	H'01A8		
	TETSI (transmit status)	107	H'01AC		
SCI channel 3	ERI3 (receive error 3)	120	H'01E0	IPRO6 to IPRO4	
	RXI3 (receive completion 3)	121	H'01E4		
	TXI3 (transmit data empty 3)	122	H'01E8		
	TEI3 (transmit end)	123	H'01EC		Low

Notes: 1. Lower 16 bits of the start address.
2. IPR6 to IPR4, and IPR2 to IPR0 bits are reserved, because these bits have no corresponding interruption. These bits are always read as 0 and cannot be modified.
3. Not available in the H8S/2227 Group.
4. Not available in the H8S/2237 Group and H8S/2227 Group.
5. Supported only by the H8S/2239 Group.
6. Supported only by the H8S/2258 Group.

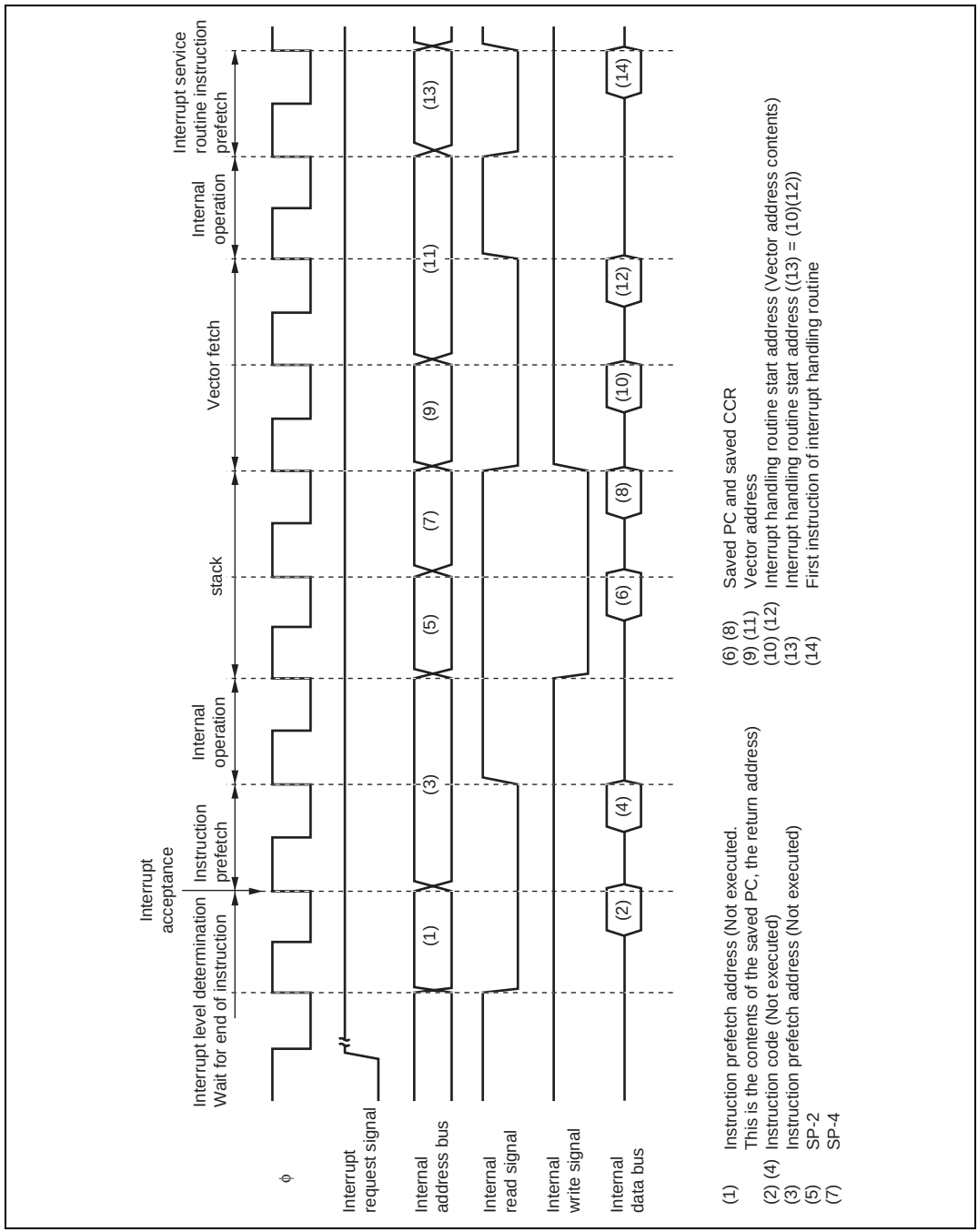

Figure 5.7 Interrupt Exception Handling

Rn as its addressing mode, and that instruction is located in on-chip ROM or RAM, the instruction will be one state later than in normal operation.

6.4 Usage Notes

6.4.1 Module Stop Mode Setting

PBC operation can be disabled or enabled using the module stop control register. The initial setting is for PBC operation to be halted. Register access is enabled by clearing module stop mode. For details, refer to section 24, Power-Down Modes.

6.4.2 PC Break Interrupts

The PC break interrupt is shared by channels A and B. The channel from which the request was issued must be determined by the interrupt handler.

6.4.3 CMFA and CMFB

The CMFA and CMFB flags are not automatically cleared to 0, so 0 must be written to CMFA or CMFB after first reading the flag while it is set to 1. If the flag is left set to 1, another interrupt will be requested after interrupt handling ends.

6.4.4 PC Break Interrupt when DTC and DMAC* Is Bus Master

A PC break interrupt generated when the DTC and DMAC* is the bus master is accepted after the bus has been transferred to the CPU by the bus controller.

Note: * Supported only by the H8S/2239 Group.

6.4.5 PC Break Set for Instruction Fetch at Address Following BSR, JSR, JMP, TRAPA, RTE, and RTS Instruction

Even if the instruction at the address following a BSR, JSR, JMP, TRAPA, RTE, or RTS instruction is fetched, it is not executed, and so a PC break interrupt is not generated by the instruction fetch at the next address.

Only the basic bus interface can be used for the area 7.

7.4.4 Chip Select Signals

This LSI can output chip select signals ($\overline{CS7}$ to $\overline{CS0}$) to areas 7 to 0, the signal being driven low when the corresponding external space area is accessed. Figure 7.3 shows an example of $\overline{CSn}$ (n = 7 to 0) output timing. Enabling or disabling of the $\overline{CSn}$ signal is performed by setting the data direction register (DDR) for the port corresponding to the particular $\overline{CSn}$ pin.

In ROM-disabled extended mode, the $\overline{CS0}$ pin is placed in the output state after a power-on reset. Pins $\overline{CS7}$ to $\overline{CS1}$ are placed in the input state after a power-on reset, and so the corresponding DDR should be set to 1 when outputting signals $\overline{CS7}$ to $\overline{CS1}$.

In ROM-enabled extended mode, pins $\overline{CS7}$ to $\overline{CS0}$ are all placed in the input state after a power-on reset, and so the corresponding DDR should be set to 1 when outputting signals $\overline{CS7}$ to $\overline{CS0}$. For details, see section 10, I/O Ports.

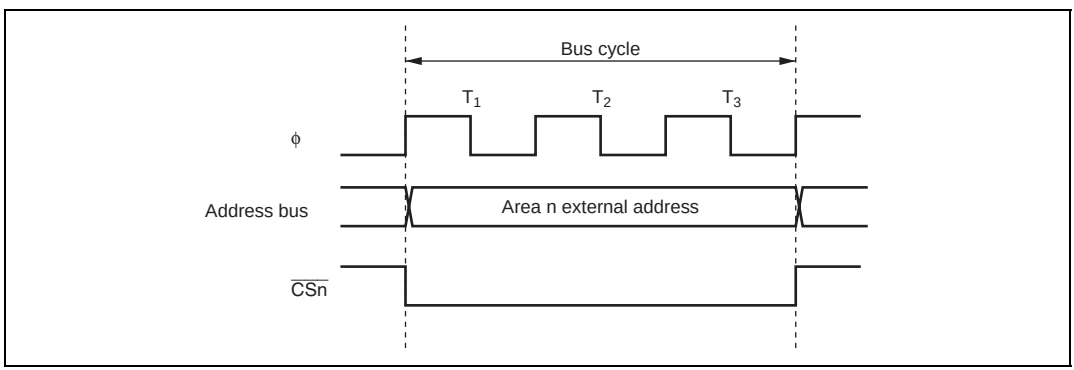

Figure 7.3 $\overline{CSn}$ Signal Output Timing (n = 0 to 7)

7.5 Basic Timing

The CPU is driven by a system clock (ϕ), denoted by the symbol ϕ. The period from one rising edge of ϕ to the next is referred to as a “state”. The memory cycle or bus cycle consists of one, two, or three states. Different methods are used to access on-chip memory, on-chip peripheral modules, and the external address space.

Bit	Bit Name	Initial Value	R/W	Description
11	DTA1B	0	R/W	Data Transfer Acknowledge 1B
10	DTA1A	0	R/W	Data Transfer Acknowledge 1A
9	DTA0B	0	R/W	Data Transfer Acknowledge 0B
8	DTA0A	0	R/W	Data Transfer Acknowledge 0A These bits enable or disable clearing when DMA transfer is performed for the internal interrupt source selected by the DTF3 to DTF0 bits in DMACR. It the DTA bit is set to 1 when DTE = 1, the internal interrupt source is cleared automatically by DMA transfer. When DTE = 1 and DTA = 1, the internal interrupt source does not issue an interrupt request to the CPU or DTC. If the DTA bit is cleared to 0 when DTE = 1, the internal interrupt source is not cleared when a transfer is performed, and can issue an interrupt request to the CPU or DTC in parallel. In this case, the interrupt source should be cleared by the CPU or DTC transfer. When DTE = 0, the internal interrupt source issues an interrupt request to the CPU or DTC regardless of the DTA bit setting. 0: Clearing is disabled when DMA transfer is performed for the selected internal interrupt source 1: Clearing is enabled when DMA transfer is performed for the selected internal interrupt source

Bit	Bit Name	Initial value	R/W	Description
2	TGIEC	0	R/W	TGR Interrupt Enable C Enables or disables interrupt requests (TGIC) by the TGFC bit when the TGFC bit in TSR is set to 1 in channels 0 and 3*. In channels 1, 2, 4*, and 5*, bit 2 is reserved. It is always read as 0 and cannot be modified. 0: Interrupt requests (TGIC) by TGFC bit disabled 1: Interrupt requests (TGIC) by TGFC bit enabled
1	TGIEB	0	R/W	TGR Interrupt Enable B Enables or disables interrupt requests (TGIB) by the TGFB bit when the TGFB bit in TSR is set to 1. 0: Interrupt requests (TGIB) by TGFB bit disabled 1: Interrupt requests (TGIB) by TGFB bit enabled
0	TGIEA	0	R/W	TGR Interrupt Enable A Enables or disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1. 0: Interrupt requests (TGIA) by TGFA bit disabled 1: Interrupt requests (TGIA) by TGFA bit enabled

Note: * Not available in the H8S/2227 Group.

Bit	Bit Name	Initial value	R/W	Description
3	TGFD	0	R/(W)*1	Input Capture/Output Compare Flag D Status flag that indicates the occurrence of TGRD input capture or compare match in channels 0 and 3*3. In channels 1, 2, 4*3, and 5*3, bit 3 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register [Clearing conditions] • When DTC is activated by TGID interrupt while DISEL bit of MRB in DTC is 0 with the transfer counter not being 0 • When 0 is written to TGFD after reading TGFD = 1
2	TGFC	0	R/(W)*1	Input Capture/Output Compare Flag C Status flag that indicates the occurrence of TGRC input capture or compare match in channels 0 and 3*3. In channels 1, 2, 4*3, and 5*3, bit 2 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register [Clearing conditions] • When DTC is activated by TGIC interrupt while DISEL bit of MRB in DTC is 0 with the transfer counter not being 0 • When 0 is written to TGFC after reading TGFC = 1

Input Capture Function: The TCNT value can be transferred to TGR on detection of the TIOC pin input edge.

Rising edge, falling edge, or both edges can be selected as the detection edge. For channels 0, 1, 3*, and 4*, it is also possible to specify another channel's counter input clock or compare match signal as the input capture source.

Notes: When another channel's counter input clock is used as the input capture input for channels 0 and 3, $\phi/1$ should not be selected as the counter input clock used for input capture input. Input capture will not be generated if $\phi/1$ is selected.

* Not available in the H8S/2227 Group.

1. Example of setting procedure for input capture operation

   Figure 11.9 shows an example of the setting procedure for input capture operation.

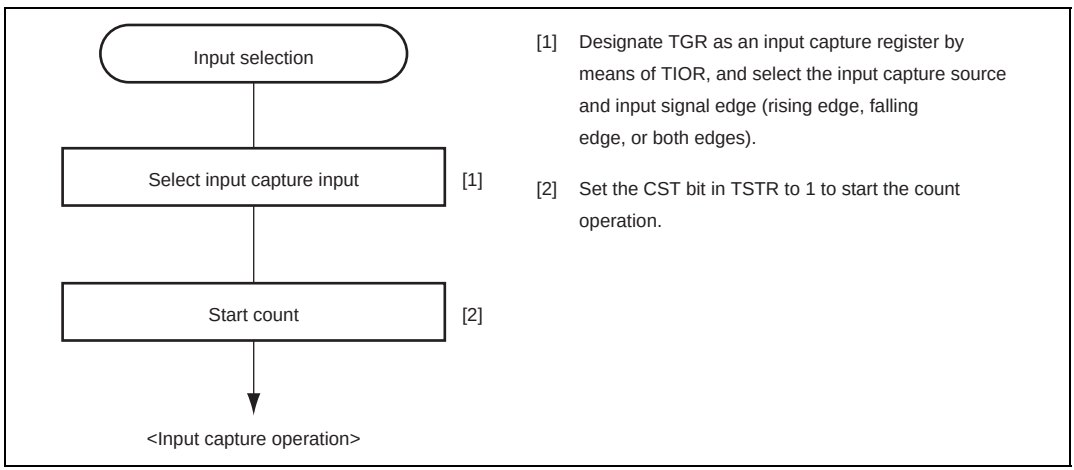

Figure 11.9 Example of Setting Procedure for Input Capture Operation

2. Example of input capture operation

   Figure 11.10 shows an example of input capture operation.

   In this example both rising and falling edges have been selected as the TIOCA pin input capture input edge, falling edge has been selected as the TIOCB pin input capture input edge, and counter clearing by TGRB input capture has been designated for TCNT.

For details on PWM modes, see section 11.4.5, PWM Modes.

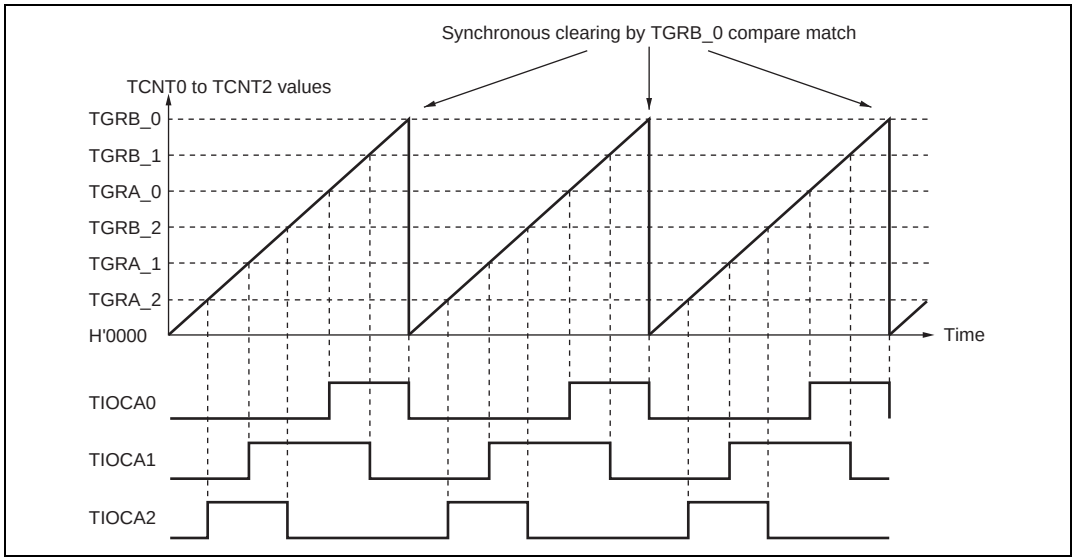

Figure 11.12 Example of Synchronous Operation

11.4.3 Buffer Operation

Buffer operation, provided for channels 0 and 3, enables TGRC and TGRD to be used as buffer registers.

Buffer operation differs depending on whether TGR has been designated as an input capture register or a compare match register.

Table 11.28 shows the register combinations used in buffer operation.

Table 11.28 Register Combinations in Buffer Operation

Channel	Timer General Register	Buffer Register
0	TGRA_0	TGRC_0
	TGRB_0	TGRD_0
3*	TGRA_3	TGRC_3
	TGRB_3	TGRD_3

Note: * Not available in the H8S/2227 Group.

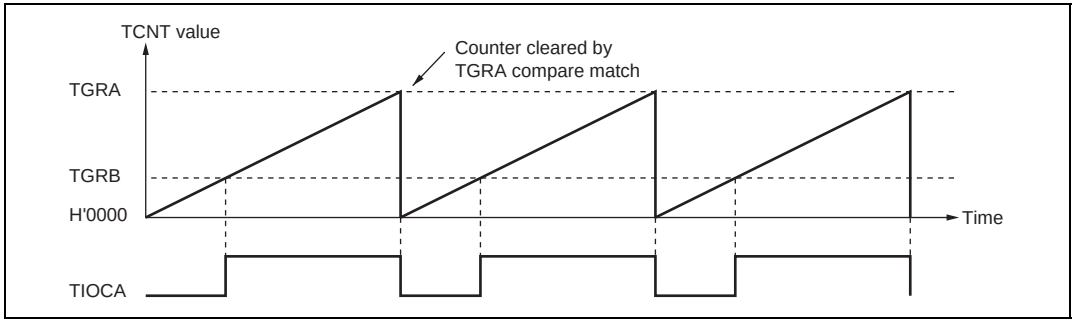

Figure 11.22 Example of PWM Mode Operation (1)

Figure 11.23 shows an example of PWM mode 2 operation.

In this example, synchronous operation is designated for channels 0 and 1, TGRB_1 compare match is set as the TCNT clearing source, and 0 is set for the initial output value and 1 for the output value of the other TGR registers (TGRA_0 to TGRD_0, TGRA_1), to output a 5-phase PWM waveform.

In this case, the value set in TGRB_1 is used as the cycle, and the values set in the other TGRs as the duty cycle.

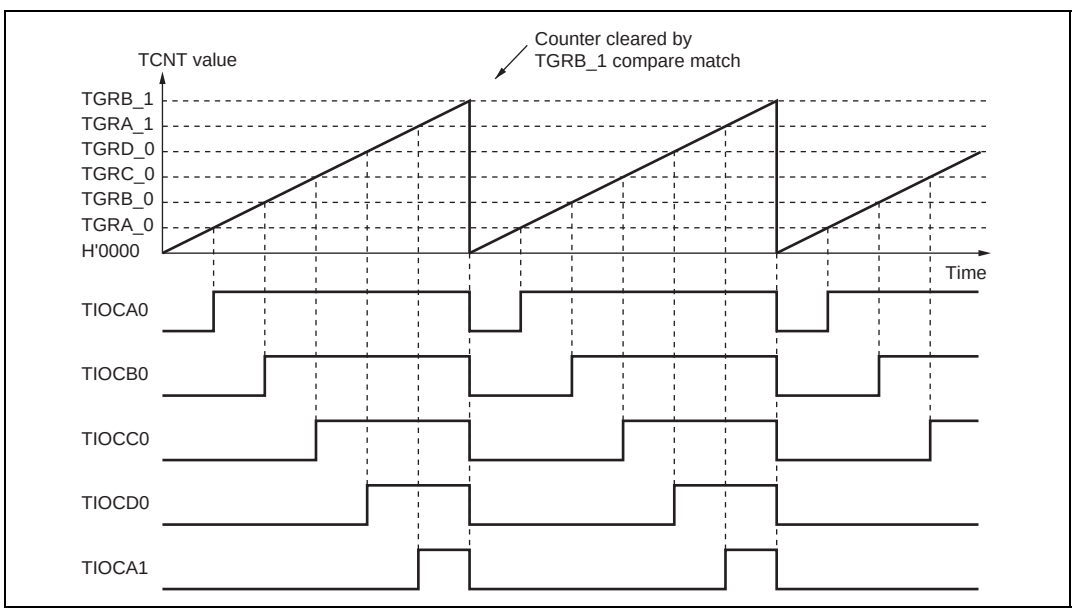

Figure 11.23 Example of PWM Mode Operation (2)

14.6 Usage Notes

14.6.1 Setting Module Stop Mode

The IEB is enabled or disabled by setting the module stop control register. In the initial state, the IEB is disabled. After the module stop mode is canceled, registers can be accessed. For details, see section 24, Power-Down Modes.

14.6.2 TxRDY Flag and Underrun Error

1. The TxRDY flag indicates that IETBR is empty. Writing to IETBR by the DTC clears the TxRDY flag. Meanwhile, the TxRDY flag must be cleared by software since writing to IETBR by the CPU does not clear the TxRDY flag.
2. If the CPU fails to write to IETBR by the timing of the frame transmission or if the number of transfer words is less than the length specified by the message length bits, an underrun error occurs.
3. The IEB decides that an underrun error occurred when the data is loaded from IETBR to the transmit shift register while the TxRDY flag is set to 1. In this case, the IEB sets the TxE flag in IETSR and enters the wait state. The UE flag in IETEF is also set to 1.
4. On the receive side, the unit decides that a timing error has occurred because the communications are terminated.
5. In data transfer using the DTC, the TxRDY flag in IETSR is not cleared after the last byte data is transferred to IETBR and a CPU interrupt caused by the DTC interrupt will occur.

   If the TxRDY flag is not cleared in this CPU interrupt handling routine, an underrun error will occur when the last byte data is loaded from IETBR to the transmit shift register. In this case, if the LUEE bit is cleared to 0 (initial value), no underrun error occurs and the last byte of the data field is transmitted correctly. (If the LUEE bit is set to 1, an underrun error occurs.)
6. Although the DTC is used as described in item 5, if the number of DTC transfer words is less than the length specified by the message length bits, the LUEE bit setting is invalid. (The LUEE bit is valid only when data is transmitted for the number of bytes specified by the message length bits has been transmitted.) In this case, an underrun error occurs, data is transmitted for one byte less than the DTC transfer words, and the transfer is terminated by a transmit error.

Table 15.8 Examples of Bit Rate for Various BRR Settings (Smart Card Interface Mode) (When n = 0 and S = 372)

Bit Rate (bps)	Operating Frequency ϕ (MHz)									
	5.00*2		7.00*2		7.1424*2		10.00		10.7136	
	N	Error (%)	N	Error (%)	N	Error (%)	N	Error (%)	N	Error (%)
6720	0	0.01	1	30.00	1	28.57	1	0.01	1	7.14
9600	0	30.00	0	1.99	0	0.00	1	30.00	1	25.00

Bit Rate (bps)	Operating Frequency ϕ (MHz)									
	13.00		14.2848*1		16.00*1		18.00*1		20.00*1	
	N	Error (%)	N	Error (%)	N	Error (%)	N	Error (%)	N	Error (%)
6720	2	13.33	2	4.76	2	6.67	3	9.99	3	0.01
9600	1	8.99	1	0.00	1	12.01	2	15.99	2	6.66

Notes: 1. Supported only by the H8S/2239 Group.
2. The H8S/2258 Group is out of operation.

Table 15.9 Maximum Bit Rate at Various Frequencies (Smart Card Interface Mode) (When S = 372)

ϕ (MHz)	Maximum Bit Rate (bps)	n	N
5.00*2	6720	0	0
7.00*2	9409	0	0
7.1424*2	9600	0	0
10.00	13441	0	0
10.7136	14400	0	0
13.00	17473	0	0
14.2848*1	19200	0	0
16.00*1	21505	0	0
18.00*1	24194	0	0
20.00*1	26882	0	0

Notes: 1. Supported only by the H8S/2239 Group.
2. The H8S/2258 Group is out of operation.

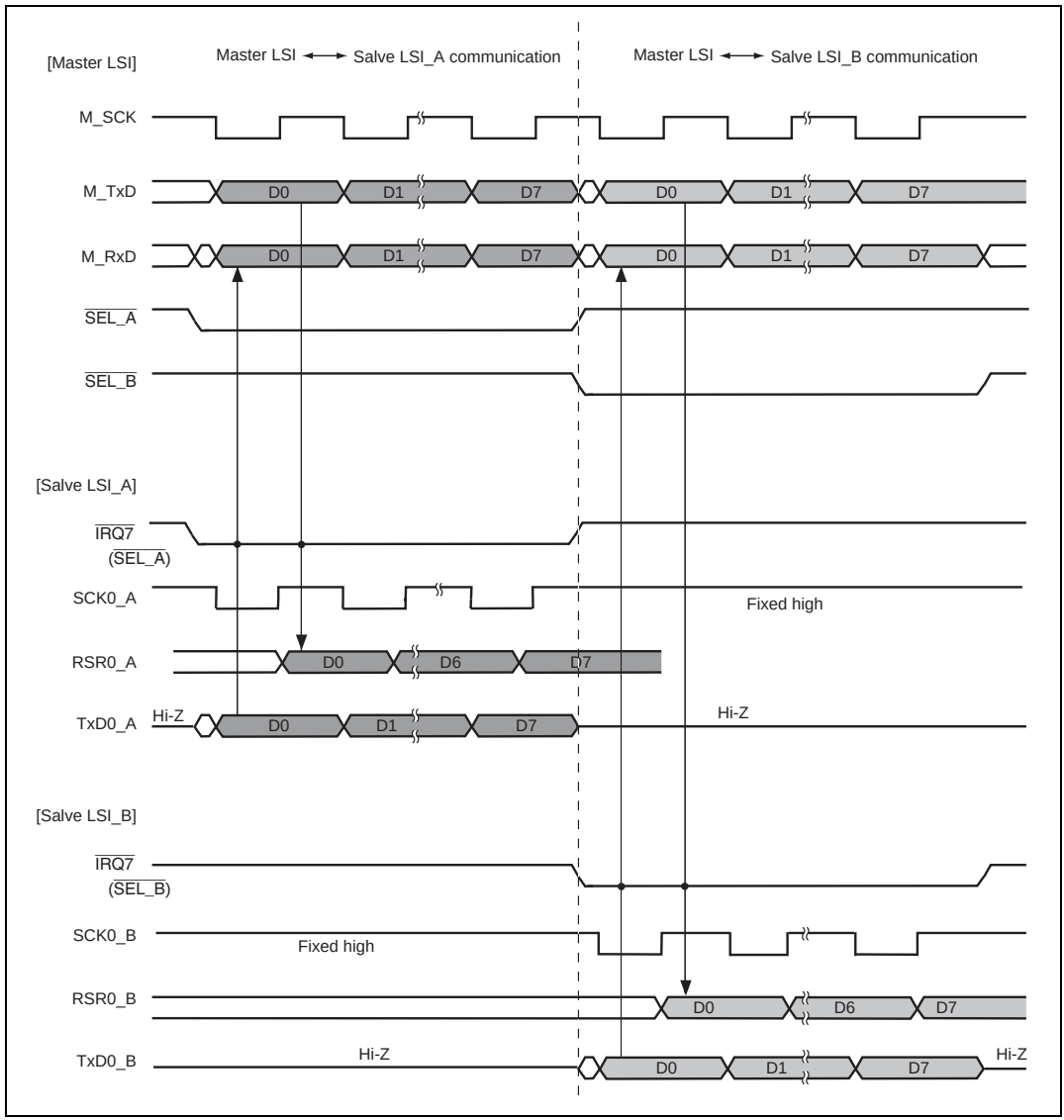

Figure 15.37 Summary of SCI Select Function Operation

Table 23.3 External Clock Input Conditions (2) (H8S/2238B, H8S/2236B)

		F-ZTAT		Masked ROM				
		V_{cc} = 3.0 V to 5.5 V		V_{cc} = 2.7 V to 5.5 V				
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
External clock input low pulse width	t_{EXL}	30	—	30	—	ns	Figure 23.5	
External clock input high pulse width	t_{EXH}	30	—	30	—	ns		
External clock rise time	t_{EXr}	—	7	—	7	ns		
External clock fall time	t_{EXf}	—	7	—	7	ns		
Clock low pulse width	t_{CL}	0.4	0.6	0.4	0.6	t_{cyc}	$\phi \geq 5$ MHz	Figure 27.10
		80	—	80	—	ns	$\phi < 5$ MHz	
Clock high pulse width	t_{CH}	0.4	0.6	0.4	0.6	t_{cyc}	$\phi \geq 5$ MHz	
		80	—	80	—	ns	$\phi < 5$ MHz	

Table 23.3 External Clock Input Conditions (3) (H8S/2238R, H8S/2236R)

		F-ZTAT		Masked ROM				
		V_{cc} = 2.7 V to 3.6 V		V_{cc} = 2.2 V to 3.6 V				
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
External clock input low pulse width	t_{EXL}	30	—	65	—	ns	Figure 23.5	
External clock input high pulse width	t_{EXH}	30	—	65	—	ns		
External clock rise time	t_{EXr}	—	7	—	15	ns		
External clock fall time	t_{EXf}	—	7	—	15	ns		
Clock low pulse width	t_{CL}	0.4	0.6	0.35	0.65	t_{cyc}	$\phi \geq 5$ MHz	Figure 27.10
		80	—	70	—	ns	$\phi < 5$ MHz	
Clock high pulse width	t_{CH}	0.4	0.6	0.35	0.65	t_{cyc}	$\phi \geq 5$ MHz	
		80	—	70	—	ns	$\phi < 5$ MHz	

than interrupts IRQ7 to IRQ0 is generated. Software standby mode cannot be cleared if the interrupt has been masked on the CPU side or has been designated as a DTC activation source.

- Clearing with the $\overline{\text{RES}}$ Pin or $\overline{\text{MRES}}$ Pin

  When the $\overline{\text{RES}}$ pin or $\overline{\text{MRES}}$ pin is driven low, clock oscillation is started. At the same time as clock oscillation starts, clocks are supplied to the entire this LSI chip. Note that the $\overline{\text{RES}}$ pin or $\overline{\text{MRES}}$ pin must be held low until clock oscillation settles. When the $\overline{\text{RES}}$ pin or $\overline{\text{MRES}}$ pin goes high, the CPU begins reset exception handling.
- Clearing with the $\overline{\text{STBY}}$ Pin

  When the $\overline{\text{STBY}}$ pin is driven low, a transition is made to hardware standby mode.

24.4.3 Oscillation Settling Time after Clearing Software Standby Mode

Bits STS2 to STS0 in SBYCR should be set as described below.

- Using a Crystal Oscillator

  Set bits STS2 to STS0 so that the standby time is at least tOSC2 ms (the oscillation settling time). Table 24.3 shows the standby times for different operating frequencies and settings of bits STS2 to STS0.
- Using an External Clock

  Any value can be set. Normally, minimum time is recommended.

Note: Do not set 16 states for standby time in the F-ZTAT version. 8192 states or more should be set.

Table 24.3 Oscillation Settling Time Settings

STS2	STS1	STS0	Standby Time	20 MHz[*1]	16 MHz[*1]	13 MHz	10 MHz	8 MHz[*2]	6 MHz[*2]	4 MHz[*2]	2 MHz[*2]	Unit
0	0	0	8192 states	0.41	0.51	0.6	0.8	1.0	1.4	2.0	4.1	ms
		1	16384 states	0.82	1.0	1.3	1.6	2.0	2.7	4.1	8.2	
	1	0	32768 states	1.6	2.0	2.5	3.3	4.1	5.5	8.2	16.4	
		1	65536 states	3.3	4.1	5.0	6.6	8.2	10.9	16.4	32.8	
1	0	0	131072 states	6.6	8.2	10.1	13.1	16.4	21.8	32.8	65.5	
		1	262144 states	13.1	16.4	20.2	26.2	32.8	43.7	65.5	131.1	
	1	0	Reserved	—	—	—	—	—	—	—	—	—
		1	16 states	0.8	1.0	1.2	1.6	2.0	2.7	4.0	8.0	µs

: Recommended time setting

Notes: 1. Supported only by the H8S/2239 Group.
2. The H8S/2258 Group is out of operation.

26.2 Register Bits

Register addresses and bit names of the on-chip peripheral modules are described below.

Each line covers eight bits, and 16-bit register is shown as 2 lines.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
MRA	SM1	SM0	DM1	DM0	MD1	MD0	DTS	Sz	DTC
SAR	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
MRB	CHNE	DISEL	—	—	—	—	—	—	
DAR	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
CRA	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
CRB	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
IECTR	IEE	IOL	DEE	CK	RE	LUEE	—	—	IEB
IECMR	—	—	—	—	—	CMD2	CMD1	CMD0	
IEMCR	SS	RN2	RN1	RN0	CTL3	CTL2	CTL1	CTL0	
IEAR1	IAR3	IAR2	IAR1	IAR0	IMD1	IMD0	—	STE	
IEAR2	IAR11	IAR10	IAR9	IAR8	IAR7	IAR6	IAR5	IAR4	
IESA1	ISA3	ISA2	ISA1	ISA0	—	—	—	—	
IESA2	ISA11	ISA10	ISA9	ISA8	ISA7	ISA6	ISA5	ISA4	
IETBFL	TBFL7	TBFL6	TBFL5	TBFL4	TBFL3	TBFL2	TBFL1	TBFL0	
IETBR	TBR7	TBR6	TBR5	TBR4	TBR3	TBR2	TBR1	TBR0	
IEMA1	IMA3	IMA2	IMA1	IMA0	—	—	—	—	
IEMA2	IMA11	IMA10	IMA9	IMA8	IMA7	IMA6	IMA5	IMA4	
IERCTL	—	—	—	—	RCTL3	RCTL2	RCTL1	RCTL0	
IERBFL	RBFL7	RBFL6	RBFL5	RBFL4	RBFL3	RBFL2	RBFL1	RBFL0	
IERBR	RBR7	RBR6	RBR5	RBR4	RBR3	RBR2	RBR1	RBR0	
IELA1	ILA7	ILA6	ILA5	ILA4	ILA3	ILA2	ILA1	ILA0	

27.4.3 AC Characteristics

Figure 27.9 shows the test conditions for the AC characteristics.

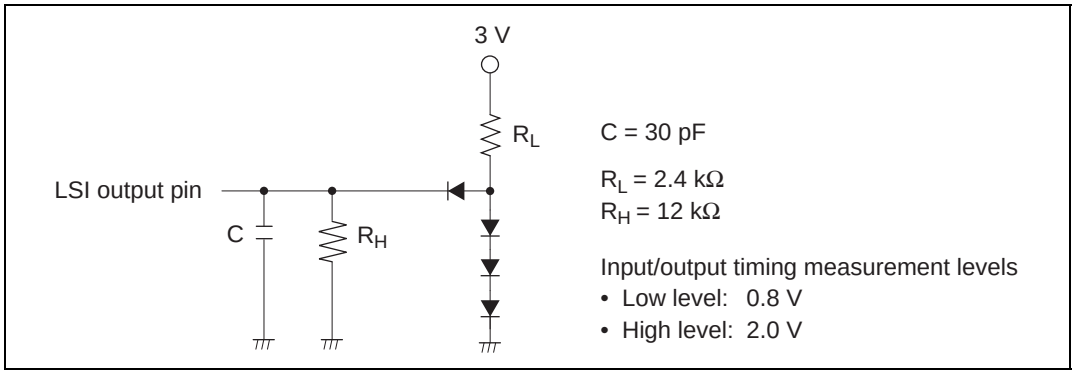

Figure 27.9 Output Load Circuit

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Erasing	Wait time after SWE1 bit clearing	t_{cswe}	100	100	—	µs	
	Maximum number of erases*1*5	N	—	—	100	Times	

Notes:
1. Follow the program/erase algorithms when making the time settings.
2. Programming time per 128 bytes (Indicates the total time during which the P1 bit is set in flash memory control register 1 (FLMCR1). Does not include the program-verify time.)
3. Time to erase one block (Indicates the time during which the E1 bit is set in FLMCR1. Does not include the erase-verify time.)
4. Maximum programming time
   (t_p(max) = Wait time after P1 bit setting (t_{sp}) × maximum number of writes (N))
   (t_{sp30} + t_{sp10}) × 6 + (t_{sp200}) × 994
5. For the maximum erase time (t_E(max)), the following relationship applies between the wait time after E1 bit setting (z) and the maximum number of erases (N):
   t_E(max) = Wait time after E1 bit setting (t_{se}) × maximum number of erases (N)
6. The minimum times that all characteristics after rewriting are guaranteed. (A range between 1 and minimum value is guaranteed.)
7. The reference value at 25°C. (Normally, it is a reference that rewriting is enabled up to this value.)
8. Data hold characteristics when rewriting is performed within the range of specifications including minimum value.