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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2238rbr13wv

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(3) Pin Arrangement of H8S/2238 Group

Figures 1.10 to 1.12 show the pin arrangement of the H8S/2238 Group.

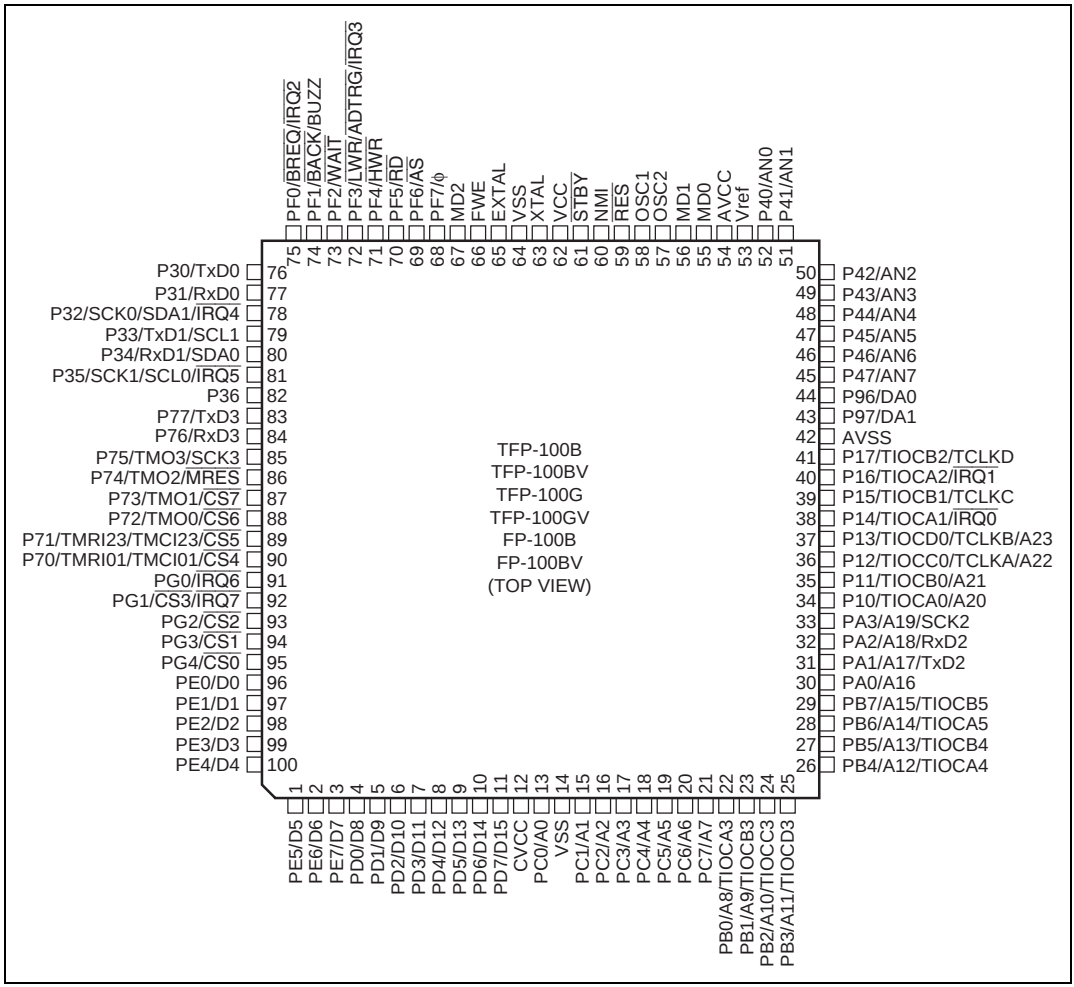


Figure 1.10 Pin Arrangement of H8S/2238 Group
(TFP-100B, TFP-100BV, TFP-100G, TFP-100GV, FP-100B, FP-100BV: Top View)

Type	Symbol	Pin No. TFP-100B TFP-100BV FP-100B FP-100BV	Pin No. FP-100A FP-100AV	I/O	Function
16-bit timer-pulse unit (TPU)	TIOCA3 TIOCB3 TIOCC3 TIOCD3	22 23 24 25	25 26 27 28	Input/ Output	Pins for the TGRA_3 to TGRD_3 input capture input, output compare output, or PWM output.
	TIOCA4 TIOCB4	26 27	29 30	Input/ Output	Pins for the TGRA_4 and TGRB_4 input capture input, output compare output, or PWM output.
	TIOCA5 TIOCB5	28 29	31 32	Input/ Output	Pins for the TGRA_5 and TGRB_5 input capture input, output compare output, or PWM output.
8-bit timer	TMO3 to TMO0	88 to 85	91 to 88	Output	Compare-match output pins.
	TMCI23 TMCI01	89 90	92 93	Input	Pins for external clock input to the counter.
	TMRI23 TMRI01	89 90	92 93	Input	Counter reset input pins.
Watchdog timer (WDT)	BUZZ	74	77	Output	This pin outputs the pulse that is divided by watchdog timer.
Serial communi-cation interface (SCI)/ smart card interface	TxD3 TxD2 TxD1 TxD0	83 31 79 76	86 34 82 79	Output	Data output pins.
	RxD3 RxD2 RxD1 RxD0	84 32 80 77	87 35 83 80	Input	Data input pins.
	SCK3 SCK2 SCK1 SCK0	85 33 81 78	88 36 84 81	Input/ Output	Clock input/output pins. SCK1 outputs NMOS push/pull.
I^2C bus interface (IIC) (optional)	SCL1 SCL0	79 81	82 84	Input/ Output	I^2C clock input/output pins. These pins drive bus. The output of SCL0 is NMOS open drain.
	SDA1 SDA0	78 80	81 83	Input/ Output	I^2C data input/output pins. These pins drive bus. The output of SDA0 is NMOS open drain.

2.8 Processing States

The H8S/2000 CPU has five main processing states: the reset state, exception handling state, program execution state, bus-released state, and power-down state. Figure 2.13 indicates the state transitions.

- Reset State

  In this state, the CPU and all on-chip peripheral modules are initialized and not operating. When the $\overline{\text{RES}}$ input goes low, all current processing stops and the CPU enters the reset state. All interrupts are masked in the reset state. Reset exception handling starts when the $\overline{\text{RES}}$ signal changes from low to high. For details, refer to section 4, Exception Handling.

  The reset state can also be entered by a watchdog timer overflow.

- Exception-Handling State

  The exception-handling state is a transient state that occurs when the CPU alters the normal processing flow due to an exception source, such as a reset, trace, interrupt, or trap instruction. The CPU fetches a start address (vector) from the exception vector table and branches to that address. For further details, refer to section 4, Exception Handling.

- Program Execution State

  In this state, the CPU executes program instructions in sequence.

- Bus-Released State

  In a product which has a DMA controller (DMAC)* or data transfer controller (DTC), the bus-released state occurs when the bus has been released in response to a bus request from a bus master other than the CPU.

  While the bus is released, the CPU halts operations.

- Power-down State

  This is a power-down state in which the CPU stops operating. The program stop state occurs when a SLEEP instruction is executed or the CPU enters hardware standby mode. For further details, refer to section 24, Power-Down Modes.

Note: * Supported only by the H8S/2239 Group.

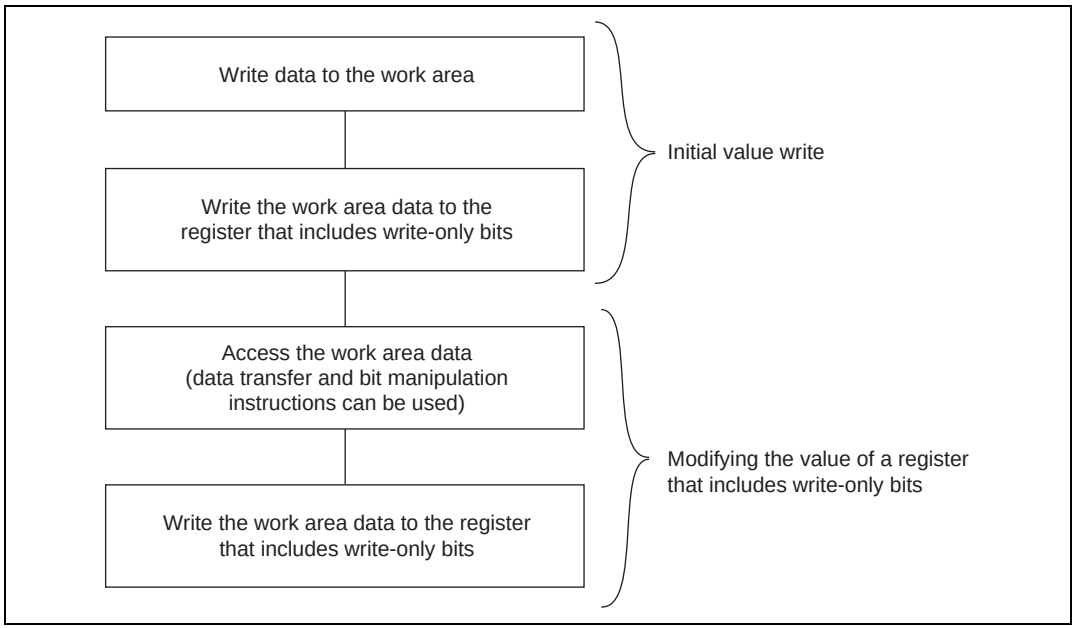


Figure 2.14 Flowchart for Access Methods for Registers That Include Write-Only Bits

Example: To clear only bit 4 in the port 1 P1DDR

The P1DDR register consists of 8 write-only bits and sets the I/O direction of the port 1 pins. Reading this register is invalid. When read, the values returned are undefined.

Here we present an example in which P14 is specified to be an input port using the BCLR instruction. First, we write the initial value H'F0 written to P1DDR to the work area in RAM (RAM0).

```
MOV.B   #H'F0,   R0L
MOV.B   R0L,     @PAM0
MOV.B   R0L,     @P1DDR
```

	P17	P16	P15	P14	P13	P12	P11	P10
I/O	Output	Output	Output	Output	Input	Input	Input	Input
P1DDR	1	1	1	1	0	0	0	0

RAM0	1	1	1	1	0	0	0	0

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*1 Advanced Mode	IPR*2	Priority
—	Reserved	53	H'00D4	IPRG2 to IPRG0	High
		54	H'00D8		
		55	H'00DC		
TPU channel 4*3	TGI4A (TGR4A input capture/compare-match)	56	H'00E0	IPRH6 to IPRH4	
	TGI4B (TGR4B input capture/compare-match)	57	H'00E4		
	TCI4V (overflow 4)	58	H'00E8		
	TCI4U (underflow 4)	59	H'00EC		
TPU channel 5*3	TGI5A (TGR5A input capture/compare-match)	60	H'00F0	IPRH2 to IPRH0	
	TGI5B (TGR5B input capture/compare-match)	61	H'00F4		
	TCI5V (overflow 5)	62	H'00F8		
	TCI5U (underflow 5)	63	H'00FC		
8-bit timer channel 0	CMIA0 (compare-match A0)	64	H'0100	IPRI6 to IPRI4	
	CMIB0 (compare-match B0)	65	H'0104		
	OVI0 (overflow 0)	66	H'0108		
—	Reserved	67	H'010C		
8-bit timer channel 1	CMIA1 (compare-match A1)	68	H'0110	IPRI2 to IPRI0	
	CMIB1 (compare-match B1)	69	H'0114		
	OVI1 (overflow 1)	70	H'0118		
—	Reserved	71	H'011C		Low

7.3.1 Bus Width Control Register (ABWCR)

ABWCR designates each area for either 8-bit access or 16-bit access.

ABWCR sets the data bus width for the external memory space. The bus width for on-chip memory and internal I/O registers is fixed regardless of the settings in ABWCR.

Bit	Bit Name	Initial Value	R/W	Description
7	ABW7	1/0*	R/W	Area 7 to 0 Bus Width Control
6	ABW6	1/0*	R/W	These bits select whether the corresponding area is to be designated for 8-bit access or 16-bit access.
5	ABW5	1/0*	R/W	
4	ABW4	1/0*	R/W	0: Area n is designated for 16-bit access
3	ABW3	1/0*	R/W	1: Area n is designated for 8-bit access
2	ABW2	1/0*	R/W	Note: n = 7 to 0
1	ABW1	1/0*	R/W	
0	ABW0	1/0*	R/W	

Note: * In modes 5 to 7, initial value of each bit is 1. In mode 4, initial value of each bit is 0.

7.3.2 Access State Control Register (ASTCR)

ASTCR designates each area as either a 2-state access space or a 3-state access space.

ASTCR sets the number of access states for the external memory space. The number of access states for on-chip memory and internal I/O registers is fixed regardless of the settings in ASTCR.

Bit	Bit Name	Initial Value	R/W	Description
7	AST7	1	R/W	Area 7 to 0 Access State Control
6	AST6	1	R/W	These bits select whether the corresponding area is to be designated as a 2-state access space or a 3-state access space. Wait state insertion is enabled or disabled at the same time.
5	AST5	1	R/W	
4	AST4	1	R/W	
3	AST3	1	R/W	0: Area n is designated for 2-state access
2	AST2	1	R/W	Wait state insertion in area n external space is disabled
1	AST1	1	R/W	
0	AST0	1	R/W	1: Area n is designated for 3-state access
				Wait state insertion in area n external space is enabled
				Note: n = 7 to 0

Bit	Bit Name	Initial Value	R/W	Description
12	BLKDIR	0	R/W	Block Direction
11	BLKE	0	R/W	Block Enable These bits specify whether normal mode or block transfer mode is to be used for data transfer. If block transfer mode is specified, the BLKDIR bit specifies whether the source side or the destination side is to be the block area. ×0: Transfer in normal mode 01: Transfer in block transfer mode (destination side is block area) 11: Transfer in block transfer mode (source side is block area)
10 to 8	—	All 0	R/W	Reserved These bits can be read from or written to. However, the write value should always be 0.

Legend:

×: Don't care

8.5 Operation

8.5.1 Transfer Modes

Table 8.4 lists the DMAC transfer modes.

Table 8.4 DMAC Transfer Modes

Transfer Mode		Transfer Source	Remarks
Short address mode	Dual address mode • 1-byte or 1-word transfer for a single transfer request • Specify source and destination addresses to transfer data in two bus cycles. (1) Sequential mode • Memory address incremented or decremented by 1 or 2 • Number of transfers: 1 to 65,536 (2) Idle mode • Memory address fixed • Number of transfers: 1 to 65,536 (3) Repeat mode • Memory address incremented or decremented by 1 or 2 • Continues transfer after sending number of transfers (1 to 256) and restoring the initial value	• TPU channel 0 to 5 compare match/input capture A interrupt • SCI transmit-data-empty interrupt • SCI receive-data-full interrupt • A/D converter conversion end interrupt • External request	• Up to 4 channels can operate independently • External request applies to channel B only • Single address mode applies to channel B only
	Single address mode • 1-byte or 1-word transfer for a single transfer request • 1-bus cycle transfer by means of $\overline{\text{DACK}}$ pin instead of using address for specifying I/O • Sequential mode, idle mode, or repeat mode can be specified	• External request	

10.1.4 Pin Functions

Port 1 pins also function as TPU I/O pins (TPU_0, TPU_1, and TPU_2), DMAC* output pins, interrupt input pins and address output pins. Values of the register and pin functions are shown below.

Note: * Supported only by the H8S/2239 Group.

- P17/TIOCB2/TCLKD

  The pin functions are switched as shown below according to the combination of the TPU channel 2 setting, TPSC2 to TPS0 bits in TCR_0 and TCR_5, and the P17DDR bit.

TPU Channel 2 Setting*1	Output	Input or Initial Value	
P17DDR	—	0	1
Pin functions	TIOCB2 output pin	P17 input pin	P17 output pin
		TIOCB2 input pin*2	
	TCLKD input pin*3		

Notes: 1. For the setting of the TPU channel, see section 11, 16-Bit Timer Pulse Unit (TPU).
2. This pin functions as TIOCB2 input when TPU channel 2 timer operating mode is set to normal operating or phase counting mode and IOB3 in TIOR_2 is set to 1.
3. This pin functions as TCLKD input when TPSC2 to TPSC0 in TCR_0 or TCR_5 are set to 111 or when channels 2 and 4 are set to phase counting mode.

- P16/TIOCA2/$\overline{\text{IRQ1}}$

  The pin functions are switched as shown below according to the combination of the TPU channel 2 setting and the P16DDR bit.

TPU Channel 2 Setting*1	Output	Input or Initial Value	
P16DDR	—	0	1
Pin functions	TIOCA2 output pin	P16 input pin	P16 output pin
		TIOCA2 input pin*2	
	$\overline{\text{IRQ1}}$ input pin*3		

Notes: 1. For the setting of the TPU channel, see section 11, 16-Bit Timer Pulse Unit (TPU).
2. This pin functions as TIOCA2 input when TPU channel 2 timer operating mode is set to normal operating or phase counting mode and IOA3 in TIOR_2 is 1.
3. When this pin is used as an external interrupt pin, do not specify other functions.

10.7.3 Port B Register (PORTB)

PORTB shows the pin states and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7	—*	R	If these bits are read while the corresponding PBDDR bits are set to 1, the PBDR value is read. If these bits are read while PBDDR bits are cleared to 0, the pin states are read.
6	PB6	—*	R	
5	PB5	—*	R	
4	PB4	—*	R	
3	PB3	—*	R	
2	PB2	—*	R	
1	PB1	—*	R	
0	PB0	—*	R	

Note: * Determined by the states of pins PB7 to PB0.

10.7.4 Port B Pull-Up MOS Control Register (PBPCR)

PBPCR controls the on/off state of port B input pull-up MOS.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7PCR	0	R/W	When a pin is specified as an input port, setting the corresponding bit to 1 turns on the input pull-up MOS for that pin.
6	PB6PCR	0	R/W	
5	PB5PCR	0	R/W	
4	PB4PCR	0	R/W	
3	PB3PCR	0	R/W	
2	PB2PCR	0	R/W	
1	PB1PCR	0	R/W	
0	PB0PCR	0	R/W	

10.7.5 Pin Functions

Port B pins also function as TPU I/O pins (TPU_3*, TPU_4*, and TPU_5*) and address output pins. The values of register and pin functions are shown bellow.

Note: * Not available in the H8S/2227 Group.

10.11 Port F

Port F is an 8-bit I/O port and has the following registers.

- Port F data direction register (PFDDR)
- Port F data register (PFDR)
- Port F register (PORTF)

10.11.1 Port F Data Direction Register (PFDDR)

PFDDR specifies input or output of the port F pins using the individual bits. PFDDR cannot be read; if it is, an undefined value will be read. This register is a write-only register, and cannot be written by bit manipulation instruction. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7	PF7DDR	0/1*	W	When a pin is specified as a general purpose I/O port, setting this bit to 1 makes the corresponding port F pin an output port. Clearing this bit to 0 makes the pin an input port.
6	PF6DDR	0	W	
5	PF5DDR	0	W	
4	PF4DDR	0	W	
3	PF3DDR	0	W	
2	PF2DDR	0	W	
1	PF1DDR	0	W	
0	PF0DDR	0	W	

Note: * In modes 4 to 6, initial value is 1. In mode 7, initial value is 0.

Example of Phase Counting Mode Setting Procedure: Figure 11.25 shows an example of the phase counting mode setting procedure.

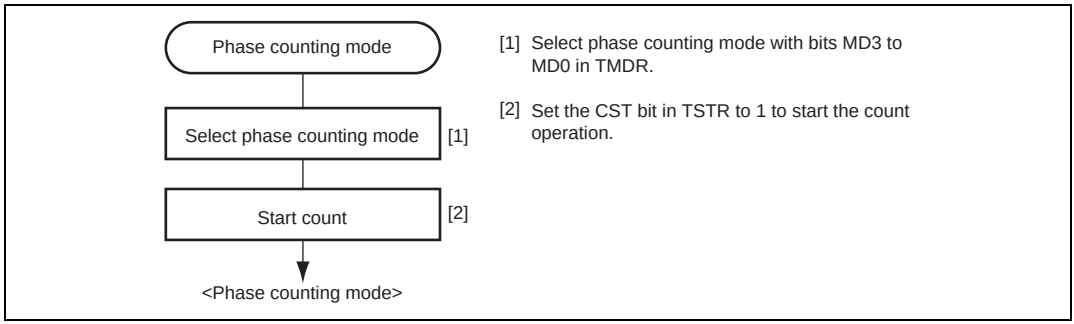


Figure 11.25 Example of Phase Counting Mode Setting Procedure

Examples of Phase Counting Mode Operation: In phase counting mode, TCNT counts up or down according to the phase difference between two external clocks. There are four modes, according to the count conditions.

1. Phase counting mode 1

   Figure 11.26 shows an example of phase counting mode 1 operation, and table 11.32 summarizes the TCNT up/down-count conditions.

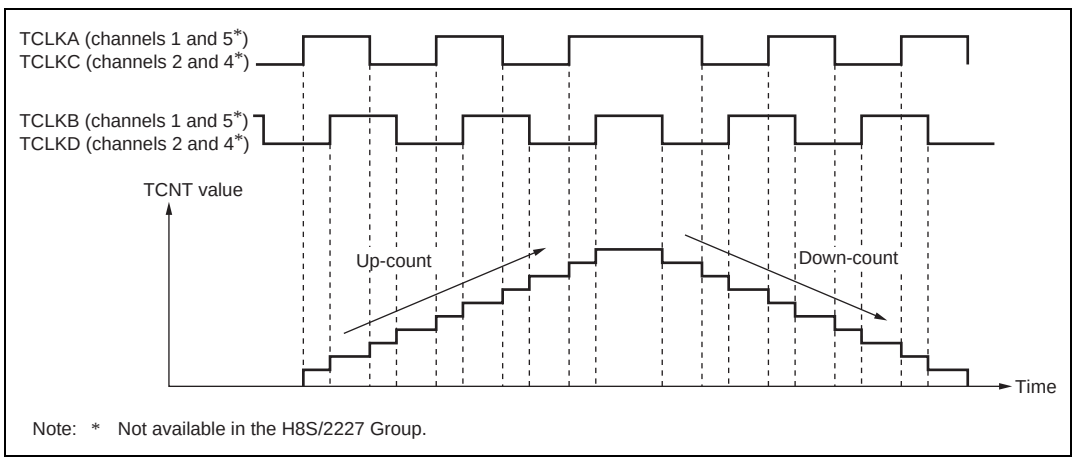


Figure 11.26 Example of Phase Counting Mode 1 Operation

Bit	Bit Name	Initial Value	R/W	Description
2	TxS	0	R/W	Transmit Start Detection Indicates that the IEB starts transmission. [Setting conditions] • Master transmission: When the arbitration is won and when the master address field transmission is completed • Slave transmission: When the control bits of H'3 (0011) or H'7 (0111) is received from the master unit meaning that data transfer is requested [Clearing condition] When writing 0 after reading TxS = 1
1	TxF	0	R/W	Transmit Normal Completion Indicates that data for the number of bytes specified by the message length bits has been transmitted with no error. [Setting condition] When data for the number of bytes specified by the message length bits has been transmitted normally [Clearing condition] When writing 0 after reading TxF = 1

14.6 Usage Notes

14.6.1 Setting Module Stop Mode

The IEB is enabled or disabled by setting the module stop control register. In the initial state, the IEB is disabled. After the module stop mode is canceled, registers can be accessed. For details, see section 24, Power-Down Modes.

14.6.2 TxRDY Flag and Underrun Error

1. The TxRDY flag indicates that IETBR is empty. Writing to IETBR by the DTC clears the TxRDY flag. Meanwhile, the TxRDY flag must be cleared by software since writing to IETBR by the CPU does not clear the TxRDY flag.
2. If the CPU fails to write to IETBR by the timing of the frame transmission or if the number of transfer words is less than the length specified by the message length bits, an underrun error occurs.
3. The IEB decides that an underrun error occurred when the data is loaded from IETBR to the transmit shift register while the TxRDY flag is set to 1. In this case, the IEB sets the TxE flag in IETSR and enters the wait state. The UE flag in IETEF is also set to 1.
4. On the receive side, the unit decides that a timing error has occurred because the communications are terminated.
5. In data transfer using the DTC, the TxRDY flag in IETSR is not cleared after the last byte data is transferred to IETBR and a CPU interrupt caused by the DTC interrupt will occur.

   If the TxRDY flag is not cleared in this CPU interrupt handling routine, an underrun error will occur when the last byte data is loaded from IETBR to the transmit shift register. In this case, if the LUEE bit is cleared to 0 (initial value), no underrun error occurs and the last byte of the data field is transmitted correctly. (If the LUEE bit is set to 1, an underrun error occurs.)
6. Although the DTC is used as described in item 5, if the number of DTC transfer words is less than the length specified by the message length bits, the LUEE bit setting is invalid. (The LUEE bit is valid only when data is transmitted for the number of bytes specified by the message length bits has been transmitted.) In this case, an underrun error occurs, data is transmitted for one byte less than the DTC transfer words, and the transfer is terminated by a transmit error.

9. Notes on I²C Bus Interface Stop Condition Instruction Issuance

If the rise time of the 9th SCL acknowledge exceeds the specification because the bus load capacitance is large, or if there is a slave device of the type that drives SCL low to effect a wait, issue the stop condition instruction after reading SCL and determining it to be low, as shown below.

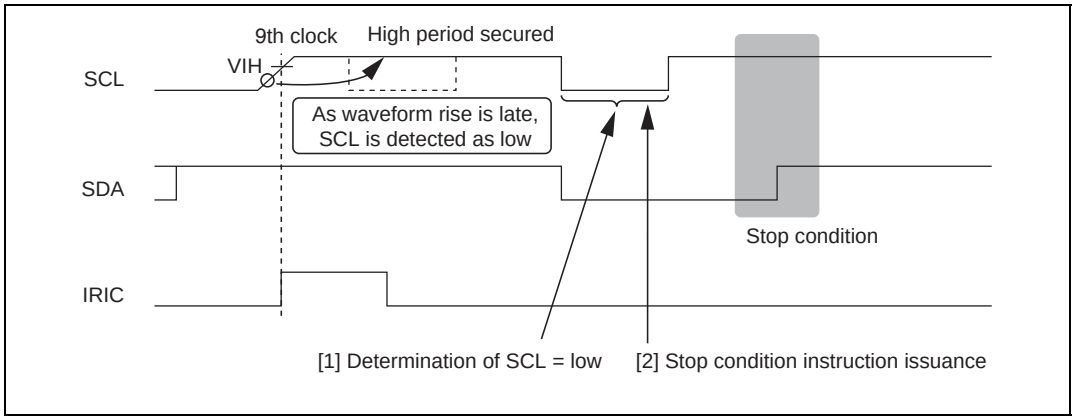


Figure 16.23 Timing of Stop Condition Issuance

10. Notes on IRIC Flag Clearance when Using Wait Function

If the SCL rise time exceeds the designated duration or if the slave device is of the type that keeps SCL low and applies a wait state when the wait function is used in the master mode of the I²C bus interface, read SCL and clear the IRIC flag after determining that SCL has gone low, as shown below.

Clearing the IRIC flag to 0 when WAIT is set to 1 and SCL is being held at high level can cause the SDA value to change before SCL goes low, resulting in a start condition or stop condition being generated erroneously.

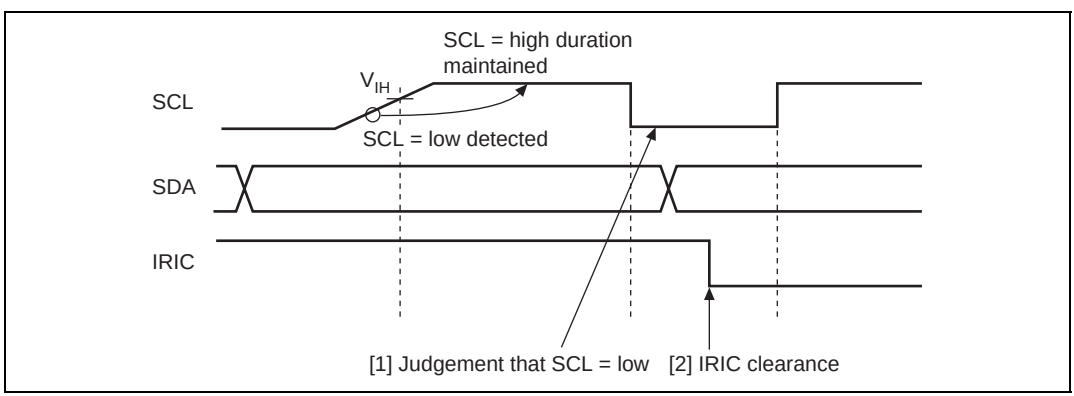


Figure 16.24 IRIC Flag Clearance in WAIT = 1 Status

In boot mode, if any data has been programmed into the flash memory (if all data is not 1), all flash memory blocks are erased. Boot mode is for use when user program mode is unavailable, such as the first time on-board programming is performed, or if the program activated in user program mode is accidentally erased.

2. SCI should be set to asynchronous mode, and the transfer format as follows: 8-bit data, 1 stop bit, and no parity.
3. When the boot program is initiated, the chip measures the low-level period of asynchronous SCI communication data (H'00) transmitted continuously from the host. The chip then calculates the bit rate of transmission from the host, and adjusts the SCI bit rate to match that of the host. The reset should end with the RxD pin high. The RxD and TxD pins should be pulled up on the board if necessary. After the reset is complete, it takes approximately 100 states before the chip is ready to measure the low-level period.
4. After matching the bit rates, the chip transmits one H'00 byte to the host to indicate the completion of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception could not be performed normally, initiate boot mode again by a reset. Depending on the host's transfer bit rate and system clock frequency of this LSI, there will be a discrepancy between the bit rates of the host and the chip. To operate the SCI properly, set the host's transfer bit rate and system clock frequency of this LSI within the ranges listed in table 20.5.
5. In boot mode, a part of the on-chip RAM area is used by the boot program. The area H'FFC000 to H'FFDFFF is the area to which the programming control program is transferred from the host. The boot program area cannot be used until the execution state in boot mode switches to the programming control program.
6. Before branching to the programming control program, the chip terminates transfer operations by SCI (by clearing the RE and TE bits in SCR to 0), however the adjusted bit rate value remains set in BRR. Therefore, the programming control program can still use it for transfer of write data or verify data with the host. The TxD pin is high. The contents of the CPU general registers are undefined immediately after branching to the programming control program. These registers must be initialized at the beginning of the programming control program, as the stack pointer (SP), in particular, is used implicitly in subroutine calls, etc.
7. Boot mode can be cleared by driving the reset pin low, waiting at least 20 states, then setting the FWE pin and mode pins, and executing reset release*. Boot mode is also cleared when a WDT overflow occurs.
8. All interrupts are disabled during programming or erasing of the flash memory.

Note: * The input signals on the FWE and mode pins must satisfy the mode programming setup time (t_{MDS} = 200 ns) at the reset release timing.

(1) Clock Timing

Table 27.5 lists the clock timing.

Table 27.5 Clock Timing

Condition A: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{ref} = 4.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32.768 kHz, 10 to 13.5 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Clock cycle time	t_{cyc}	74	100	ns	Figure 27.10
Clock high pulse width	t_{CH}	25	—	ns	
Clock low pulse width	t_{CL}	25	—	ns	
Clock rise time	t_{Cr}	—	10	ns	
Clock fall time	t_{Cf}	—	10	ns	
Oscillation stabilization time at reset (crystal)	t_{OSC1}	20	—	ms	Figure 27.11
Oscillation stabilization time in software standby (crystal)	t_{OSC2}	8	—	ms	
External clock output stabilization delay time	t_{DEXT}	500	—	µs	Figure 27.11
32-kHz clock oscillation stabilization time	t_{OSC3}	—	2	s	
Subclock oscillator frequency	f_{SUB}	32.768	32.768	kHz	
Subclock (ϕ_{SUB}) cycle time	t_{SUB}	30.5	30.5	µs	

27.3 Electrical Characteristics of H8S/2239 Group

27.3.1 Absolute Maximum Ratings

Table 27.13 lists the absolute maximum ratings.

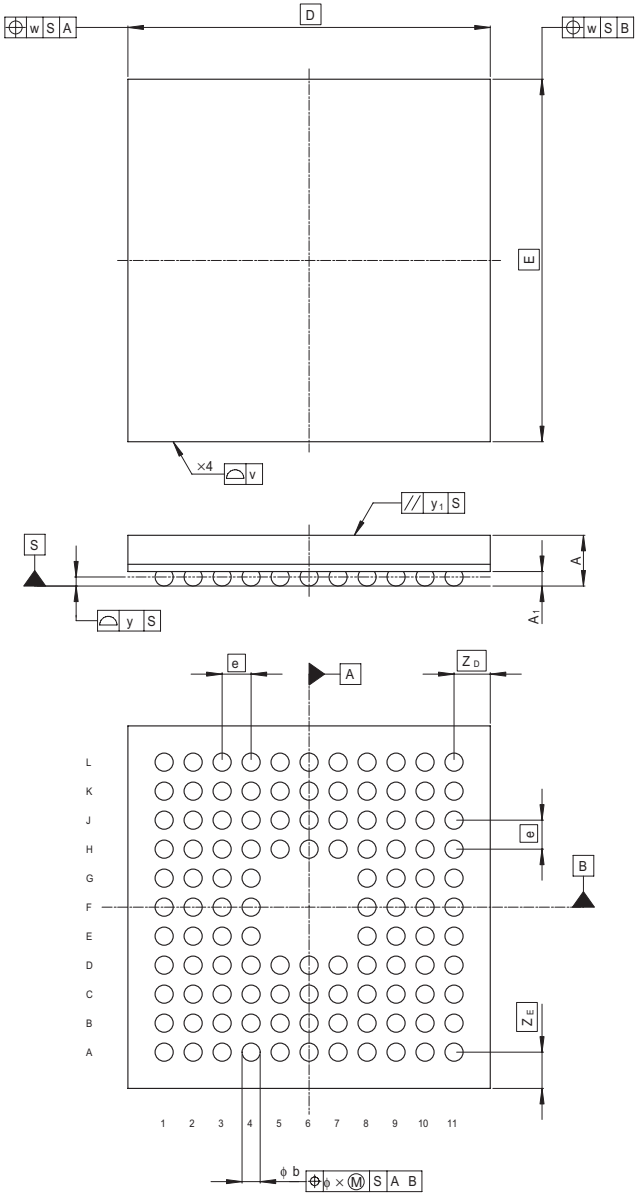
Table 27.13 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +4.3	V
	CV_{CC}	–0.3 to +4.3	V
Input voltage (except ports 4 and 9)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (ports 4 and 9)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75*	°C
		Wide-range specifications: –40 to +85*	
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum rating are exceeded.

Note: * The operating temperature ranges for flash memory programming/erasing are T_a = –20°C to +50°C (regular specifications).

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA112-10x10-0.80	PLBG0112GA-A	BP-112/BP-112V	0.3g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.00	—
E	—	10.00	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	1.00	—
Z_E	—	1.00	—

Figure C.5 BP-112 Package Dimensions