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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	6MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2238rfa6v

Configuration of This Manual

This manual comprises the following items:

1. General Precautions in the Handling of MPU/MCU Products
2. Configuration of This Manual
3. Preface
4. Main Revisions for This Edition

   The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.
5. Contents
6. Overview
7. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

   The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

   i) Feature

   ii) Input/Output Pin

   iii) Register Description

   iv) Operation

   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

8. List of Registers
9. Electrical Characteristics
10. Appendix
11. Index

Section 3 MCU Operating Modes

Section 4 Exception Handling

Section 5 Interrupt Controller

Section 6 PC Break Controller (PBC)

Section 7 Bus Controller

Table 11.32 Up/Down-Count Conditions in Phase Counting Mode 1

TCLKA (Channels 1 and 5*) TCLKC (Channels 2 and 4*)	TCLKB (Channels 1 and 5*) TCLKD (Channels 2 and 4*)	Operation
High level	↑	Up-count
Low level	↓	
↑	Low level	
↓	High level	
High level	↓	Down-count
Low level	↑	
↑	High level	
↓	Low level	

Legend:

↑: Rising edge

↓: Falling edge

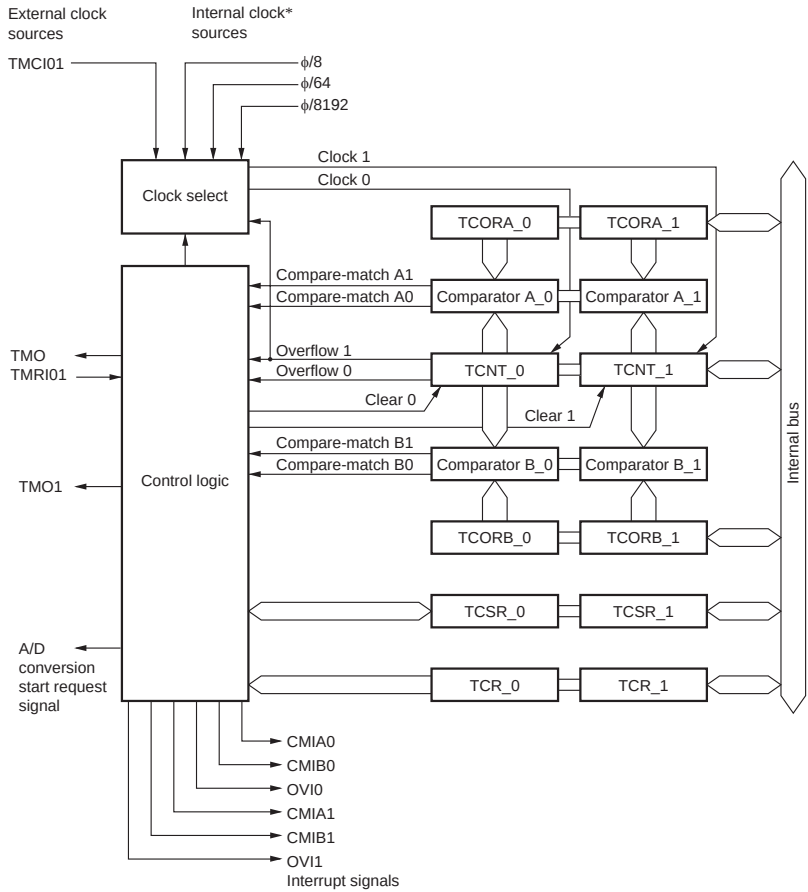
Note: * Not available in the H8S/2227 Group.

- Module stop mode can be set

  At initialization, the 8-bit timer operation is halted. Register access is enabled by canceling the module stop mode.

Note: * Not available in the H8S/2237 Group and H8S/2227 Group.

Figure 12.1 shows a block diagram of the 8-bit timer module (TMR_0 and TMR_1).



Legend:

TCORA_0:	Time constant register A_0	TCORA_1:	Time constant register A_1
TCORB_0:	Time constant register B_0	TCORB_1:	Time constant register B_1
TCNT_0:	Timer counter _0	TCNT_1:	Timer counter _1
TCSR_0:	Timer control/status register _0	TCSR_1:	Timer control/status register _1
TCR_0:	Timer control register _0	TCR_1:	Timer control register _1

Note: * When a sub-clock is operating in power-down mode, φ will be f_{SUB}.

Figure 12.1 Block Diagram of 8-Bit Timer Module

12.5.3 Timing of Timer Output when a Compare-Match Occurs

When a compare-match occurs, the timer output changes as specified by the output select bits (OS3 to OS0) in TCSR. Figure 12.6 shows the timing when the output is set to toggle at compare-match A.

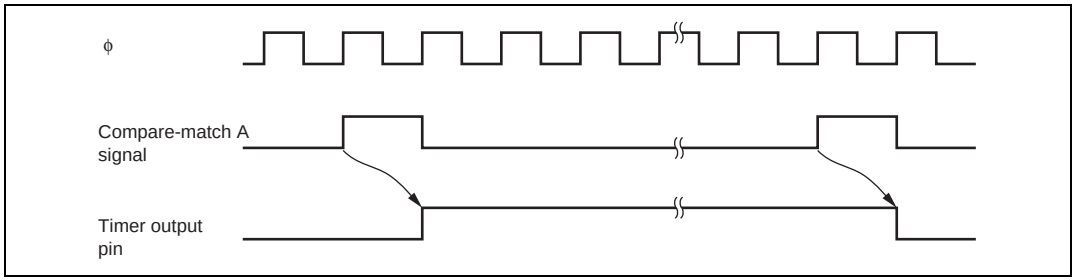


Figure 12.6 Timing of Timer Output

12.5.4 Timing of Compare-Match Clear when a Compare-Match Occurs

TCNT is cleared when compare-match A or B occurs, depending on the setting of the CCLR1 and CCLR0 bits in TCR. Figure 12.7 shows the timing of this operation.

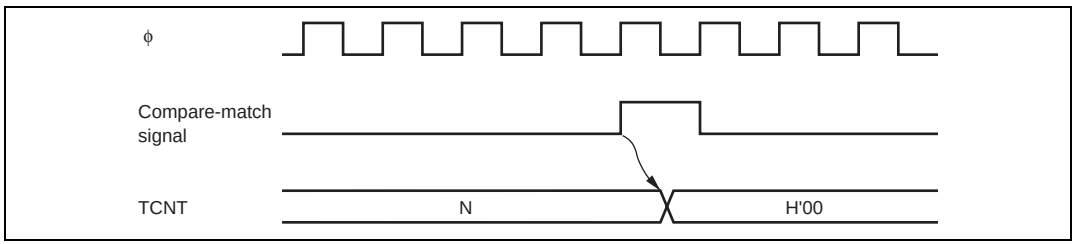


Figure 12.7 Timing of Compare-Match Clear

14.3.5 IEBus Master Unit Address Register 2 (IEAR2)

IEAR2 sets the upper 8 bits of the master unit address. In master communications, this register becomes the master address field value. In slave communications, this register is compared with the received slave address field.

Bit	Bit Name	Initial Value	R/W	Description
7	IAR11	0	R/W	Upper 8 Bits of IEBus Master Unit Address
6	IAR10	0	R/W	Set the upper 8 bits of the master unit address.
5	IAR9	0	R/W	
4	IAR8	0	R/W	
3	IAR7	0	R/W	
2	IAR6	0	R/W	
1	IAR5	0	R/W	
0	IAR4	0	R/W	

14.3.6 IEBus Slave Address Setting Register 1 (IESA1)

IESA1 sets the lower 4 bits of the communications destination slave unit address. For slave communications, it is not necessary to set this register.

Bit	Bit Name	Initial Value	R/W	Description
7	ISA3	0	R/W	Lower 4 Bits of IEBus Slave Address
6	ISA2	0	R/W	These bits set the lower 4 bits of the communications destination slave unit address
5	ISA1	0	R/W	
4	ISA0	0	R/W	
3 to 0	—	All 0	—	Reserved These bits are always read as 0 and cannot be modified.

Section 15 Serial Communication Interface (SCI)

This LSI has independent serial communication interfaces (SCIs). The SCI can handle both asynchronous and clocked synchronous serial communication. Serial data communication can be carried out using standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or an Asynchronous Communication Interface Adapter (ACIA). A function is also provided for serial communication between processors (multiprocessor communication function). The SCI also supports an IC card (Smart Card) interface conforming to ISO/IEC 7816-3 (Identification Card) as a serial communication interface extended function.

15.1 Features

- The number of on-chip channels

  H8S/2258 Group, H8S/2239 Group, H8S/2238 Group, and H8S/2237 Group: Four channels (channels 0, 1, 2, and 3)

  H8S/2227 Group: Three channels (channels 0, 1, and 3)
- Choice of asynchronous or clocked synchronous serial communication mode
- Full-duplex communication capability

  The transmitter and receiver are mutually independent, enabling transmission and reception to be executed simultaneously.

  Double-buffering is used in both the transmitter and the receiver, enabling continuous transmission and continuous reception of serial data.
- On-chip baud rate generator allows any bit rate to be selected

  External clock can be selected as a transfer clock source (except for in Smart Card interface mode).
- Choice of LSB-first or MSB-first transfer (except in the case of asynchronous mode 7-bit data)
- Four interrupt sources

  Transmit-end, transmit-data-empty, receive-data-full, and receive error — that can issue requests.

  The transmit-data-empty interrupt and receive data full interrupts can be used to activate the data transfer controller (DTC) or the direct memory access controller (DMAC) (H8S/2239 Group only).
- Module stop mode can be set

Figure 15.1 shows a block diagram of the SCI (except SCI_0 of the H8S/2239 Group), and figure 15.2 shows that of the SCI_0 of the H8S/2239 Group.

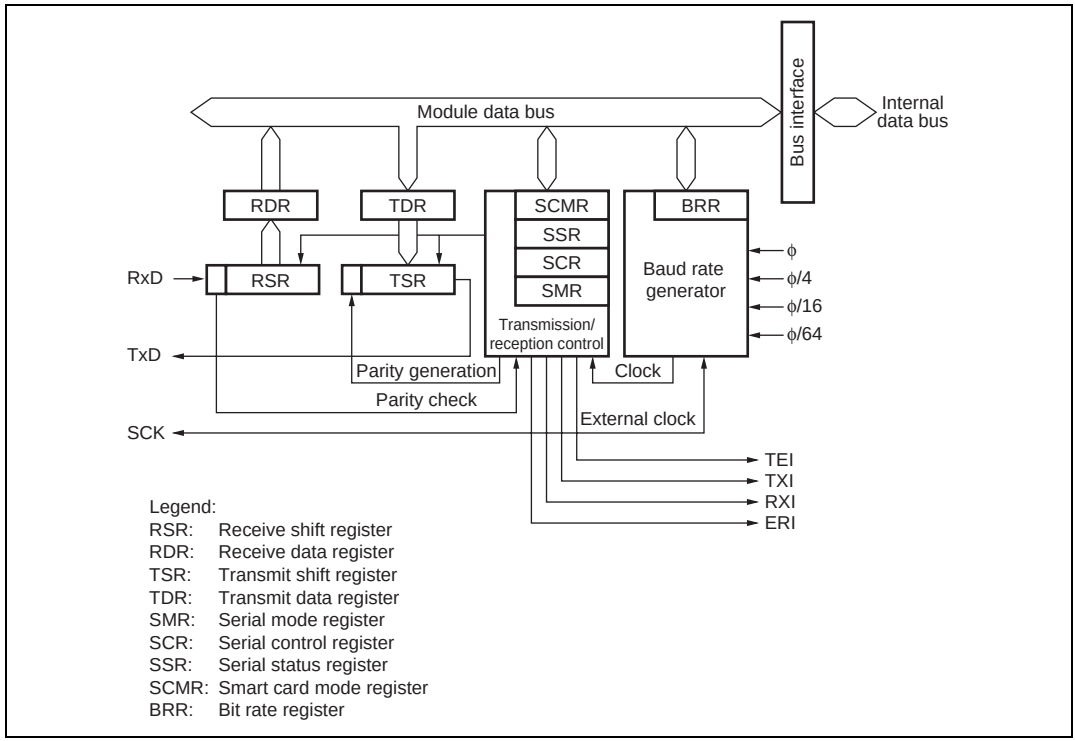
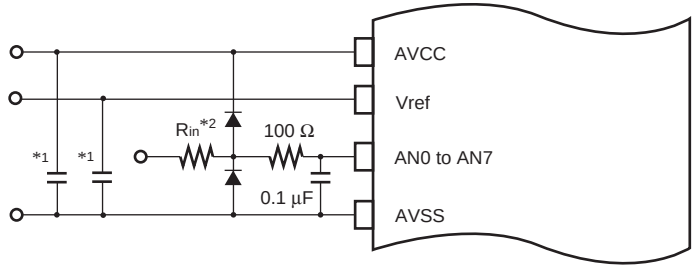
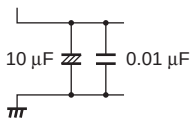


Figure 15.1 Block Diagram of SCI



Notes: Values are reference values.

1.

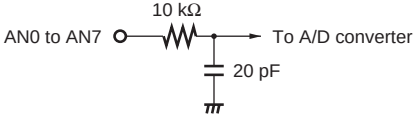


2. R_{in}: Input impedance

Figure 17.10 Example of Analog Input Protection Circuit

Table 17.6 Analog Pin Specifications

Item	Min	Max	Unit
Analog input capacitance	—	20	pF
Permissible signal source impedance	—	5	kΩ



Note: Values are reference values.

Figure 17.11 Analog Input Pin Equivalent Circuit

20.4 Input/Output Pins

The flash memory is controlled by means of the pins shown in table 20.2.

Table 20.2 Pin Configuration

Pin Name	I/O	Function
$\overline{\text{RES}}$	Input	Reset
FWE	Input	Flash program/erase protection by hardware
MD2	Input	Sets this LSI's operating mode
MD1	Input	Sets this LSI's operating mode
MD0	Input	Sets this LSI's operating mode
PF0	Input	Sets MCU operating mode in programmer mode
P16	Input	Sets MCU operating mode in programmer mode
P14	Input	Sets MCU operating mode in programmer mode
TxD*	Output	Serial transmit data output
RxD*	Input	Serial receive data input

Note: * SCI_2 (TxD2, RxD2) is used for the H8S/2258, H8S/2239, H8S/2238B, and H8S/2238R, and SCI_0 (TxD0, RxD0) for the H8S/2227.

20.5 Register Descriptions

The flash memory has the following registers.

- Flash memory control register 1 (FLMCR1)
- Flash memory control register 2 (FLMCR2)
- Erase block register 1 (EBR1)
- Erase block register 2 (EBR2)
- RAM emulation register (RAMER)
- Flash memory power control register (FLPWCR)
- Serial control register X (SCRX)

The registers described above are not present in the masked ROM version. If a register described above is read in the masked ROM version, an undefined value will be returned.

Bit	Bit Name	Initial Value	R/W	Description
1	STC1	0	R/W	Multiplication factor setting
0	STC0	0	R/W	Specifies multiplication factor of the PLL circuit built in the evaluation chip. The specified multiplication factor becomes valid software standby mode, watch mode, or subactive mode is entered. These bits should be set to 11 in this LSI. Since the value becomes STC1 = STC0 = 0 after a reset, set STC1 = STC0 = 1. 00: × 1 01: × 2 (setting prohibited) 10: × 4 (setting prohibited) 11: PLL is bypass

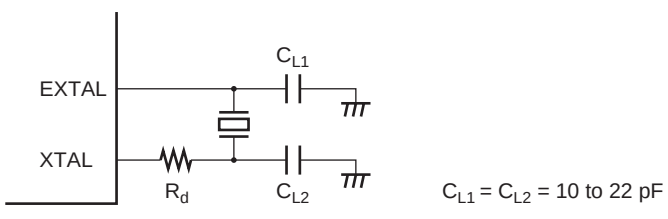
Note: * When watch mode or subactive mode is entered, set high-speed mode.

23.2 System Clock Oscillator

System clock pulses can be supplied by connecting a crystal resonator, or by input of an external clock.

23.2.1 Connecting a Crystal Resonator

A crystal resonator can be connected as shown in the example in figure 23.2. Select the damping resistance R_d according to table 23.1. An AT-cut parallel-resonance crystal should be used.



Note: C_{L1} and C_{L2} are reference values including the floating capacitance of the board.

Figure 23.2 Connection of Crystal Resonator (Example)

Register Name	Abbreviation	Bit No.	Address*1	Module	Data Bus Width	Access State
Timer control register_5	TCR_5	8	H'FEA0	TPU_5	8	2
Timer mode register_5	TMDR_5	8	H'FEA1	TPU_5	8	2
Timer I/O control register_5	TIOR_5	8	H'FEA2	TPU_5	8	2
Timer interrupt enable register_5	TIER_5	8	H'FEA4	TPU_5	8	2
Timer status register_5	TSR_5	8	H'FEA5	TPU_5	8	2
Timer counter_5	TCNT_5	16	H'FEA6	TPU_5	16	2
Timer general register A_5	TGRA_5	16	H'FEA8	TPU_5	16	2
Timer general register B_5	TGRB_5	16	H'FEAA	TPU_5	16	2
Timer start register	TSTR	8	H'FEB0	TPU	8	2
Timer synchro register	TSYR	8	H'FEB1	TPU	8	2
Interrupt priority register A	IPRA	8	H'FEC0	INT	8	2
Interrupt priority register B	IPRB	8	H'FEC1	INT	8	2
Interrupt priority register C	IPRC	8	H'FEC2	INT	8	2
Interrupt priority register D	IPRD	8	H'FEC3	INT	8	2
Interrupt priority register E	IPRE	8	H'FEC4	INT	8	2
Interrupt priority register F	IPRF	8	H'FEC5	INT	8	2
Interrupt priority register G	IPRG	8	H'FEC6	INT	8	2
Interrupt priority register H	IPRH	8	H'FEC7	INT	8	2
Interrupt priority register I	IPRI	8	H'FEC8	INT	8	2
Interrupt priority register J	IPRJ	8	H'FEC9	INT	8	2
Interrupt priority register K	IPRK	8	H'FECA	INT	8	2
Interrupt priority register L	IPRL	8	H'FECB	INT	8	2
Interrupt priority register O	IPRO	8	H'FECE	INT	8	2
Bus width control register	ABWCR	8	H'FED0	BSC	8	2
Access state control register	ASTCR	8	H'FED1	BSC	8	2
Wait control register H	WCRH	8	H'FED2	BSC	8	2
Wait control register L	WCRL	8	H'FED3	BSC	8	2
Bus control register H	BCRH	8	H'FED4	BSC	8	2
Bus control register L	BCRL	8	H'FED5	BSC	8	2
RAM emulation register	RAMER	8	H'FEDB	FLASH	8	2
Memory address register_0AH	MAR_0AH	16	H'FEE0	DMAC	16	2
Memory address register_0AL	MAR_0AL	16	H'FEE2	DMAC	16	2

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
PORTE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORT
PORTF	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	
PORTG	—	—	—	PG4	PG3	PG2	PG1	PG0	

Notes: 1. Some bit names differ depending on whether used in normal mode and Smart Card interface mode.
The name in ( ) indicates the name in Smart Card interface mode.
2. Short address mode
3. Full address mode

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Output high voltage	All output pins*4 except P34 and P35	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA*2
	P34 and P35*3		V_{CC} – 2.0	—	—	V	I_{OH} = –100 µA (reference value)
Output low voltage	All output pins*4	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA
			—	—	0.4	V	I_{OL} = 0.8 mA*2
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0.2 to V_{CC} – 0.2 V
	$\overline{STBY}$, NMI, FWE, MD2 to MD0		—	—	1.0	µA	
	Ports 4, 9		—	—	1.0	µA	V_{in} = 0.2 to AV_{CC} – 0.2 V
Three states leakage current (off)	Ports 1, 3, 7, and A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.2 to V_{CC} – 0.2 V
Input pull-up MOS current	Ports A to E	$-I_P$	10	—	300	µA	V_{in} = 0V

Notes: 1. If the A/D or D/A converter is not used, the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Even if the A/D or D/A converter is not used, connect the AV_{CC} and V_{ref} pins to V_{CC} and supply 2.0 V to 3.6 V. In this case, $V_{ref} \leq AV_{CC}$.

2. V_{CC} = 2.7 V to 3.6 V
3. P35/SCK1 and P34 function as NMOS push-pull output. To output the high voltage, connect an external pull-up resistor.
4. In the case when ICE = 0. Low voltage output with bus driving function is specified in table 27.16.
5. When $V_{CC} < AV_{CC}$, the maximum value for P40 and P41 is V_{CC} + 0.3 V.

Table 27.27 DC Characteristics (2)

Condition A (F-ZTAT version): V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.6 V to 5.5 V,
V_{ref} = 3.6 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)*1

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
	NMI		—	—	30	pF	
	P32 to P35		—	—	20	pF	
	All input pins except the above		—	—	15	pF	
Current dissipation*2	Normal operation	I_{CC}*4	—	23 V_{CC} = 3.0 V	40 V_{CC} = 5.5 V	mA	f = 13.5 MHz
	Sleep mode		—	18 V_{CC} = 3.0 V	30 V_{CC} = 5.5 V	mA	f = 13.5 MHz
	All modules stopped		—	13	—	mA	f = 13.5 MHz, V_{CC} = 3.0 V (reference values)
	Medium-speed mode (ϕ/32)		—	13	—	mA	f = 13.5 MHz, V_{CC} = 3.0 V (reference values)
	Subactive mode		—	80	180	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used
	Subsleep mode		—	60	130	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used
	Watch mode		—	8	40	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used

27.7 Operating Timing

27.7.1 Clock Timing

The clock timing is shown below.

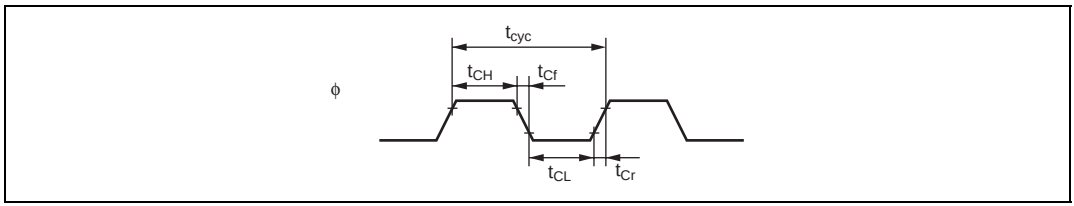


Figure 27.10 System Clock Timing

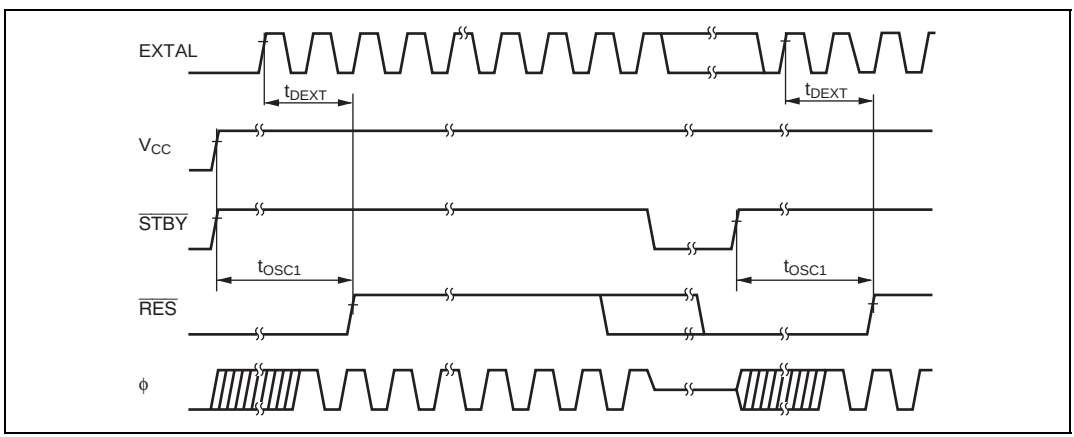


Figure 27.11 Oscillation Stabilization Timing