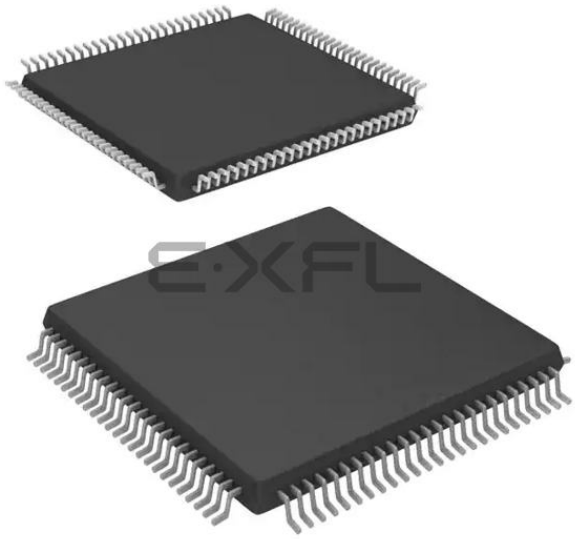

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Product Status	Obsolete
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Core Size	16-Bit
Speed	6MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
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Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
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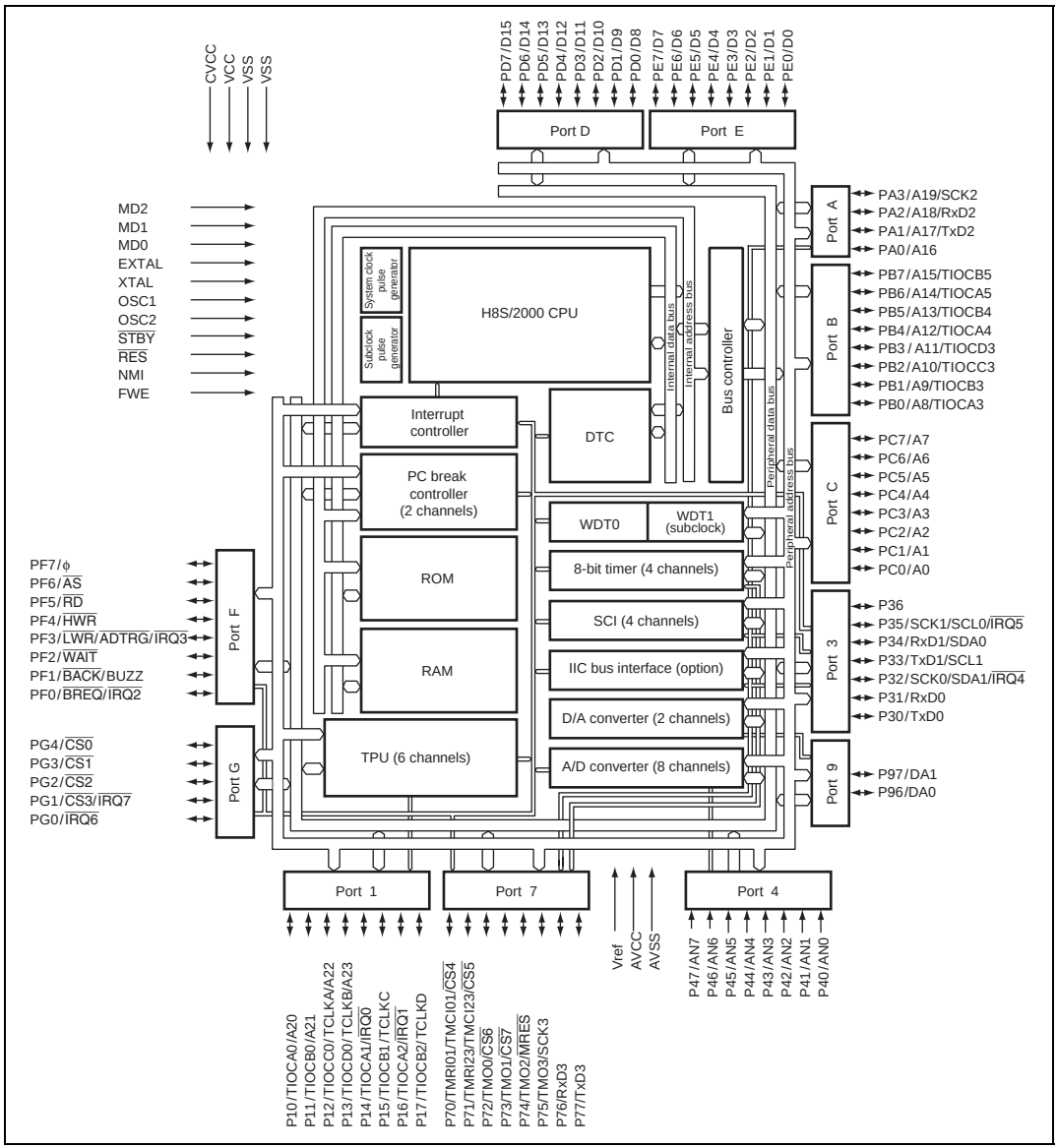


Figure 1.3 Internal Block Diagram of H8S/2238 Group

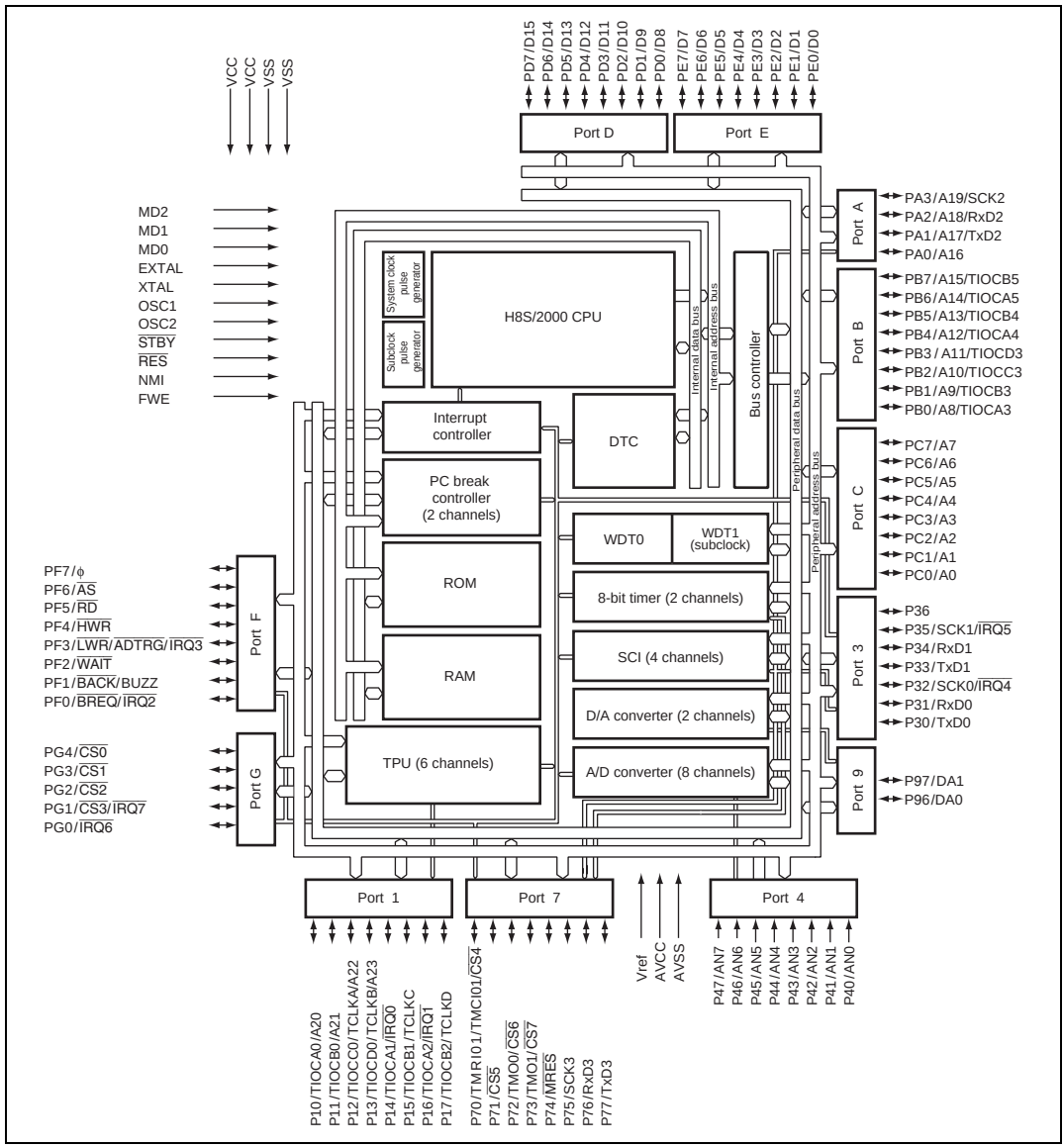


Figure 1.4 Internal Block Diagram of H8S/2237 Group

Section 5 Interrupt Controller

5.1 Features

This LSI controls interrupts with the interrupt controller. The interrupt controller has the following features:

- Two interrupt control modes
  - Any of two interrupt control modes can be set by means of the INTM1 and INTM0 bits in the system control register (SYSCR).
- Priorities settable with IPR
  - An interrupt priority register (IPR) is provided for setting interrupt priorities. Eight priority levels can be set for each module for all interrupts except NMI. NMI is assigned the highest priority level of 8, also accepted (using nesting) during interrupt processing. Additionally accepted during state 12 if Opcode = H'57F3.
- Independent vector addresses
  - All interrupt sources are assigned independent vector addresses, making it unnecessary for the source to be identified in the interrupt handling routine.
- Nine external interrupts
  - NMI is the highest-priority interrupt, and is accepted at all times. Rising edge or falling edge can be selected for NMI. Falling edge, rising edge, or both edge detection, or level sensing, can be independently selected for IRQ7 to IRQ0.
- DTC and DMAC* control
  - The DTC and DMAC* can be activated by an interrupt request.

Note: * Supported only by the H8S/2239 Group.

Table 5.8 Number of States in Interrupt Handling Routine Execution Status

		Object of Access				
			External Device			
			8 Bit Bus		16 Bit Bus	
Symbol		Internal Memory	2-State Access	3-State Access	2-State Access	3-State Access
Instruction fetch	S_I	1	4	6 + 2 m	2	3 + m
Branch address read	S_J					
Stack manipulation	S_K					

Legend:
m: Number of wait states in an external device access.

5.5.6 DTC and DMAC* Activation by Interrupt

The DTC and DMAC* can be started by interrupts. The following settings are required for this operation.

1. Interrupt request to the CPU
2. Start request to the DTC
3. Start request to the DMAC*
4. Multiple specification of items 1 to 3.

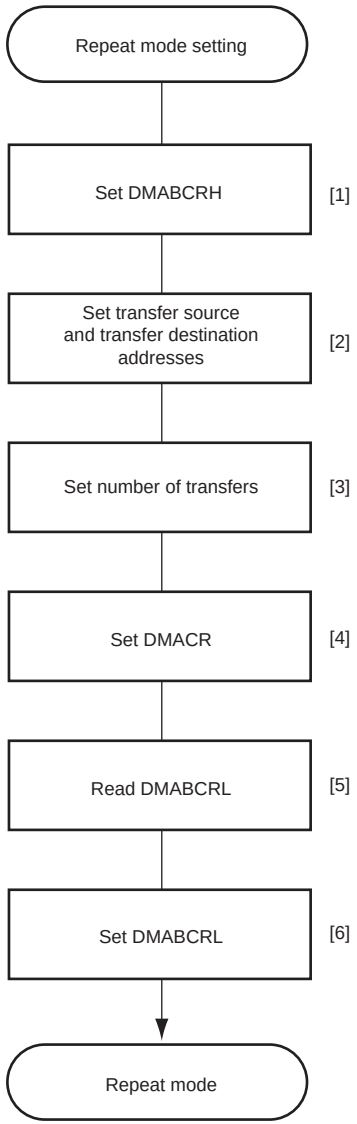
See section 8, DMA Controller (DMAC)*, and section 9, Data Transfer Controller (DTC) for more information on the interrupts that can start the DTC and DMAC*.

Figure 5.8 shows the block diagram of the DTC, DMAC*, and interrupt controller circuits.

Note: * Supported only by the H8S/2239 Group.

Transfer requests (activation sources) consist of A/D converter conversion end interrupts, external requests, SCI transmit-data-empty and receive-data-full interrupts, and TPU channel 0 to 5 compare match/input capture A interrupts. External requests can only be specified for channel B.

Figure 8.8 shows an example of the setting procedure for repeat mode.



[1] Set each bit in DMABCRH.
- Clear the FAE bit to 0 to select short address mode.
- Specify enabling or disabling of internal interrupt clearing with the DTA bit.

[2] Set the transfer source address and transfer destination address in MAR and IOAR.

[3] Set the number of transfers in both ETCRH and ETCRL.

[4] Set each bit in DMACR.
- Set the transfer data size with the DTSZ bit.
- Specify whether MAR is to be incremented or decremented with the DTID bit.
- Set the RPE bit to 1.
- Specify the transfer direction with the DTDIR bit.
- Select the activation source with bits DTF3 to DTF0.

[5] Read the DTE bit in DMABCRL as 0.

[6] Set each bit in DMABCRL.
- Clear the DTIE bit to 0.
- Set the DTE bit to 1 to enable transfer.

Figure 8.8 Example of Repeat Mode Setting Procedure

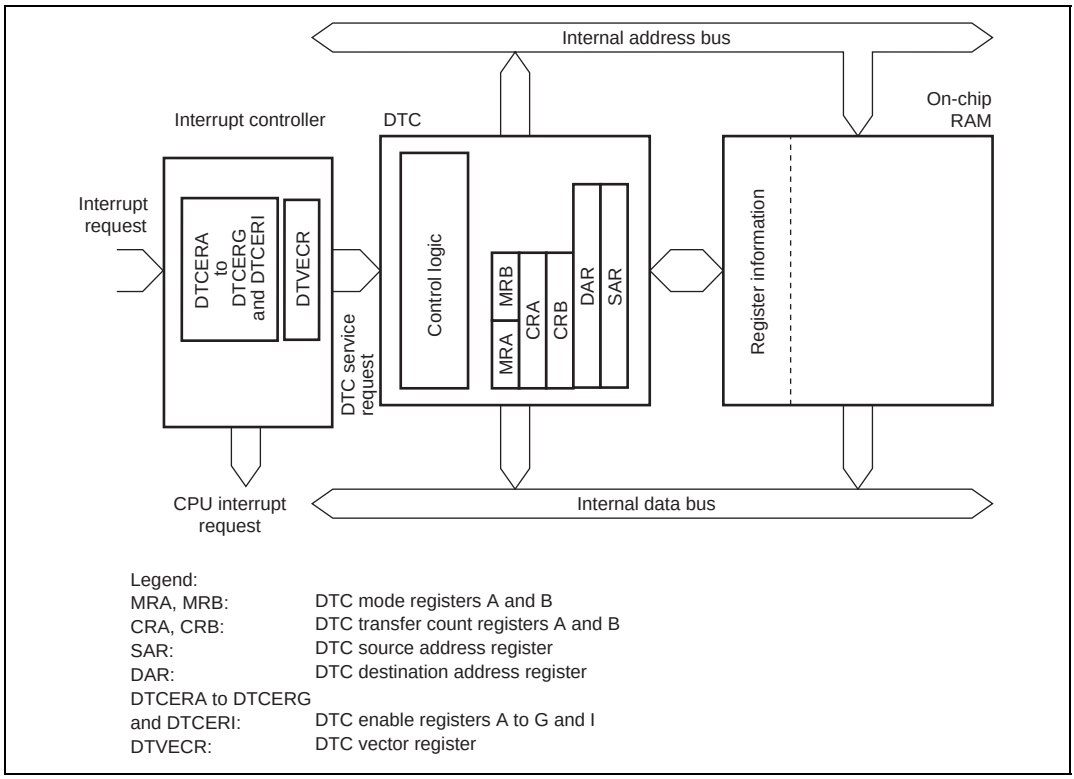


Figure 9.1 Block Diagram of DTC

9.2 Register Descriptions

The DTC has the following registers.

- DTC mode register A (MRA)
- DTC mode register B (MRB)
- DTC source address register (SAR)
- DTC destination address register (DAR)
- DTC transfer count register A (CRA)
- DTC transfer count register B (CRB)

These six registers cannot be directly accessed from the CPU.

When activated, the DTC reads a set of register information that is stored in on-chip RAM to the corresponding DTC registers and transfers data. After the data transfer, it writes a set of updated register information back to the RAM.

Table 9.2 Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs

Interrupt Source	Origin of Interrupt Source	Vector Number	DTC Vector Address	DTCE[*1]	Priority
Software	Write to DTVECR	DTVECR	H'0400 + vector number × 2	—	High
External pin	IRQ0	16	H'0420	DTCEA7	
	IRQ1	17	H'0422	DTCEA6	
	IRQ2	18	H'0424	DTCEA5	
	IRQ3	19	H'0426	DTCEA4	
	IRQ4	20	H'0428	DTCEA3	
	IRQ5	21	H'042A	DTCEA2	
	IRQ6	22	H'042C	DTCEA1	
	IRQ7	23	H'042E	DTCEA0	
A/D converter	ADI (A/D conversion end)	28	H'0438	DTCEB6	
TPU Channel 0	TGI0A	32	H'0440	DTCEB5	
	TGI0B	33	H'0442	DTCEB4	
	TGI0C	34	H'0444	DTCEB3	
	TGI0D	35	H'0446	DTCEB2	
TPU Channel 1	TGI1A	40	H'0450	DTCEB1	
	TGI1B	41	H'0452	DTCEB0	
TPU Channel 2	TGI2A	44	H'0458	DTCEC7	
	TGI2B	45	H'045A	DTCEC6	
TPU Channel 3[*4]	TGI3A	48	H'0460	DTCEC5	
	TGI3B	49	H'0462	DTCEC4	
	TGI3C	50	H'0464	DTCEC3	
	TGI3D	51	H'0466	DTCEC2	
TPU Channel 4[*4]	TGI4A	56	H'0470	DTCEC1	
	TGI4B	57	H'0472	DTCEC0	
TPU Channel 5[*4]	TGI5A	60	H'0478	DTCED5	
	TGI5B	61	H'047A	DTCED4	
8-bit timer channel 0	CMIA0	64	H'0480	DTCED3	
	CMIB0	65	H'0482	DTCED2	Low

- P35/SCK1/SCL0/$\overline{\text{IRQ5}}$

  The pin functions are switched as shown below according to the combination of the ICE bit*3 in ICCR_0 of IIC_0, the C/$\overline{\text{A}}$ bit in SMR_1 of SCI_1, CKE0 and CKE1 bits in SCR_1, and the P35DDR bit. To use this port as SCL0 I/O pin, clear the C/$\overline{\text{A}}$ bit, CKE1 bit, and CKE0 bit to 0.

  The SCL0 functions as NMOS open drain output and the pin can drive bus directly. When this pin is specified as the P35 output pin or SCK1 output pin, it functions as NMOS push/pull output.*4

ICE*3	0					1
CKE1	0				1	0
C/$\overline{\text{A}}$	0			1	—	0
CKE0	0		1	—	—	0
P35DDR	0	1	—	—	—	—
Pin functions	P35 input pin	P35 output pin*1	SCK1 output pin*1	SCK1 output pin*1	SCK1 input pin	SCL0 I/O pin*3
	$\overline{\text{IRQ5}}$ Input pin*2					

Notes: 1. When the P35ODR is set to 1, it functions as NMOS open drain output. When the P35ODR is cleared to 0, it functions as NMOS push/pull output.*4
2. When this pin is used as an external interrupt pin, do not specify other functions.
3. Not available in the H8S/2237 Group and H8S/2227 Group.
4. It functions as CMOS output in the H8S/2237 Group and H8S/2227 Group.

- P34/RxD1/SDA0

  The pin functions are switched as shown below according to the combination of the ICE bit*2 in ICCR_0 of IIC_0, the RE bit in SCR_1 of SCI_1, and the P34DDR bit. When this pin is specified as P34 output pin, it functions as NMOS push-pull output.*3 The SDA0 also functions as NMOS open drain outputs and can drive bus directly.

ICE*2	0			1
RE	0		1	—
P34DDR	0	1	—	—
Pin functions	P34 input pin	P34 output pin*1	RxD1 input pin	SDA0 I/O pin*2

Notes: 1. When P34ODR is set to 1, it functions as NMOS open drain output. When the P34ODR is cleared to 0, it functions as NMOS push/pull output.*3
2. Not available in theH8S/2237 Group and H8S/2227 Group.
3. It functions as CMOS output in the H8S/2237 Group and H8S/2227 Group.

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
DTC activation	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture
DMAC*2 activation	TGRA_0 compare match or input capture	TGRA_1 compare match or input capture	TGRA_2 compare match or input capture	TGRA_3 compare match or input capture	TGRA_4 compare match or input capture	TGRA_5 compare match or input capture
A/D converter trigger	TGRA_0 compare match or input capture	TGRA_1 compare match or input capture	TGRA_2 compare match or input capture	TGRA_3 compare match or input capture	TGRA_4 compare match or input capture	TGRA_5 compare match or input capture
Interrupt sources	5 sources • Compare match or input capture 0A • Compare match or input capture 0B • Compare match or input capture 0C • Compare match or input capture 0D • Overflow	4 sources • Compare match or input capture 1A • Compare match or input capture 1B • Overflow • Underflow	4 sources • Compare match or input capture 2A • Compare match or input capture 2B • Overflow • Underflow	5 sources • Compare match or input capture 3A • Compare match or input capture 3B • Compare match or input capture 3C • Compare match or input capture 3D • Overflow	4 sources • Compare match or input capture 4A • Compare match or input capture 4B • Overflow • Underflow	4 sources • Compare match or input capture 5A • Compare match or input capture 5B • Overflow • Underflow

Legend:

O: Possible

—: Not possible

Notes: 1. Not available in the H8S/2227 Group.

2. Supported only by the H8S/2239 Group.

11.3.1 Timer Control Register (TCR)

The TCR registers control the TCNT operation for each channel. The TPU of the H8S/2227 Group has a total of three TCR registers, one each for channels 0 to 2. In other groups, the TPU has a total of six TCR registers, one each for channels 0 to 5. TCR register settings should be made only when TCNT operation is stopped.

Bit	Bit Name	Initial Value	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	These bits select the TCNT counter clearing source. See tables 11.3 and 11.4 for details.
5	CCLR0	0	R/W	
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge. When the input clock is counted using both edges, the input clock period is halved (e.g. ϕ/4 both edges = ϕ/2 rising edge). If phase counting mode is used on channels 1, 2, 4*, and 5*, this setting is ignored and the phase counting mode setting has priority. Internal clock edge selection is valid when the input clock is ϕ/4 or slower. When the input clock is ϕ/1 or when overflow/underflow of another channel is selected, this setting is ignored and the input clock is counted at the falling edge of ϕ. 00: Count at rising edge 01: Count at falling edge 1×: Count at both edges Legend: ×: Don't care
2	TPSC2	0	R/W	Time Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT counter clock. The clock source can be selected independently for each channel. See tables 11.5 to 11.10 for details.
0	TPSC0	0	R/W	

Note: * Not available in the H8S/2227 Group.

Table 11.9 TPSC2 to TPSC0 (Channel 4)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
4*	0	0	0	Internal clock: counts on ϕ/1
			1	Internal clock: counts on ϕ/4
		1	0	Internal clock: counts on ϕ/16
			1	Internal clock: counts on ϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKC pin input
		1	0	Internal clock: counts on ϕ/1024
			1	Counts on TCNT5 overflow/underflow

Notes: This setting is ignored when channel 4 is in phase counting mode.

* Not available in the H8S/2227 Group.

Table 11.10 TPSC2 to TPSC0 (Channel 5)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
5*	0	0	0	Internal clock: counts on ϕ/1
			1	Internal clock: counts on ϕ/4
		1	0	Internal clock: counts on ϕ/16
			1	Internal clock: counts on ϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKC pin input
		1	0	Internal clock: counts on ϕ/256
			1	External clock: counts on TCLKD pin input

Notes: This setting is ignored when channel 5 is in phase counting mode.

* Not available in the H8S/2227 Group.

Table 11.16 TIORH_3

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_3 Function*2**	**TIOCB3 Pin Function*2**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCB3 pin Input capture at rising edge
			1		Capture input source is TIOCB3 pin Input capture at falling edge
		1	×		Capture input source is TIOCB3 pin Input capture at both edges
	1	×	×		Capture input source is channel 4/count clock Input capture at TCNT_4 count-up/count-down*1

Legend: ×: Don't care

Notes: 1. When bits TPSC2 to TPSC0 in TCR_4 are set to B'000 and φ/1 is used as the TCNT_4 count clock, this setting is invalid and input capture is not generated.

2. Not available in the H8S/2227 Group.

(When ϕ = 12 MHz)

Field name	Header		Master address field		Slave address field			Control field			Message length field			Data field					
Number of bits	1	1	12	1	12	1	1	4	1	1	8	1	1	8	1	1	8	1	1
	Start bit	Broad-cast bit	Master address	P	Slave address	P	A	Control bits	P	A	Message length bits	P	A	Data bits	P	A	Data bits	P	A
Transfer time																			
Mode 0	Approximately 7330 µs													Approximately 1590 × N µs					
Mode 1	Approximately 2090 µs													Approximately 410 × N µs					
Mode 2	Approximately 1590 µs													Approximately 300 × N µs					

P: Parity bit (1 bit)
A: Acknowledge bit (1 bit)
When A = 0: ACK
When A = 1: NAK
N: Number of bytes

Note: The value of acknowledge bit is ignored in broadcast communications.

Figure 14.2 Transfer Signal Format

(1) Header

Header is comprised of a start bit and a broadcast bit.

(a) Start Bit

The start bit is a signal for informing a start of data transfer to other units. A unit, which attempts to start data transfer, outputs a low-level signal (start bit) for a specified period and then outputs the broadcast bit.

If another unit is already outputting a start bit when a unit attempts to output a start bit, the unit waits for completion of output of the start bit from the other unit without outputting the start bit, and then outputs the broadcast bit synchronized with the completion timing.

Other units enter the receive state after detecting the start bit.

(b) Broadcast Bit

The broadcast bit is a bit to identify the type of communications: broadcast or normal.

When this bit is cleared to 0, it indicates the broadcast communications. When it is set to 1, it indicates the normal communications. Broadcast communications includes group broadcast and general broadcast, which are identified by a value of the slave address. (For details of the slave address, see section 14.1.2 (3), Slave Address Field.)

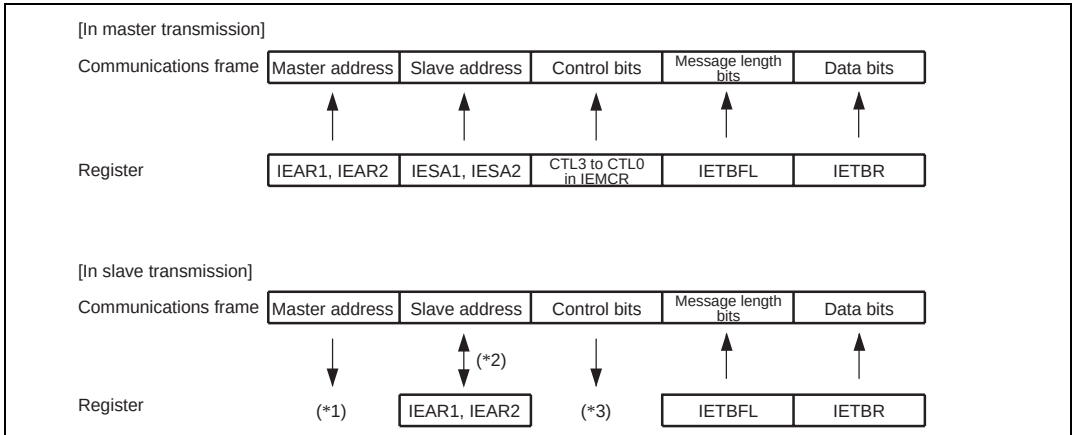
Since there are multiple slave units, which are communications destination units, in the case of broadcast communications, the acknowledge bit is not returned from each field described in (2) and below.

14.3.9 IEBus Transmit Buffer Register (IETBR)

IETBR is a 1-byte buffer to which data to be transmitted in master or slave transmission is written. IETBR is empty when the TxRDY flag in IETSR is 1. Check the TxRDY flag before setting transmit data in IETBR.

Data written in IETBR is transmitted in the data field in master or slave transmission. Figure 14.6 shows the correspondence between the communications signal format and registers for IEBus data transfer.

Bit	Bit Name	Initial Value	R/W	Description
7	TBR7	0	R/W	Data to be transmitted is written to this 1-byte buffer.
6	TBR6	0	R/W	
5	TBR5	0	R/W	
4	TBR4	0	R/W	
3	TBR3	0	R/W	
2	TBR2	0	R/W	
1	TBR1	0	R/W	
0	TBR0	0	R/W	



Notes: 1. In slave transmission, the received master address is not saved. If the unit is locked, address comparison performed.
2. The received slave address is compared with IEAR1 and IEAR2, and if these addresses match, operation continues.
3. In slave transmission, the received control bits are not saved. The received control bits are decoded to decide the subsequent operation.

Figure 14.6 Transmission Signal Format and Registers in Data Transfer

Bit	Bit Name	Initial Value	R/W	Description
3	ACKE	0	R/W	Acknowledge Bit Judgement Selection 0: The value of the acknowledge bit is ignored, and continuous transfer is performed. The value of the received acknowledge bit is not indicated by the ACKB bit, which is always 0. 1: If the acknowledge bit is 1, continuous transfer is interrupted. In this LSI, the DTC can be used to perform continuous transfer. The DTC is activated when the IRTR interrupt flag is set to 1 (IRTR us one of two interrupt flags, the other being IRIC). When the ACKE bit is 0, the TDRE, IRIC, and IRTR flags are set on completion of data transmission, regardless of the acknowledge bit. When the ACKE bit is 1, the TDRE, IRIC, and IRTR flags are set on completion of data transmission when the acknowledge bit is 0, and the IRIC flag alone is set on completion of data transmission when the acknowledge bit is 1. When the DTC is activated, the TDRE, IRIC, and IRTR flags are cleared to 0 after the specified number of data transfers have been executed. Consequently, interrupts are not generated during continuos data transfer, but if data transmission is completed with a 1 acknowledge bit when the ACKE bit is set to 1, the DTC is not activated and an interrupt is generated, if enabled. Depending on the receiving device, the acknowledge bit may be significant, in indicating completion of processing of the received data, for instance, or may be fixed at 1 and have no significance.
2	BBSY	0	R/W	Bus Busy In slave mode, reading the BBSY flag enables to confirm whether the I²C bus is occupied or released. The BBSY flag is set to 0 when the SDA level changes from high to low under the condition of SCl = high, assuming that the start condition has been issued. The BBSY flag is cleared to 0 when the SDA level changes from low to high under the condition of SCl = high, assuming that the start condition has been issued. Writing to the BBSY flag in slave mode is disabled. In master mode, the BBSY flag is used to issue start and stop conditions. Write 1 to BBSY and 0 to SCP to issue a start condition. Follow this procedure when also re-transmitting a start condition. To issue a start/stop condition, use the MOV instruction. The I²C bus interface must be set in master transmit mode before the issue of a start condition.

17.3.2 A/D Control/Status Register (ADCSR)

ADCSR controls A/D conversion operations.

Bit	Bit Name	Initial Value	R/W	Description
7	ADF	0	R/(W)*	A/D End Flag A status flag that indicates the end of A/D conversion. [Setting conditions] • When A/D conversion ends in single mode • When A/D conversion ends on all specified channels in scan mode [Clearing conditions] • When 0 is written after reading ADF = 1 • When the data transfer controller (DTC) is activated by an ADI interrupt and DISEL in DTC is 0 with the transfer counter not being 0
6	ADIE	0	R/W	A/D Interrupt Enable A/D conversion end interrupt (ADI) request enabled when 1 is set
5	ADST	0	R/W	A/D Start Clearing this bit to 0 stops A/D conversion, and the A/D converter enters the wait state. Setting this bit to 1 starts A/D conversion. In single mode, this bit is cleared to 0 automatically when conversion on the specified channel is complete. In scan mode, conversion continues sequentially on the specified channels until this bit is cleared to 0 by software, a reset, software standby mode, hardware standby mode, or module stop mode. The ADST bit can be set to 1 by software, a timer conversion start trigger, or the A/D external trigger input pin ($\overline{\text{ADTRG}}$).

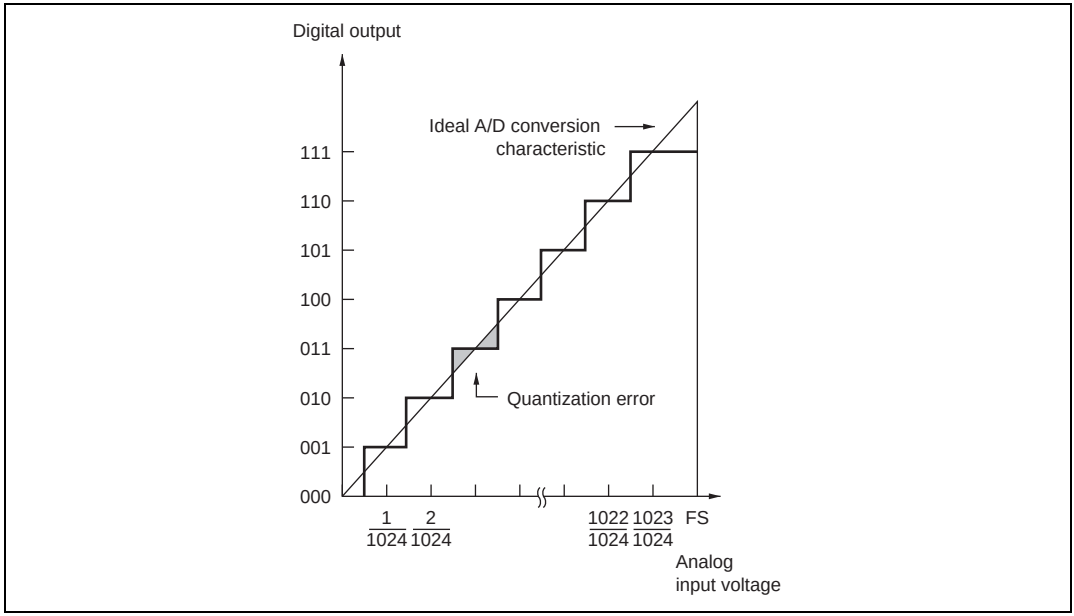


Figure 17.7 A/D Conversion Accuracy Definitions

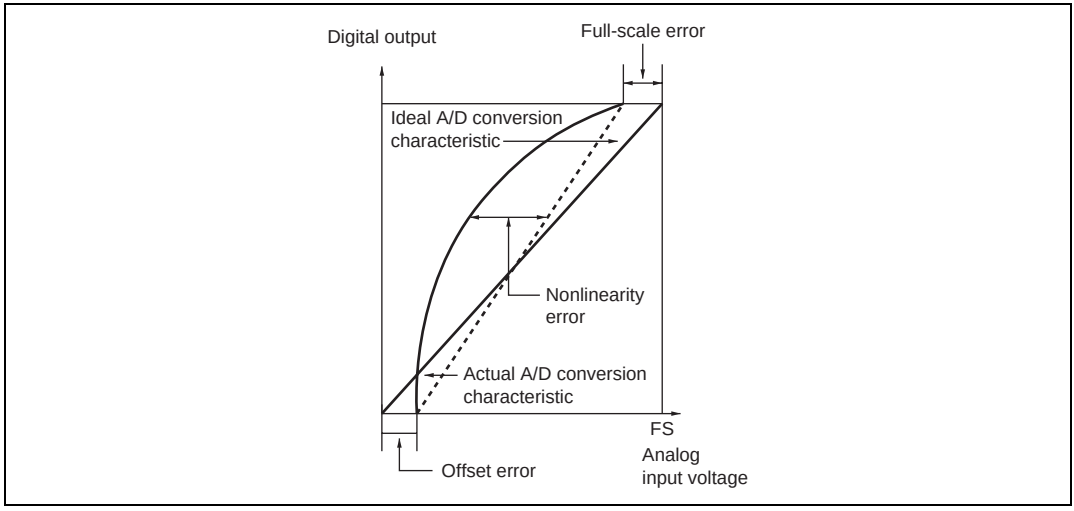


Figure 17.8 A/D Conversion Accuracy Definitions

(1) Clock Timing

Table 27.17 lists the clock timing.

Table 27.17 Clock Timing

Condition A (F-ZTAT version and masked ROM version):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32.768 kHz, 2 to 16.0 MHz, T_a = –20°C to +75°C (regular specifications)

Condition B (Masked ROM version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V, V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32.768 kHz, 2 to 6.25 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C (F-ZTAT version and masked ROM version):
V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32.768 kHz, 10.0 to 20.0 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A			Condition B			Condition C				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Clock cycle time	t_{cyc}	62.5	—	500	160	—	500	50	—	100	ns	Figure 27.10
Clock high pulse width	t_{CH}	20	—	—	50	—	—	17	—	—	ns	
Clock low pulse width	t_{CL}	20	—	—	50	—	—	17	—	—	ns	
Clock rise time	t_{Cr}	—	—	10	—	—	25	—	—	10	ns	
Clock fall time	t_{Cf}	—	—	10	—	—	25	—	—	10	ns	
Oscillation stabilization time at reset (crystal)	t_{OSC1}	20	—	—	40	—	—	20	—	—	ms	Figure 27.11