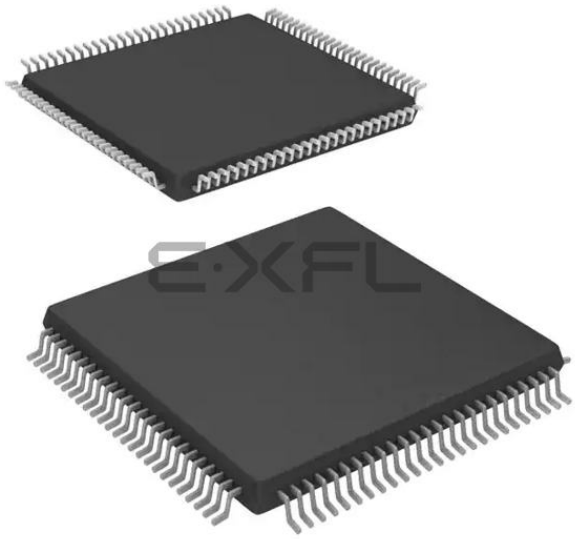

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
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Supplier Device Package	100-TQFP (12x12)
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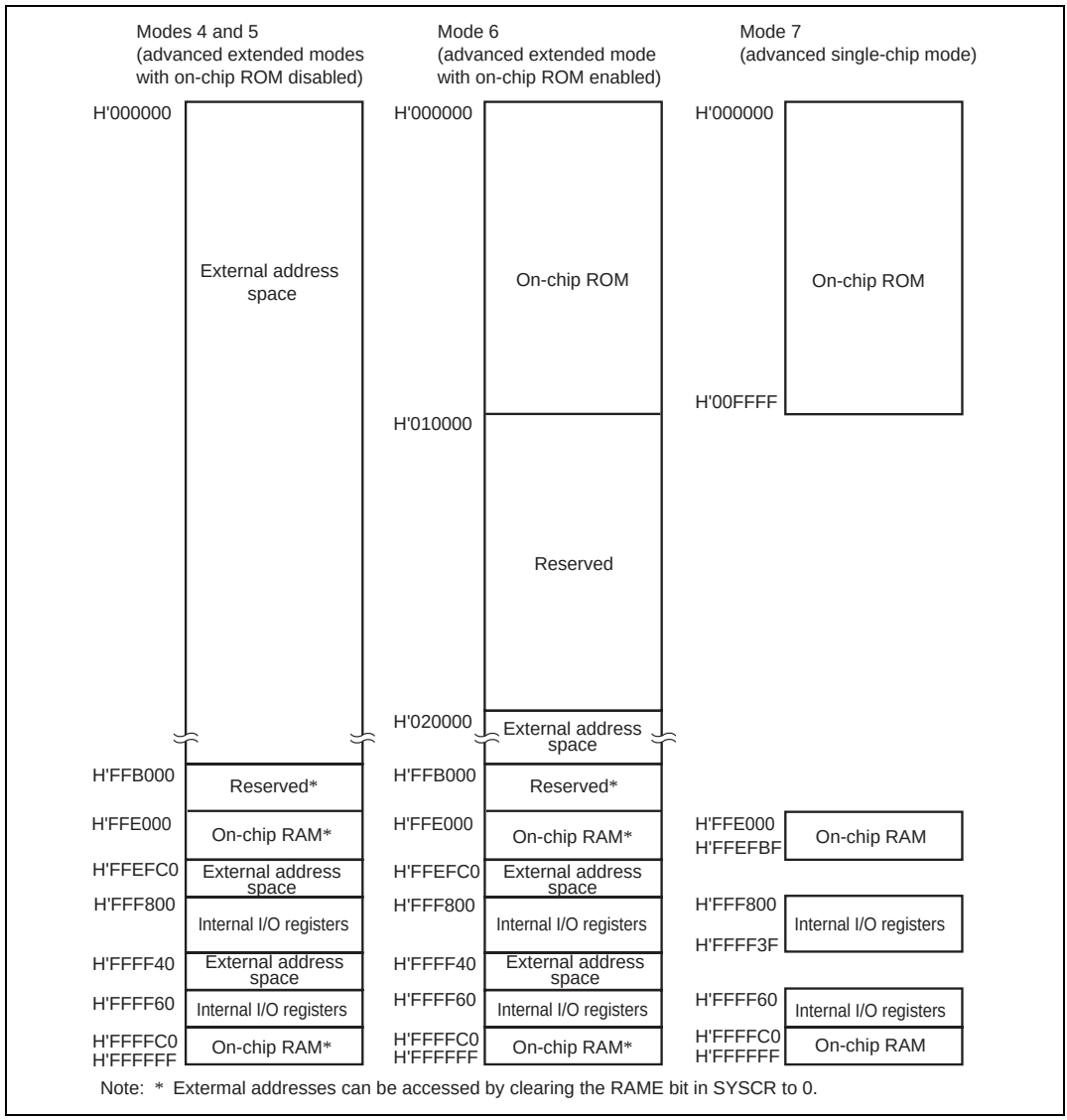
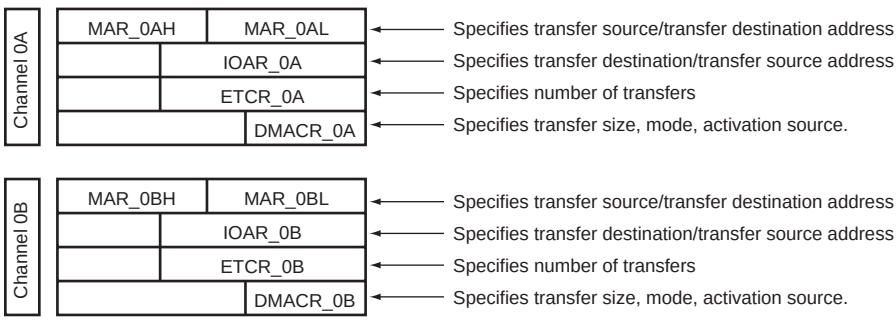
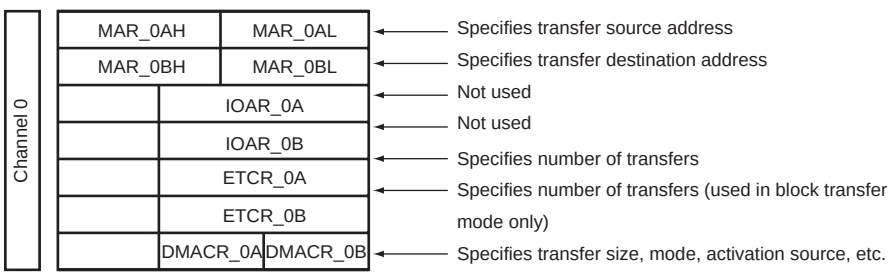


Figure 3.9 H8S/2233 and H8S/2223 Memory Map in Each Operating Mode

- DMA control register_1A (DMACR_1A)
- DMA control register_1B (DMACR_1B)
- DMA band control register H (DMABCRH)
- DMA band control register L (DMABCRL)
- DMA write enable register (DMAWER)
- DMA terminal control register (DMATCR)

The functions of MAR, IOAR, ETCR, DMACR, and DMABCR differ according to the transfer mode (short address mode or full address mode). The transfer mode can be selected by means of the FAE1 and FAE0 bits in DMABCRH. The register configurations for short address mode and full address mode of channel 0 are shown in table 8.2.

Table 8.2 Short Address Mode and Full Address Mode (Channel 0)

FAE0	Description
0	Short address mode specified (channels 0A and 0B operate independently) 
1	Full address mode specified (channels 0A and 0B operate in combination as channel 0) 

chain transfer. When re-setting the control register area, perform masking by setting bits in DMAWER to prevent modification of the contents of other channels.

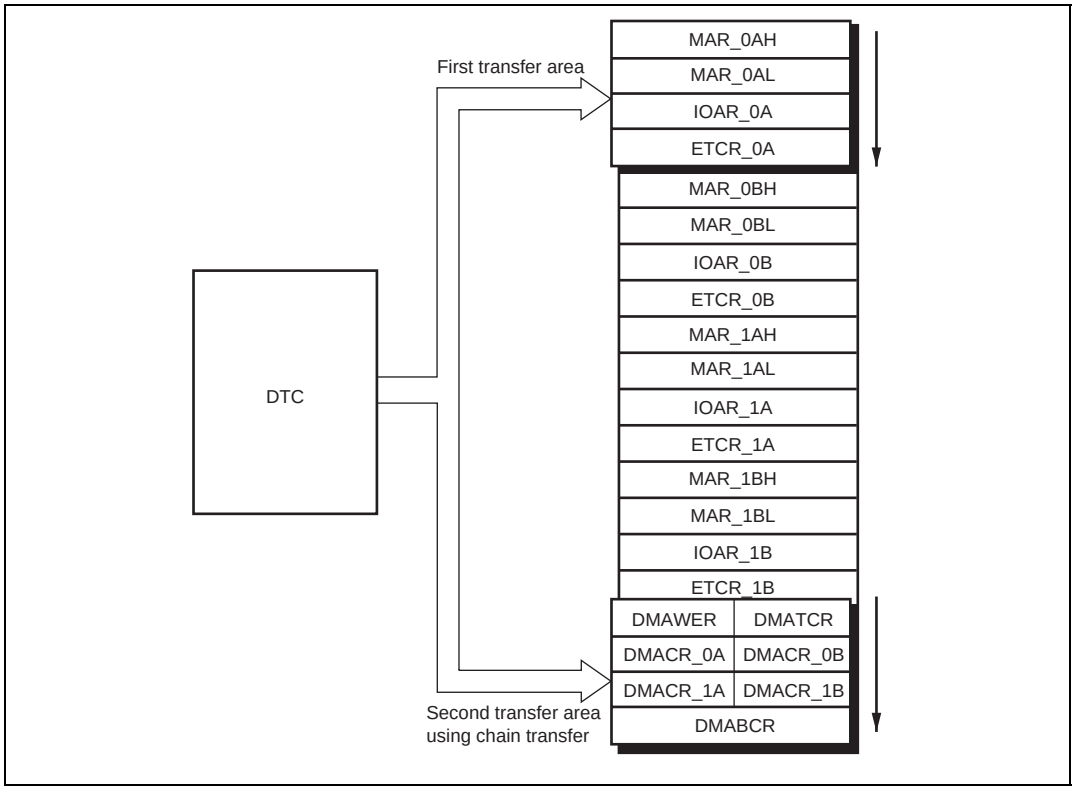


Figure 8.2 Areas for Register Re-Setting by DTC (Channel 0A)

Writes by the DTC to bits 15 to 12 (FAE and SAE) in DMABCR are invalid regardless of the DMAWER settings. These bits should be changed, if necessary, by CPU processing.

In writes by the DTC to bits 7 to 4 (DTE) in DMABCR, 1 can be written without first reading 0. To reactivate a channel set to full address mode, write 1 to both Write Enable A and Write Enable B for the channel to be reactivated.

MAR, IOAR, and ETCR can always be written to regardless of the DMAWER settings. When modifying these registers, the channel to be modified should be halted.

8.5.3 Idle Mode

Idle mode can be specified by setting the RPE bit in DMACR and DTIE bit in DMABCRL to 1. In idle mode, one byte or word is transferred in response to a single transfer request, and this is executed the number of times specified in ETCR. One address is specified by MAR, and the other by IOAR. The transfer direction can be specified by the DTDIR bit in DMACR. Table 8.6 summarizes register functions in idle mode.

Table 8.6 Register Functions in Idle Mode

Register	Function		Initial Setting	Operation
	DTDIR = 0	DTDIR = 1		
23 MAR 0	Source address register	Destination address register	Start address of transfer destination or transfer source	Fixed
23 H'FF 15 IOAR 0	Destination address register	Source address register	Start address of transfer source or transfer destination	Fixed
15 ETCR 0	Transfer counter		Number of transfers	Decremented every transfer; transfer ends when count reaches H'0000

MAR specifies the start address of the transfer source or transfer destination as 24 bits. MAR is neither incremented nor decremented by a data transfer. IOAR specifies the lower 16 bits of the other address. The upper 8 bits of IOAR have a value of H'FF.
Figure 8.5 illustrates operation in idle mode.

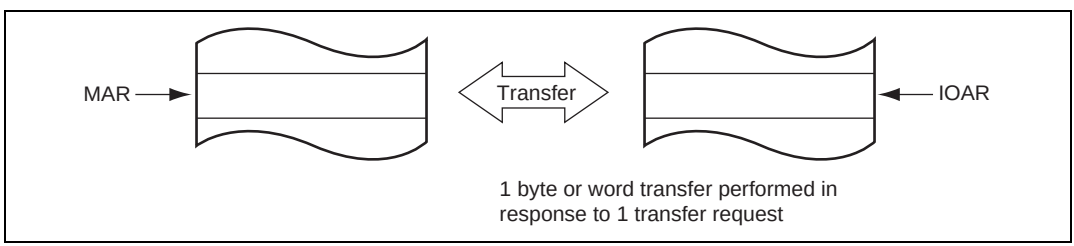


Figure 8.5 Operation in Idle Mode

The number of transfers is specified as 16 bits in ETCR. ETCR is decremented by 1 each time a transfer is executed, and when its value reaches H'0000, the DTE bit is cleared and data transfer ends. If the DTIE bit is set to 1 at this time, an interrupt request is sent to the CPU or DTC. The maximum number of transfers, when H'0000 is set in ETCR, is 65,536.

10.4.2 Port 7 Data Register (P7DR)

P7DR stores output data for port 7 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P77DR	0	R/W	Output data for a pin is stored when the pin is specified as a general purpose output port.
6	P76DR	0	R/W	
5	P75DR	0	R/W	
4	P74DR	0	R/W	
3	P73DR	0	R/W	
2	P72DR	0	R/W	
1	P71DR	0	R/W	
0	P70DR	0	R/W	

10.4.3 Port 7 Register (PORT7)

PORT7 shows the pin states. This register cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	P77	—*	R	If a port 1 read is performed while P7DDR bits are set to 1, the P7DR values are read. If a port 1 read is performed while P7DDR bits are cleared to 0, the pin states are read.
6	P76	—*	R	
5	P75	—*	R	
4	P74	—*	R	
3	P73	—*	R	
2	P72	—*	R	
1	P71	—*	R	
0	P70	—*	R	

Note: * Determined by the states of pins P77 to P70.

- Port B pull-up MOS control register (PBPCR)

10.7.1 Port B Data Direction Register (PBDDR)

PBDDR specifies input or output the port B pins using the individual bits. PBDDR cannot be read; if it is, an undefined value will be read. This register is a write-only register, and cannot be written by bit manipulation instruction. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7DDR	0	W	When a pin is specified as a general purpose I/O port, setting the bit to 1 makes the corresponding port B pin an output pin. Clearing the bit to 0 makes the pin an input pin.
6	PB6DDR	0	W	
5	PB5DDR	0	W	
4	PB4DDR	0	W	
3	PB3DDR	0	W	
2	PB2DDR	0	W	
1	PB1DDR	0	W	
0	PB0DDR	0	W	

10.7.2 Port B Data Register (PBDR)

PBDR stores output data for port B pins.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7DR	0	R/W	Output data for a pin is stored when the pin is specified as a general purpose output port.
6	PB6DR	0	R/W	
5	PB5DR	0	R/W	
4	PB4DR	0	R/W	
3	PB3DR	0	R/W	
2	PB2DR	0	R/W	
1	PB1DR	0	R/W	
0	PB0DR	0	R/W	

10.13 Handling of Unused Pins

Unused input pins should be fixed high or low. Generally, the input pins of CMOS products are high-impedance. Leaving unused pins open can cause the generation of intermediate levels due to peripheral noise induction. This can result in shoot-through current inside the device and cause it to malfunction. Table 10.7 lists examples of ways to handle unused pins. Pins marked NC should be left open.

Table 10.7 Examples of Ways to Handle Unused Input Pins

Port Name	Pin Handling Example
Port 1	Connect each pin to Vcc (pull-up) or to Vss (pull-down) via a resistor.
Port 3	
Port 4	Connect each pin to AVcc (pull-up) or to AVss (pull-down) via a resistor.
Port 7	Connect each pin to Vcc (pull-up) or to Vss (pull-down) via a resistor.
Port 9	Connect each pin to AVcc (pull-up) or to AVss (pull-down) via a resistor.
Port A	Connect each pin to Vcc (pull-up) or to Vss (pull-down) via a resistor.
Port B	
Port C	
Port D	
Port E	
Port F	
Port G	

- TCSR_1

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W) *1	Overflow Flag Indicates that TCNT has overflowed. Only a 0 can be written to this bit, to clear the flag. [Setting condition] When TCNT overflows (changes from H'FF to H'00) When internal reset request generation is selected in watchdog timer mode, OVF is cleared automatically by the internal reset. [Clearing condition] Cleared by reading TCSR*2 when OVF = 1, then writing 0 to OVF
6	WT/$\overline{IT}$	0	R/W	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Interval timer mode (an interval timer interrupt (WOVI) is requested to CPU) 1: Watchdog timer mode (a power-on reset or NMI interrupt is requested to CPU)
5	TME	0	R/W	Timer Enable When this bit is set to 1, TCNT starts counting. When this bit is cleared, TCNT stops counting and is initialized to H'00.
4	PSS	0	R/W	Prescaler Select Selects the clock source input to TCNT of WDT_1 0: TCNT counts divided clock of ϕ-base prescaler (PSM) 1: TCNT counts divided clock of ϕ_{SUB}-base prescaler (PSS)
3	RST/$\overline{NMI}$	0	R/W	Reset or NMI (RST/$\overline{NMI}$) When TCNT overflows in watchdog timer mode, either a power-on reset or NMI interrupt is selected. 0: An NMI interrupt is requested 1: Reset is requested

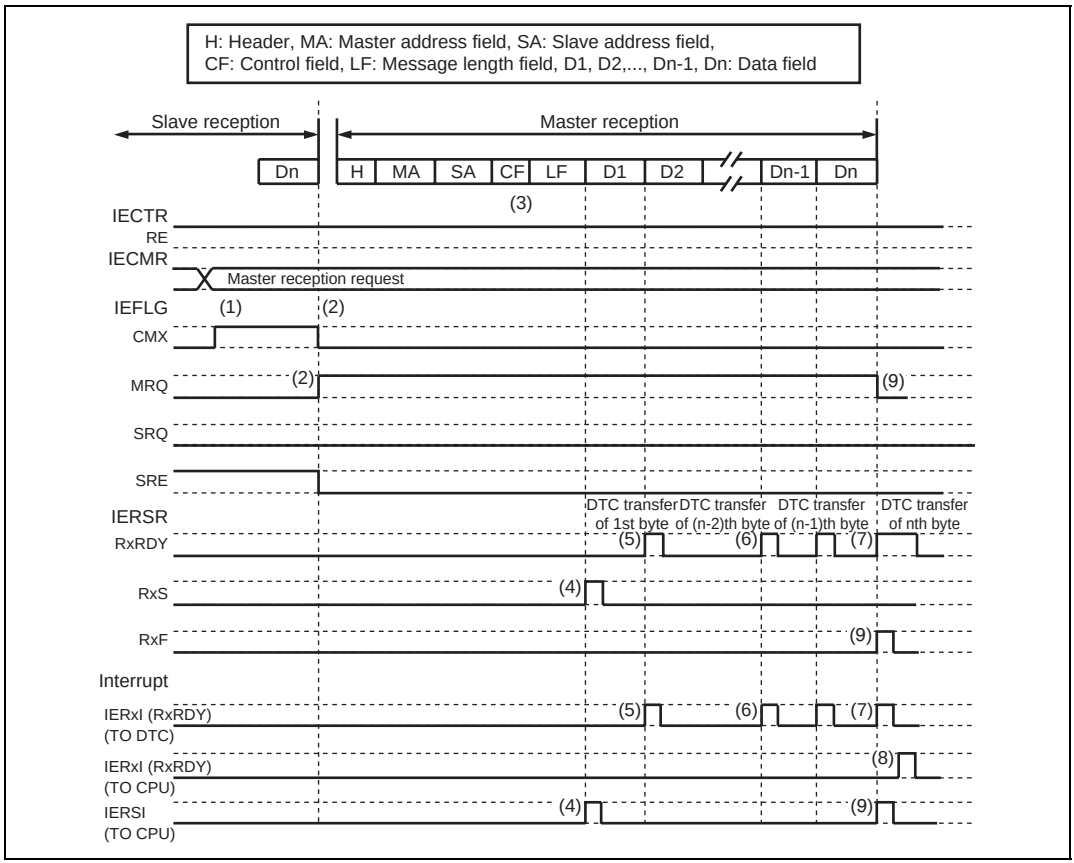


Figure 14.11 Master Receive Operation Timing

14.4.4 Slave Transmission

This section shows an example of performing a slave transmission using the DTC after slave reception.

(1) IEB Initialization

(a) Setting the IEBus Control Register (IECTR)

Enable the IEBus pins, select the signal polarity, and select a clock supplied to the IEB. Clear the LUEE bit to 0 because transfer by the DTC is performed.

(b) Setting the IEBus Master Unit Address Registers 1 and 2 (IEAR1 and IEAR2)

Specify the master unit address and specify the communications mode in IEAR1. Compare with the slave address in the communications frame and receive the frame if matched.

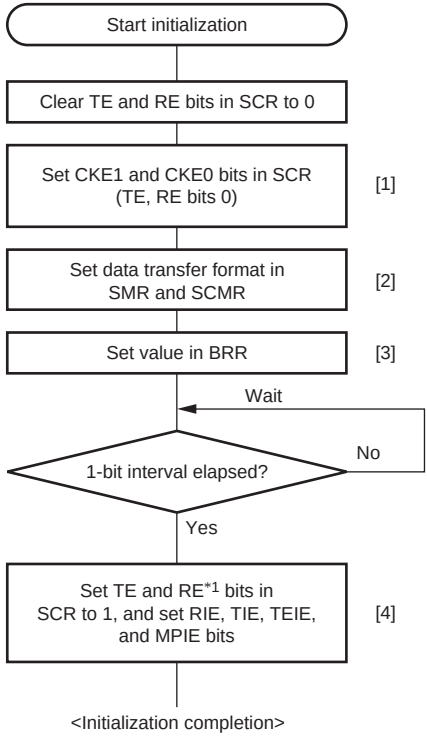
Bit	Bit Name	Initial Value	R/W	Description
1	CKE1	0	R/W	Clock Enable 0 and 1
0	CKE0	0	R/W	Selects the clock source and SCK pin function. Asynchronous mode 00: On-chip baud rate generator SCK pin functions as I/O port 01: On-chip baud rate generator Outputs a clock of the same frequency as the bit rate from the SCK pin. 1×: External clock Inputs a clock with a frequency 16 times the bit rate from the SCK pin. Clocked synchronous mode 0×: Internal clock (SCK pin functions as clock output) 1×: External clock (SCK pin functions as clock input)

Legend:

×: Don’t care

15.4.4 SCI Initialization (Asynchronous Mode)

Before transmitting and receiving data, you should first clear the TE and RE bits in SCR to 0, then initialize the SCI as described in figure 15.8. When the operating mode, or transfer format, is changed for example, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag is set to 1. Note that clearing the RE bit to 0 does not initialize the contents of the RDRF, PER, FER, and ORER flags, or the contents of RDR. When the external clock is used in asynchronous mode, the clock must be supplied even during initialization.



[1] Set the clock selection in SCR. Be sure to clear bits RIE, TIE, TEIE, MPIE, TE, and RE, to 0.

When the clock is selected in asynchronous mode, it is output immediately after SCR settings are made.

[2] Set the data transfer format in SMR and SCMR.

[3] Write a value corresponding to the bit rate to BRR. Not necessary if an external clock or an average transfer rate clock by bits ACS2 to ACS0 in SEMR_0*2 is used.

[4] Wait at least one bit interval, then set the TE bit or RE bit in SCR to 1. Also set the RIE, TIE, TEIE, and MPIE bits.

Setting the TE and RE bits enables the TxD and RxD pins to be used.

Notes: 1. Perform this set operation with the RxD pin in the 1 state. If the RE bit is set to 1 with the RxD pin in the 0 state, it may be misinterpreted as a start bit.
2. Supported only by the H8S/2239 Group.

Figure 15.8 Sample SCI Initialization Flowchart

after checking that the SCI has finished transmission, initialize the SCI, and set TE to 0 and RE to 1. Whether SCI has finished transmission or not can be checked with the TEND flag.

15.7.6 Serial Data Transmission (Except for Block Transfer Mode)

As data transmission in Smart Card interface mode involves error signal sampling and retransmission processing, the operations are different from those in normal serial communication interface mode (except for block transfer mode). Figure 15.29 illustrates the retransfer operation when the SCI is in transmit mode.

1. If an error signal is sent back from the receiving end after transmission of one frame is complete, the ERS bit in SSR is set to 1. If the RIE bit in SCR is enabled at this time, an ERI interrupt request is generated. The ERS bit in SSR should be cleared to 0 by the time the next parity bit is sampled.
2. The TEND bit in SSR is not set for a frame in which an error signal indicating an abnormality is received. Data is retransferred from TDR to TSR, and retransmitted automatically.
3. If an error signal is not sent back from the receiving end, the ERS bit in SSR is not set. Transmission of one frame, including a retransfer, is judged to have been completed, and the TEND bit in SSR is set to 1. If the TIE bit in SCR is enabled at this time, a TXI interrupt request is generated. Writing transmit data to TDR transfers the next transmit data.

Figure 15.31 shows a flowchart for transmission. A sequence of transmit operations can be performed automatically by specifying the DTC to be activated with a TXI interrupt source. In a transmit operation, the TDRE flag is set to 1 at the same time as the TEND flag in SSR is set, and a TXI interrupt will be generated if the TIE bit in SCR has been set to 1. If the TXI request is designated beforehand as a DTC activation source, the DTC will be activated by the TXI request, and transfer of the transmit data will be carried out. At this moment, if DISEL in DTC is 0 with the transfer counter not being 0, the TDRE and TEND flags are automatically cleared to 0 when data is transferred by the DTC. When DISEL is 1, or DISEL is 0 with the transfer counter being 0, the DTC writes the transfer data to the TDR but does not clear the flag. Therefore, the flag should be cleared by CPU. In addition, in the event of the error, the SCI retransmits the same data automatically. During this period, the TEND flag remains cleared to 0 and the DTC is not activated. Therefore, the SCI and DTC will automatically transmit the specified number of bytes in the event of an error, including retransmission. However, the ERS flag is not cleared automatically when an error occurs, and so the RIE bit should be set to 1 beforehand so that an ERI request will be generated in the event of an error, and the ERS flag will be cleared.

When performing transfer using the DTC, it is essential to set and enable the DTC before carrying out SCI setting. For details of the DTC setting procedures, refer to section 9, Data Transfer Controller (DTC).

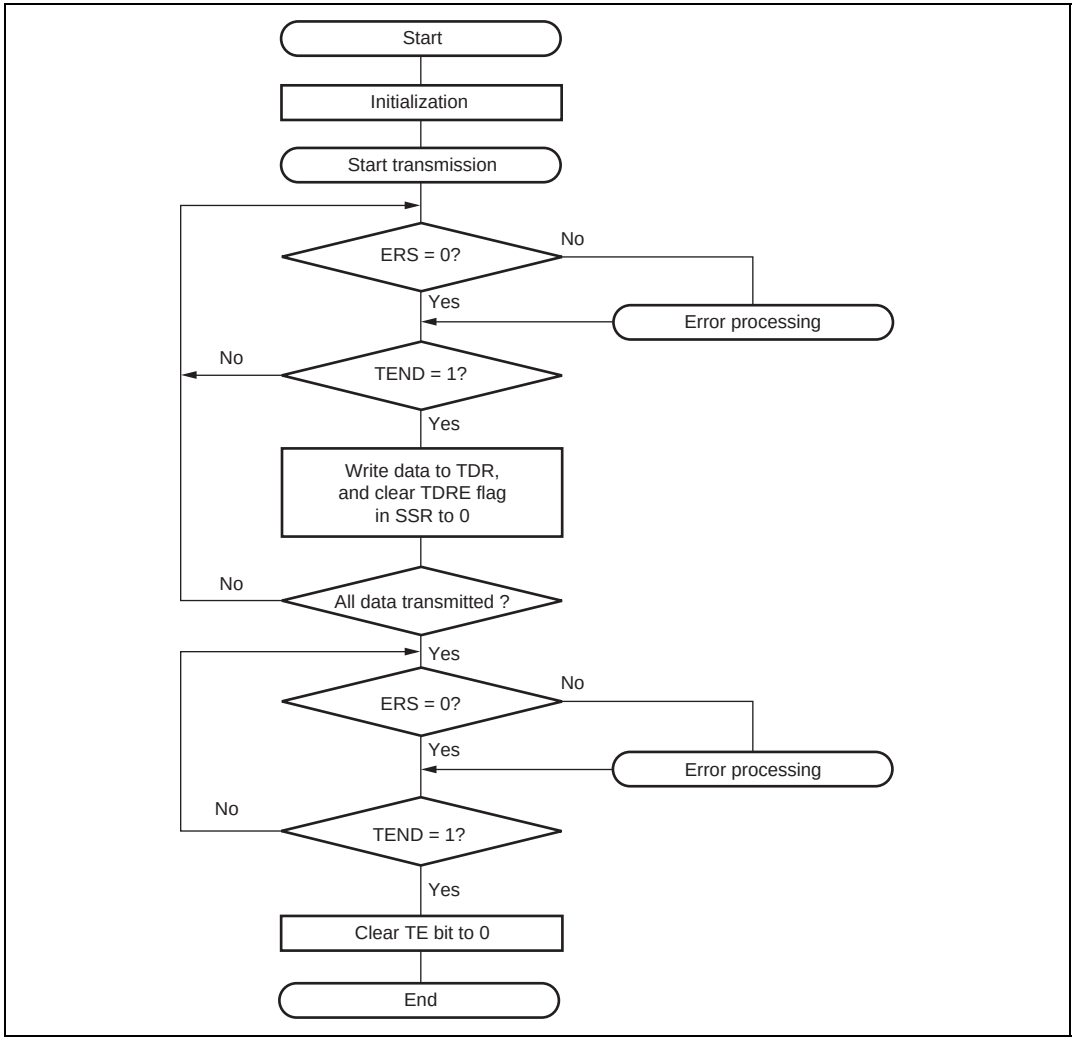


Figure 15.31 Example of Transmission Processing Flow

16.4.6 Slave Transmit Operation

If the slave address matches to the address in the first frame (address reception frame) following the start condition detection when the 8th bit data (R/$\overline{W}$) is 1 (read), the TRS bit in ICCR is automatically set to 1 and the mode changes to slave transmit mode.

Figure 16.17 shows the sample flowchart for the operations in slave transmit mode.

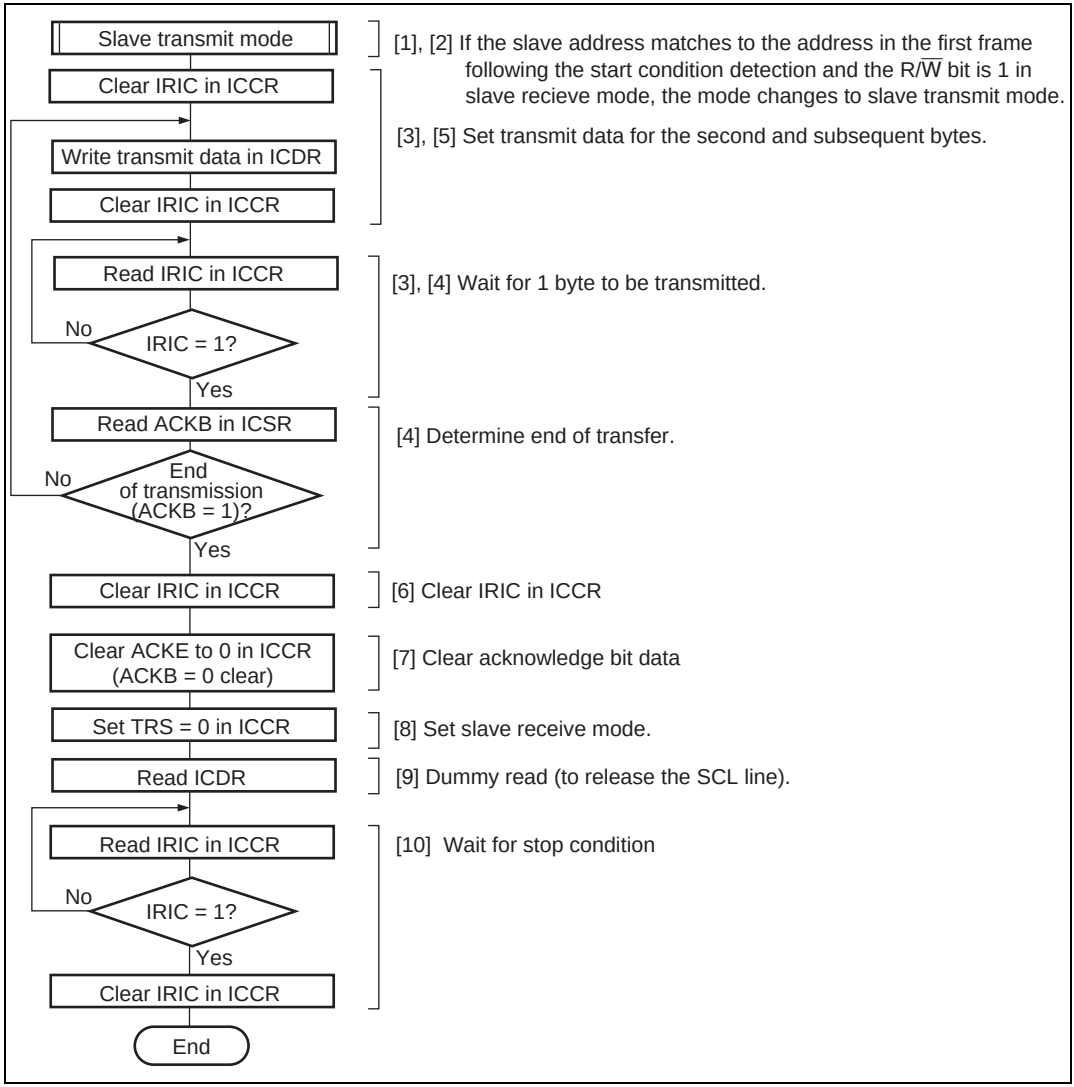


Figure 16.17 Sample Flowchart for Slave Transmit Mode

In slave transmit mode, the slave device outputs the transmit data, while the master device outputs the receive clock and returns an acknowledge signal. The transmission procedure and operations in slave transmit mode are described below.

1. Initialize slave receive mode and wait for slave address reception.
   When making initial settings for slave receive mode, set the ACKE bit in ICCR to 1. This is necessary in order to enable reception of the acknowledge bit after entering slave transmit mode.
2. When the slave address matches in the first frame following detection of the start condition, the slave device drives SDA low at the 9th clock pulse and returns an acknowledge signal. If the 8th data bit (R/$\overline{W}$) is 1, the TRS bit in ICCR is set to 1, and the mode changes to slave transmit mode automatically. The IRIC flag is set to 1 at the rise of the 9th clock. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU. At the same time, the TDRE internal flag is set to 1. The slave device drives SCL low from the fall of the transmit 9th clock until ICDR data is written, to disable the master device to output the next transfer clock.
3. After clearing the IRIC flag to 0, write data to ICDR. At this time, the TDRE internal flag is cleared to 0. The written data is transferred to ICDRS, and the TDRE internal flag and IRIC flag are set to 1 again. The slave device sequentially sends the data written into ICDRS in accordance with the clock output by the master device.

   The IRIC flag is cleared to 0 to detect the end of transmission. Processing from the ICDR register writing to the IRIC flag clearing should be performed continuously. Prevent any processing that includes interrupt processing during this period. If a duration sufficient for one byte of data to be transferred elapses before the IRIC flag is cleared, it will not be possible to determine that the transfer has completed.
4. The master device drives SDA low at the 9th clock pulse, and returns an acknowledge signal. When the value of the ACKE bit in ICSR is 1, the acknowledge signal state is stored in the ACKB bit, so the ACKB bit can be used to determine whether the transfer operation was performed successfully. When one frame of data has been transmitted, the IRIC flag in ICCR is set to 1 at the rise of the 9th transmit clock pulse. When the TDRE internal flag is 0, the data written into ICDR is transferred to ICDRS, transmission starts, and the TDRE internal flag and IRIC flag are set to 1 again. If the TDRE internal flag has been set to 1, this slave device drives SCL low from the fall of the 9th transmit clock until data is written to ICDR.
5. To continue transmission, write the next data to be transmitted into ICDR. The TDRE internal flag is cleared to 0. The IRIC flag is cleared to 0 to detect the end of transmission. Processing from the ICDR writing to the IRIC flag clearing should be performed continuously. Prevent any processing that includes interrupt processing during this period.

Transmit operations can be performed continuously by repeating steps [4] and [5].

17.5 Operation

The A/D converter operates by successive approximation with 10-bit resolution. It has two operating modes; single mode and scan mode. When changing the operating mode or analog input channel, in order to prevent incorrect operation, first clear the bit ADST to 0 in ADCSR. The ADST bit can be set at the same time as the operating mode or analog input channel is changed.

17.5.1 Single Mode

In single mode, A/D conversion is to be performed only once on the specified single channel. The operations are as follows.

1. A/D conversion is started when the ADST bit is set to 1, according to software, timer conversion start trigger, or external trigger input.
2. When A/D conversion is completed, the result is transferred to the corresponding A/D data register to the channel.
3. On completion of conversion, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt request is generated.
4. The ADST bit remains set to 1 during A/D conversion. When A/D conversion ends, the ADST bit is automatically cleared to 0 and the A/D converter enters the wait state.

- MSTPCRC

Bit	Bit Name	Initial Value	R/W	Target Module
7	MSTPC7	1	R/W	Serial communication interface 3 (SCI_3)
6	MSTPC6*1	1	R/W	
5	MSTPC5	1	R/W	D/A converter*4
4	MSTPC4	1	R/W	PC break controller (PBC)
3	MSTPC3	1	R/W	IEBus controller (IEB)*5
2	MSTPC2*1	1	R/W	
1	MSTPC1*1	1	R/W	
0	MSTPC0*1	1	R/W	

Notes: 1. Bits MSTPA3, MSTPA2, MSTPB5, MSTPB2 to MSTPB0, MSTPC6, MSTPC2 to MSTPC0 are readable/writable. The initial value of them is 1. The write value should always be 1.
2. Supported only by the H8S/2239 Group.
3. Not available in the H8S/2237 Group and H8S/2227 Group.
4. Not available in the H8S/2227 Group.
5. Supported only by the H8S/2258 Group.

24.2 Medium-Speed Mode

In high-speed mode, when the SCK2 to SCK0 bits in SCKCR are set to 1, the operating mode changes to medium-speed mode as soon as the current bus cycle ends. In medium-speed mode, the CPU operates on the operating clock (φ/2, φ/4, φ/8, φ/16, or φ/32) specified by the SCK2 to SCK0 bits. The bus masters other than the CPU (DMAC* and DTC) also operate in medium-speed mode.

On-chip peripheral modules other than the bus masters always operate on the high-speed clock (φ).

In medium-speed mode, a bus access is executed in the specified number of states with respect to the bus master operating clock. For example, if φ/4 is selected as the operating clock, on-chip memory is accessed in 4 states, and internal I/O registers in 8 states.

Medium-speed mode is cleared by clearing all of bits SCK2 to SCK0 to 0. A transition is made to high-speed mode and medium-speed mode is cleared at the end of the current bus cycle.

If a SLEEP instruction is executed when the SSBY bit in SBYCR is cleared to 0, and LSON bit in LPWRCR is cleared to 0, a transition is made to sleep mode. When sleep mode is cleared by an interrupt, medium-speed mode is restored.

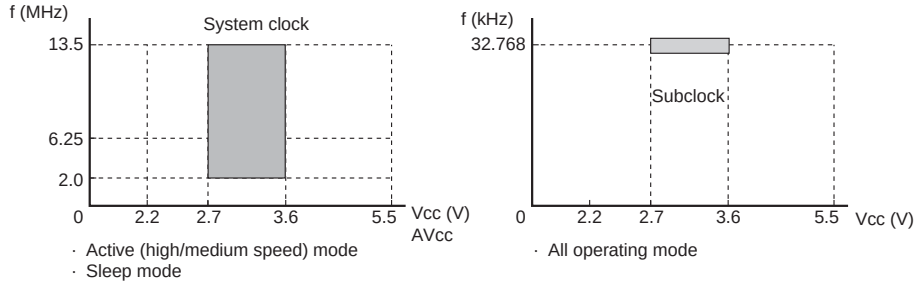
26.2 Register Bits

Register addresses and bit names of the on-chip peripheral modules are described below.

Each line covers eight bits, and 16-bit register is shown as 2 lines.

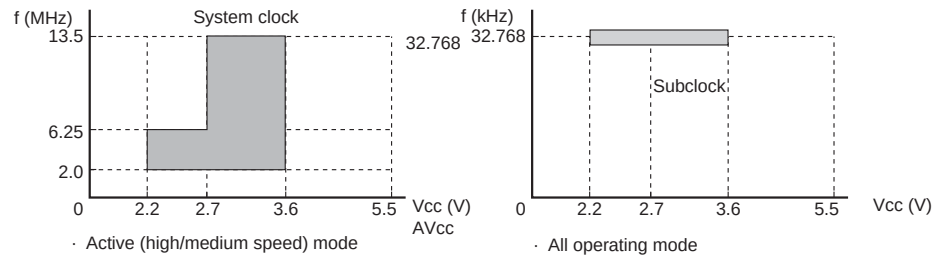
Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
MRA	SM1	SM0	DM1	DM0	MD1	MD0	DTS	Sz	DTC
SAR	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
MRB	CHNE	DISEL	—	—	—	—	—	—	
DAR	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
CRA	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
CRB	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
IECTR	IEE	IOL	DEE	CK	RE	LUEE	—	—	IEB
IECMR	—	—	—	—	—	CMD2	CMD1	CMD0	
IEMCR	SS	RN2	RN1	RN0	CTL3	CTL2	CTL1	CTL0	
IEAR1	IAR3	IAR2	IAR1	IAR0	IMD1	IMD0	—	STE	
IEAR2	IAR11	IAR10	IAR9	IAR8	IAR7	IAR6	IAR5	IAR4	
IESA1	ISA3	ISA2	ISA1	ISA0	—	—	—	—	
IESA2	ISA11	ISA10	ISA9	ISA8	ISA7	ISA6	ISA5	ISA4	
IETBFL	TBFL7	TBFL6	TBFL5	TBFL4	TBFL3	TBFL2	TBFL1	TBFL0	
IETBR	TBR7	TBR6	TBR5	TBR4	TBR3	TBR2	TBR1	TBR0	
IEMA1	IMA3	IMA2	IMA1	IMA0	—	—	—	—	
IEMA2	IMA11	IMA10	IMA9	IMA8	IMA7	IMA6	IMA5	IMA4	
IERCTL	—	—	—	—	RCTL3	RCTL2	RCTL1	RCTL0	
IERBFL	RBFL7	RBFL6	RBFL5	RBFL4	RBFL3	RBFL2	RBFL1	RBFL0	
IERBR	RBR7	RBR6	RBR5	RBR4	RBR3	RBR2	RBR1	RBR0	
IELA1	ILA7	ILA6	ILA5	ILA4	ILA3	ILA2	ILA1	ILA0	

(1) Power supply voltage/analog power supply voltage and oscilllation frequency range
(F-ZTAT-version wide-range specifications)



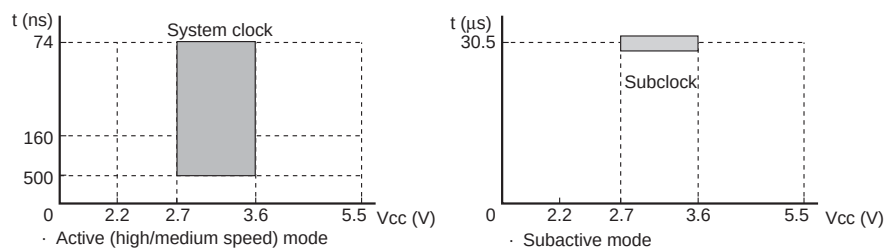
· Active (high/medium speed) mode
· Sleep mode
· All operating mode

(2) Power supply voltage/analog power supply voltage and oscilllation frequency range
(F-ZTAT-version regular specifications/Masked ROM version)



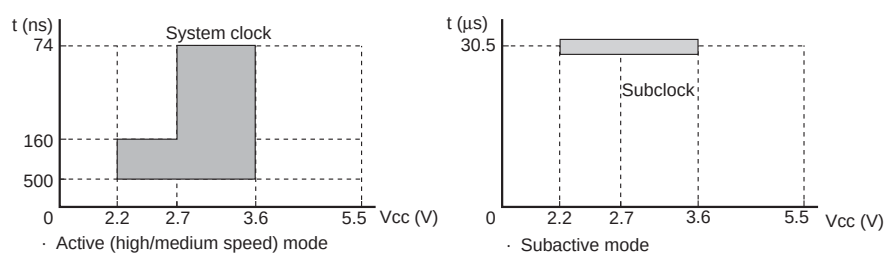
· Active (high/medium speed) mode
· Sleep mode
· All operating mode

(3) Power supply voltage and instruction executing range (F-ZTAT-version wide-range specifications)



· Active (high/medium speed) mode
· Subactive mode

(4) Power supply voltageand instruction executing range
(F-ZTAT-version regular specifications/Masked ROM version)



· Active (high/medium speed) mode
· Subactive mode

Note: The emulator does not operate at 2.2 V.

Figure 27.4 Power Supply Voltage and Operating Ranges (H8S/2238R and H8S/2236R)