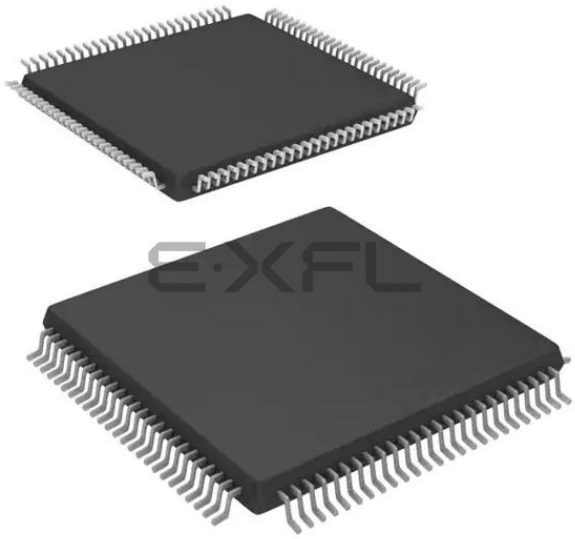

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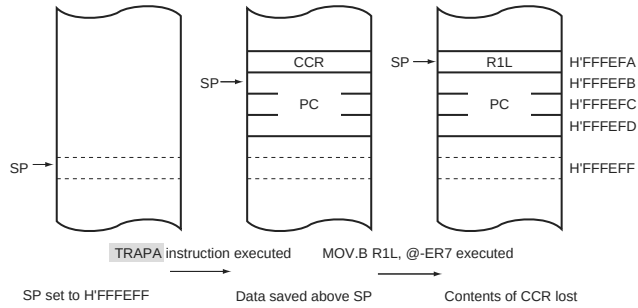
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	6MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2238rtf6v

Item	Page	Revision (See Manual for Details)
4.8 Usage Note Figure 4.3 Operation When SP Value Is Odd	126	Figure amended 
5.6.5 IRQ Interrupt	156	5.6.5 added
5.6.6 NMI Interrupts Usage Notes	156	5.6.6 added
6.3.4 Operation in Transitions to Power-Down Modes	161	Description amended • When the SLEEP instruction causes a transition from high speed mode to subactive mode (figure 6.2 (B)).
7.6.4 Wait Control (2) Pin Wait Insertion	191	Description amended Setting the WAITE bit in BCRL to 1 enables wait insertion by means of the $\overline{\text{WAIT}}$ pin.
9.2.5 DTC Transfer Count Register A (CRA)	285	Description amended In repeat mode or block transfer mode, the CRA is divided into two parts; the upper 8 bits (CRAH) and the lower 8 bits (CRAL). In repeat mode, CRAH holds the number of transfers while CRAL functions as an 8-bit transfer counter (1 to 256). In block transfer mode, CRAH holds the block size while CRAL function as an 8-bit block size counter (1 to 256). CRAL is decremented by 1 every time data is transferred, and the contents of CRAH are sent when the count reaches H'00. This operation is repeated.
10.1.2 Port 1 Data Register (P1DR)	310	Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	P17DR	0	R/W	Output data for a pin is stored when the pin is specified as a general purpose output port.
6	P16DR	0	R/W	
5	P15DR	0	R/W	
4	P14DR	0	R/W	
3	P13DR	0	R/W	
2	P12DR	0	R/W	
1	P11DR	0	R/W	
0	P10DR	0	R/W	

- On-chip memory

ROM	Model	ROM	RAM	Remarks
Flash memory version	HD64F2258	256 kbytes	16 kbytes	
	HD64F2239	384 kbytes	32 kbytes	
	HD64F2238B	256 kbytes	16 kbytes	
	HD64F2238R	256 kbytes	16 kbytes	
	HD64F2227	128 kbytes	16 kbytes	
PROM version	HD6472237	128 kbytes	16 kbytes	
Masked ROM version	HD6432258	256 kbytes	16 kbytes	
	HD6432258W	256 kbytes	16 kbytes	
	HD6432256	128 kbytes	8 kbytes	
	HD6432256W	128 kbytes	8 kbytes	
	HD6432239	384 kbytes	32 kbytes	
	HD6432239W	384 kbytes	32 kbytes	
	HD6432238B	256 kbytes	16 kbytes	
	HD6432238BW	256 kbytes	16 kbytes	
	HD6432238R	256 kbytes	16 kbytes	
	HD6432238RW	256 kbytes	16 kbytes	
	HD6432236B	128 kbytes	8 kbytes	
	HD6432236BW	128 kbytes	8 kbytes	
	HD6432236R	128 kbytes	8 kbytes	
	HD6432236RW	128 kbytes	8 kbytes	
	HD6432237	128 kbytes	16 kbytes	
	HD6432235	128 kbytes	4 kbytes	
	HD6432233	64 kbytes	4 kbytes	
	HD6432227	128 kbytes	16 kbytes	
	HD6432225	128 kbytes	4 kbytes	
	HD6432224	96 kbytes	4 kbytes	
	HD6432223	64 kbytes	4 kbytes	

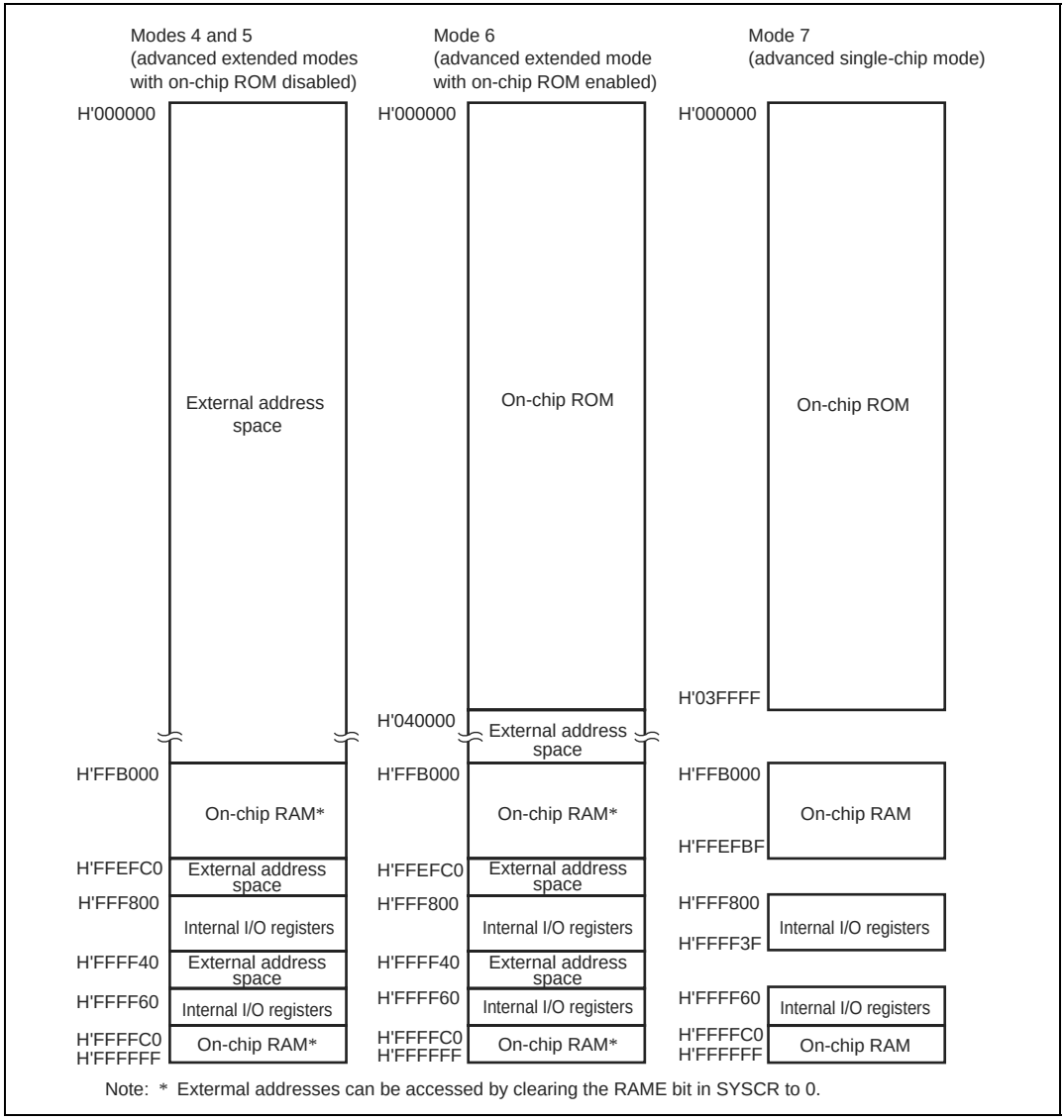
- General I/O ports
  - I/O pins: 72
  - Input-only pins: 10
- Supports various power-down states

Pin No.		Pin Name				
TFP-100B TFP-100BV TFP-100G TFP-100GV FP-100B FP-100BV	**TBP-112A*1 TBP-112AV*1**	**Mode 4**	**Mode 5**	**Mode 6**	**Mode 7**	**Flash Memory Programmable Mode*2**
27	L2	PB5/A13/ TIOCB4	PB5/A13/ TIOCB4	PB5/A13/ TIOCB4	PB5/TIOCB4	A13
28	H4	PB6/A14/ TIOCA5	PB6/A14/ TIOCA5	PB6/A14/ TIOCA5	PB6/TIOCA5	A14
29	K3	PB7/A15/ TIOCB5	PB7/A15/ TIOCB5	PB7/A15/ TIOCB5	PB7/TIOCB5	A15
30	L3	PA0/A16	PA0/A16	PA0/A16	PA0	A16
31	J4	PA1/A17/ TxD2	PA1/A17/ TxD2	PA1/A17/ TxD2	PA1/TxD2	A17
32	K4	PA2/A18/ RxD2	PA2/A18/ RxD2	PA2/A18/ RxD2	PA2/RxD2	A18
33	L4	PA3/A19/ SCK2	PA3/A19/ SCK2	PA3/A19/ SCK2	PA3/SCK2	NC
34	H5	P10/TIOCA0/ $\overline{\text{DACK0}}$/A20	P10/TIOCA0/ $\overline{\text{DACK0}}$/A20	P10/TIOCA0/ $\overline{\text{DACK0}}$/A20	P10/TIOCA0/ $\overline{\text{DACK0}}$	NC
35	J5	P11/TIOCB0/ $\overline{\text{DACK1}}$/A21	P11/TIOCB0/ $\overline{\text{DACK1}}$/A21	P11/TIOCB0/ $\overline{\text{DACK1}}$/A21	P11/TIOCB0/ $\overline{\text{DACK1}}$	NC
36	L5	P12/TIOCC0/ TCLKA/A22	P12/TIOCC0/ TCLKA/A22	P12/TIOCC0/ TCLKA/A22	P12/TIOCC0/ TCLKA	NC
37	K5	P13/TIOCD0/ TCLKB/A23	P13/TIOCD0/ TCLKB/A23	P13/TIOCD0/ TCLKB/A23	P13/TIOCD0/ TCLKB	NC
38	J6	P14/TIOCA1/ $\overline{\text{IRQ0}}$	P14/TIOCA1/ $\overline{\text{IRQ0}}$	P14/TIOCA1/ $\overline{\text{IRQ0}}$	P14/TIOCA1/ $\overline{\text{IRQ0}}$	VSS
39	L6	P15/TIOCB1/ TCLKC	P15/TIOCB1/ TCLKC	P15/TIOCB1/ TCLKC	P15/TIOCB1/ TCLKC	NC
40	K6	P16/TIOCA2/ $\overline{\text{IRQ1}}$	P16/TIOCA2/ $\overline{\text{IRQ1}}$	P16/TIOCA2/ $\overline{\text{IRQ1}}$	P16/TIOCA2/ $\overline{\text{IRQ1}}$	VSS
41	H6	P17/TIOCB2/ TCLKD	P17/TIOCB2/ TCLKD	P17/TIOCB2/ TCLKD	P17/TIOCB2/ TCLKD	NC
42	K7, L7	AVSS	AVSS	AVSS	AVSS	VSS
43	J7	P97/DA1	P97/DA1	P97/DA1	P97/DA1	NC
44	L8	P96/DA0	P96/DA0	P96/DA0	P96/DA0	NC
45	H7	P47/AN7	P47/AN7	P47/AN7	P47/AN7	NC
46	K8	P46/AN6	P46/AN6	P46/AN6	P46/AN6	NC
47	L9	P45/AN5	P45/AN5	P45/AN5	P45/AN5	NC

Table 2.3 Data Transfer Instructions

Instruction	Size*1	Function
MOV	B/W/L	(EAs) → Rd, Rs → (EAd) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register.
MOVFPE	B	Cannot be used in this LSI.
MOVTPE	B	Cannot be used in this LSI.
POP	W/L	@SP+ → Rn Pops a general register from the stack. POP.W Rn is identical to MOV.W @SP+, Rn. POP.L ERn is identical to MOV.L @SP+, ERn.
PUSH	W/L	Rn → @–SP Pushes a general register onto the stack. PUSH.W Rn is identical to MOV.W Rn, @–SP. PUSH.L ERn is identical to MOV.L ERn, @–SP.
LDM*2	L	@SP+ → Rn (register list) Pops two or more general registers from the stack.
STM*2	L	Rn (register list) → @–SP Pushes two or more general registers onto the stack.

Notes: 1. Refers to the operand size.
B: Byte
W: Word
L: Longword
2. Only register ER0 to ER6 should be used when using the STM/LDM instruction.



Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 3.4 H8S/2238B and H8S/2238R Memory Map in Each Operating Mode

7.7.2 Wait Control

As with the basic bus interface, either program wait insertion or pin wait insertion using the $\overline{\text{WAIT}}$ pin can be used in the initial cycle (full access) of the burst ROM interface. See section 7.6.4, Wait Control.

Wait states cannot be inserted in a burst cycle.

7.8 Idle Cycle

When this LSI accesses external space, it can insert a 1-state idle cycle (T_i) between bus cycles in the following two cases: (1) when read accesses between different areas occur consecutively, and (2) when a write cycle occurs immediately after a read cycle. By inserting an idle cycle it is possible, for example, to avoid data collisions between ROM, with a long output floating time, and high-speed memory, I/O interfaces, and so on.

(1) Consecutive Reads between Different Areas

If consecutive reads between different areas occur while the ICIS1 bit in BCRH is set to 1, an idle cycle is inserted at the start of the second read cycle.

Figure 7.21 shows an example of the operation in this case. In this example, bus cycle A is a read cycle from ROM with a long output floating time, and bus cycle B is a read cycle from SRAM, each being located in a different area. In (a), an idle cycle is not inserted, and a collision occurs in cycle B between the read data from ROM and that from SRAM. In (b), an idle cycle is inserted, and a data collision is prevented.

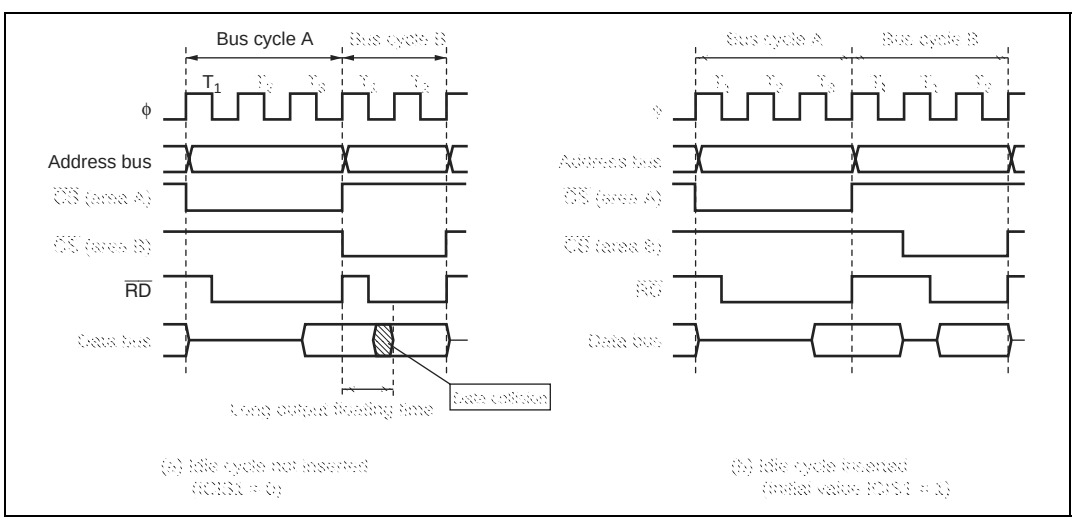


Figure 7.21 Example of Idle Cycle Operation (1)

Transfer Mode		Transfer Source	Remarks
Full address mode	Normal mode (1) Auto-request • Transfer request is internally held • Number of transfers (1 to 65,536) is continuously sent • Burst/cycle steal transfer can be selected	• Auto-request	• Max. 2-channel operation, combining channels A and B
	(2) External request • 1-byte or 1-word transfer for a single transfer request • Number of transfers: 1 to 65,536	• External request	
	Block transfer mode • Transfer of 1-block, size selected for a single transfer request • Number of transfers: 1 to 65,536 • Source or destination can be selected as block area • Block size: 1 to 256 bytes or word	• TPU channel 0 to 5 compare match/input capture A interrupt • SCI transmit-data-empty interrupt • SCI receive-data-full interrupt • A/D converter conversion end interrupt • External request	

Single Address Mode (Write): Figure 8.29 shows a transfer example in which $\overline{\text{TEND}}$ output is enabled and byte-size single address mode transfer (write) is performed from an external device to external 8-bit, 2-state access space.

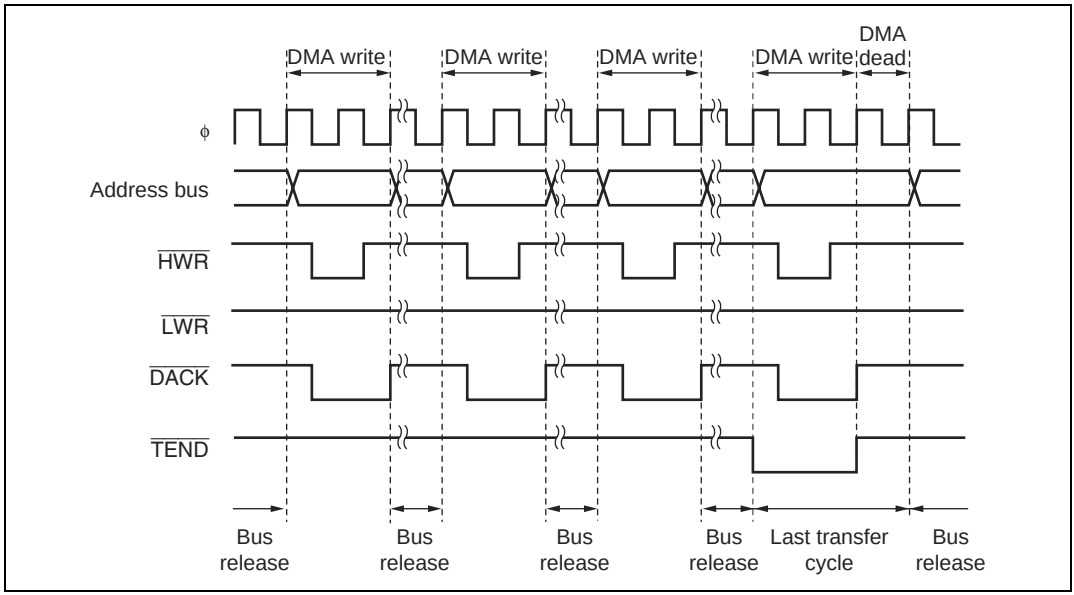
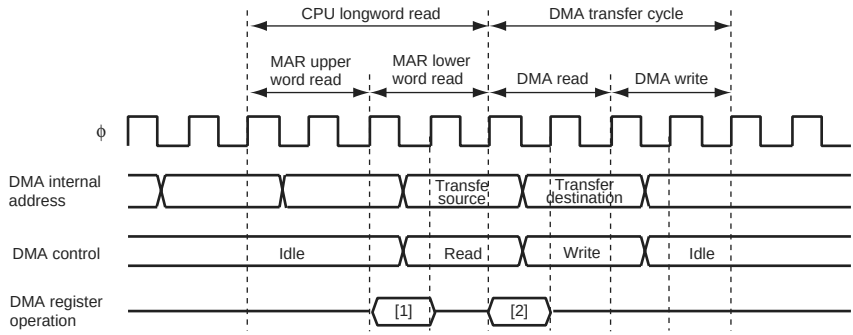


Figure 8.29 Example of Single Address Mode Transfer (Byte Write)

- If a DMAC transfer cycle occurs immediately after a DMAC register read cycle, the DMAC register is read as shown in figure 8.39.



Note: The lower word of MAR is the updated value after the operation in [1].

Figure 8.39 Contention between DMAC Register Update and CPU Read

8.7.2 Module Stop

When the MSTPA7 bit in MSTPCRA is set to 1, the DMAC clock stops, and the module stop state is entered. However, 1 cannot be written to the MSTPA7 bit if any of the DMAC channels is enabled. This setting should therefore be made when DMAC operation is stopped.

When the DMAC clock stops, DMAC register accesses can no longer be made. Since the following DMAC register settings are valid even in the module stop state, they should be invalidated, if necessary, before a module stop.

- Transfer end/break interrupt (DTE = 0 and DTIE = 1)
- $\overline{\text{TEND}}$ pin enable (TEE = 1)
- $\overline{\text{DACK}}$ pin enable (FAE = 0 and SAE = 1)

8.7.3 Medium-Speed Mode

When the DTA bit is cleared to 0, the internal interrupt signal that is specified for the DMAC transfer source is detected at the edge. In medium-speed mode, the DMAC operates by the medium-speed clock and the internal peripheral module operates by the high-speed clock. Therefore, when the corresponding interruption source is cleared by the CPU, DTC, or other channels of the DMAC and the period until the next interruption is executed is less than one state regarding to the DMAC clock (bus master clock), the signal is not detected at the edge and ignored.

- DTC enable registers A to G, and I (DTCERA to DTCERG, and DTCERI)
- DTC vector register (DTVECR)

9.2.1 DTC Mode Register A (MRA)

MRA selects the DTC operating mode.

Bit	Bit Name	Initial Value	R/W	Description
7	SM1	Undefined	—	Source Address Mode 1 and 0
6	SM0	Undefined	—	These bits specify an SAR operation after a data transfer. 0×: SAR is fixed 10: SAR is incremented after a transfer (by +1 when Sz = 0; by +2 when Sz = 1) 11: SAR is decremented after a transfer (by –1 when Sz = 0; by –2 when Sz = 1)
5	DM1	Undefined	—	Destination Address Mode 1 and 0
4	DM0	Undefined	—	These bits specify a DAR operation after a data transfer. 0×: DAR is fixed 10: DAR is incremented after a transfer (by +1 when Sz = 0; by +2 when Sz = 1) 11: DAR is decremented after a transfer (by –1 when Sz = 0; by –2 when Sz = 1)
3	MD1	Undefined	—	DTC Mode 1 and 0
2	MD0	Undefined	—	These bits specify the DTC transfer mode. 00: Normal mode 01: Repeat mode 10: Block transfer mode 11: Setting prohibited
1	DTS	Undefined	—	DTC Transfer Mode Select Specifies whether the source side or the destination side is set to be a repeat area or block area, in repeat mode or block transfer mode. 0: Destination side is repeat area or block area 1: Source side is repeat area or block area

9.3 Activation Sources

The DTC operates when activated by an interrupt or by a write to DTVECR by software. An interrupt request can be directed to the CPU or DTC, as designated by the corresponding DTCER bit. At the end of a data transfer (or the last consecutive transfer in the case of chain transfer), the activation source or corresponding DTCER bit is cleared. The activation source flag, in the case of RXI0, for example, is the RDRF flag of SCI_0. As there are a number of activation sources, the activation source flag is not cleared with the last byte (or word) transfer. Take appropriate measures at each interrupt as shown in table 9.1, Activation source and DTCER clearance.

Table 9.1 Activation Source and DTCER Clearance

Activation Source	When the DISEL Bit is 0 and the Specified Number of Transfers Have Not Ended	When the DISEL Bit is 1,or when the Specified Number of Transfers Have Ended
Software activation	• The SWDTE bit is cleared to 0	• The SWDTE bit remains set to 1 • An interrupt is issued to the CPU
Interrupt activation	• The corresponding DTCER bit remains set to 1 • The activation source flag is cleared to 0	• The corresponding DTCER bit is cleared to 0 • The activation source flag remains set to 1 • A request is issued to the CPU for the activation source interrupt

When an interrupt has been designated a DTC activation source, the existing CPU mask level and interrupt controller priorities have no effect. If there is more than one activation source at the same time, the DTC operates in accordance with the default priorities.

Figure 9.2 shows a block diagram of activation source control. For details, see section 5, Interrupt Controller.

Table 11.22 TIOR_1

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_1 Function**	**TIOCA1 Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCA1 pin Input capture at rising edge
			1		Capture input source is TIOCA1 pin Input capture at falling edge
		1	×		Capture input source is TIOCA1 pin Input capture at both edges
	1	×	×		Capture input source is TGRA_0 compare match/input capture Input capture at generation of channel 0/TGRA_0 compare match/input capture*

Legend: ×: Don't care

Note: * Not available in the H8S/2227 Group.

11.4.6 Phase Counting Mode

In phase counting mode, the phase difference between two external clock inputs is detected and TCNT is incremented/decremented accordingly. In the H8S/2227 Group, this mode can be set for channels 1 and 2. In other groups, it can be set for channels 1, 2, 4, and 5.

When phase counting mode is set, an external clock is selected as the counter input clock and TCNT operates as an up/down-counter regardless of the setting of bits TPSC2 to TPSC0 and bits CKEG1 and CKEG0 in TCR. However, the functions of bits CCLR1 and CCLR0 in TCR, and of TIOR, TIER, and TGR are valid, and input capture/compare match and interrupt functions can be used.

This can be used for two-phase encoder pulse input.

When overflow occurs while TCNT is counting up, the TCFV flag in TSR is set; when underflow occurs while TCNT is counting down, the TCFU flag is set.

The TCFD bit in TSR is the count direction flag. Reading the TCFD flag provides an indication of whether TCNT is counting up or down.

Table 11.31 shows the correspondence between external clock pins and channels.

Table 11.31 Clock Input Pins in Phase Counting Mode

	External Clock Pins	
Channels	**A-Phase**	**B-Phase**
When channel 1 or 5* is set to phase counting mode	TCLKA	TCLKB
When channel 2 or 4* is set to phase counting mode	TCLKC	TCLKD

Note: * Not available in the H8S/2227 Group.

11.5 Interrupt Sources

There are three kinds of TPU interrupt source: TGR input capture/compare match, TCNT overflow, and TCNT underflow. Each interrupt source has its own status flag and enable/disable bit, allowing generation of interrupt request signals to be enabled or disabled individually.

When an interrupt request is generated, the corresponding status flag in TSR is set to 1. If the corresponding enable/disable bit in TIER is set to 1 at this time, an interrupt is requested. The interrupt request is cleared by clearing the status flag to 0.

Relative channel priorities can be changed by the interrupt controller, but the priority order within a channel is fixed. For details, see section 5, Interrupt Controller.

Table 11.36 lists the TPU interrupt sources.

(c) Setting the IEBus Slave Address Setting Registers 1 and 2 (IESA1 and IESA2)

Specify the communications destination slave unit address.

(d) Setting the IEBus Master Control Register (IEMCR)

Select broadcast/normal communications, specify the number of retransfer counts at arbitration loss, and specify the control bits.

(e) Setting the IEBus Receive Interrupt Enable Register (IEIER)

Enable the RxRDY (IERxI), RxS, RxF, and RxE (IERSI) interrupts.

The above registers can be specified in any order. (The register specification order does not affect the IEB operation.)

(2) DTC Initialization

1. Set the start address of the RAM which stores the register information necessary for the DTC transfer in the vector address (H'000004D2) to be accessed when a DTC transfer request is generated.
2. Set the following data from the start address of the RAM.
   - Transfer source address (SAR): Address (H'FFF80D) of the IEBus receive buffer register (IERBR).
   - Transfer destination address (DAR): Start address of the RAM which stores data to be received from the data field.
   - Transfer count (CRA): Maximum number of transfer bytes in one frame in the transfer mode.
3. Set bit DTCEG6 in the DTC enabler register G (DTCERG), and enable the RxRDY interrupt (IERxI).

Because the above settings are performed before frame reception, the length of data to be received cannot be determined. Accordingly, the maximum number of transfer bytes in one frame is specified as the DTC transfer count.

If the DTC is specified after reception starts, the above settings are performed in the receive start detection (RxS) interrupt handling routine. In this case, the transfer count must be the same value as the contents of the IEBus receive message length register (IERBFL).

17.7 A/D Conversion Accuracy Definitions

This LSI's A/D conversion accuracy definitions are given below.

- Resolution

  The number of A/D converter digital output codes.
- Quantization error

  The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 17.7).
- Offset error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value B'0000000000 (H'000) to B'0000000001 (H'001) (see figure 17.8).
- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from B'1111111110 (H'3FE) to B'1111111111 (H'3FF) (see figure 17.8).
- Nonlinearity error

  The error with respect to the ideal A/D conversion characteristic between zero voltage and full-scale voltage. Does not include offset error, full-scale error, or quantization error (see figure 17.8).
- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes offset error, full-scale error, quantization error, and nonlinearity error.

Section 21 Masked ROM

This LSI incorporates a masked ROM which has the following features.

21.1 Features

- Size

Product Class		ROM Size	ROM Address (Modes 6 and 7)
H8S/2258 Group	HD6432258	256 kbytes	H'000000 to H'03FFFF
	HD6432256	128 kbytes	H'000000 to H'01FFFF
	HD6432258W	256 kbytes	H'000000 to H'03FFFF
	HD6432256W	128 kbytes	H'000000 to H'01FFFF
H8S/2239 Group	HD6432239	384 kbytes	H'000000 to H'05FFFF
	HD6432239W	384 kbytes	H'000000 to H'05FFFF
H8S/2238 Group	HD6432238B	256 kbytes	H'000000 to H'03FFFF
	HD6432236B	128 kbytes	H'000000 to H'01FFFF
	HD6432238R	256 kbytes	H'000000 to H'03FFFF
	HD6432236R	128 kbytes	H'000000 to H'01FFFF
	HD6432238BW	256 kbytes	H'000000 to H'03FFFF
	HD6432236BW	128 kbytes	H'000000 to H'01FFFF
	HD6432238RW	256 kbytes	H'000000 to H'03FFFF
	HD6432236RW	128 kbytes	H'000000 to H'03FFFF
H8S/2237 Group	HD6432237	128 kbytes	H'000000 to H'01FFFF
	HD6432235	128 kbytes	H'000000 to H'01FFFF
	HD6432233	64 kbytes	H'000000 to H'00FFFF
H8S/2227 Group	HD6432227	128 kbytes	H'000000 to H'01FFFF
	HD6432225	128 kbytes	H'000000 to H'01FFFF
	HD6432224	96 kbytes	H'000000 to H'017FFF
	HD6432223	64 kbytes	H'000000 to H'00FFFF

- Connected to the bus master through 16-bit data bus, enabling one-state access to both byte data and word data.

Figure 21.1 shows a block diagram of the on-chip masked ROM.

(1) Clock Timing

Table 27.17 lists the clock timing.

Table 27.17 Clock Timing

Condition A (F-ZTAT version and masked ROM version):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32.768 kHz, 2 to 16.0 MHz, T_a = –20°C to +75°C (regular specifications)

Condition B (Masked ROM version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V, V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32.768 kHz, 2 to 6.25 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C (F-ZTAT version and masked ROM version):
V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32.768 kHz, 10.0 to 20.0 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A			Condition B			Condition C				
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Clock cycle time	t_{cyc}	62.5	—	500	160	—	500	50	—	100	ns	Figure 27.10
Clock high pulse width	t_{CH}	20	—	—	50	—	—	17	—	—	ns	
Clock low pulse width	t_{CL}	20	—	—	50	—	—	17	—	—	ns	
Clock rise time	t_{Cr}	—	—	10	—	—	25	—	—	10	ns	
Clock fall time	t_{Cf}	—	—	10	—	—	25	—	—	10	ns	
Oscillation stabilization time at reset (crystal)	t_{OSC1}	20	—	—	40	—	—	20	—	—	ms	Figure 27.11

Table 27.51 DC Characteristics (3)

Conditions (ZTAT version): V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V,
V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)*1

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	$\overline{RES}$	C_{in}	—	—	80	pF	V_{in} = 0 V
	NMI		—	—	50	pF	f = 1 MHz
	All input pins other than above ones		—	—	15	pF	T_a = 25 °C
Current consumption*2	Normal operation	I_{CC}*4	—	16 V_{CC} = 3.0 V	28 V_{CC} = 3.6 V	mA	f = 10 MHz
	Sleep mode		—	12 V_{CC} = 3.0 V	22 V_{CC} = 3.6 V	mA	f = 10 MHz
	All modules stopped		—	12	—	mA	f = 10 MHz, V_{CC} = 3.0 V (reference value)
	Medium-speed mode (ϕ/32)		—	8.5	—	mA	f = 10 MHz, V_{CC} = 3.0 V (reference value)
	Subactive mode		—	80	120	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used
	Subsleep mode		—	60	90	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used
	Watch mode		—	8	12	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used

Product Type			Product Code	Mark Code	Package (Package Code)
H8S/2236B	Masked ROM version	5-V version	HD6432236B	HD6432236B(***)TE	100-pin TQFP (TFP-100B)
				HD6432236B(***)TF	100-pin TQFP (TFP-100G)
				HD6432236B(***)F	100-pin QFP (FP-100A)
				HD6432236B(***)FA	100-pin QFP (FP-100B)
		On-chip I^2C bus interface product (5-V version)	HD6432236BW	HD6432236BW(***)TE	100-pin TQFP (TFP-100B)
				HD6432236BW(***)TF	100-pin TQFP (TFP-100G)
				HD6432236BW(***)F	100-pin QFP (FP-100A)
				HD6432236BW(***)FA	100-pin QFP (FP-100B)
H8S/2236R	Masked ROM version	3-V version, 2.2-V version	HD6432236R	HD6432236R(***)TE	100-pin TQFP (TFP-100B)
				HD6432236R(***)TF	100-pin TQFP (TFP-100G)
				HD6432236R(***)FA	100-pin QFP (FP-100B)
		On-chip I^2C bus interface product (3-V version)	HD6432236RW	HD6432236RW(***)TE	100-pin TQFP (TFP-100B)
				HD6432236RW(***)TF	100-pin TQFP (TFP-100G)
				HD6432236RW(***)FA	100-pin QFP (FP-100B)

Legend:

(***): ROM code

Note: Please contact Renesas Technology agency to confirm the current status of each product.