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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | H8S/2000 |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | I²C, SCI, SmartCard |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 72 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BFQFP |
| Supplier Device Package | 100-QFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df2239fa16v |

User's Manual

16

The revision list can be viewed directly by clicking the title page. The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

# H8S/2258, H8S/2239, H8S/2238, H8S/2237, H8S/2227 Groups

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer

H8S Family/H8S/2200 Series

| | | | |
|---|---|---|---|
| H8S/2258 | HD64F2258 | H8S/2236R | HD6432236R |
| | HD6432258 | | HD6432236RW |
| | HD6432258W | H8S/223 | HD6472237 |
| H8S/2256 | HD6432256 | | HD6432237 |
| | HD6432256W | H8S/2235 | HD6432235 |
| H8S/2239 | HD64F2239 | H8S/2233 | HD6432233 |
| | HD6432239 | H8S/2227 | HD64F2227 |
| | HD6432239W | | HD6432227 |
| H8S/2238 | HD64F2238B | H8S/2225 | HD6432225 |
| | HD6432238B | H8S/2224 | HD6432224 |
| | HD6432238BW | H8S/2223 | HD6432223 |
| H8S/2238R | HD64F2238R | | |
| | HD6432238R | | |
| | HD6432238RW | | |
| H8S/2236B | HD6432236B | | |
| | HD6432236BW | | |

Renesas Electronics
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Rev.6.00 2010.03

- On-chip memory

| ROM | Model | ROM | RAM | Remarks |
|---|---|---|---|---|
| Flash memory version | HD64F2258 | 256 kbytes | 16 kbytes | |
| | HD64F2239 | 384 kbytes | 32 kbytes | |
| | HD64F2238B | 256 kbytes | 16 kbytes | |
| | HD64F2238R | 256 kbytes | 16 kbytes | |
| | HD64F2227 | 128 kbytes | 16 kbytes | |
| PROM version | HD6472237 | 128 kbytes | 16 kbytes | |
| Masked ROM version | HD6432258 | 256 kbytes | 16 kbytes | |
| | HD6432258W | 256 kbytes | 16 kbytes | |
| | HD6432256 | 128 kbytes | 8 kbytes | |
| | HD6432256W | 128 kbytes | 8 kbytes | |
| | HD6432239 | 384 kbytes | 32 kbytes | |
| | HD6432239W | 384 kbytes | 32 kbytes | |
| | HD6432238B | 256 kbytes | 16 kbytes | |
| | HD6432238BW | 256 kbytes | 16 kbytes | |
| | HD6432238R | 256 kbytes | 16 kbytes | |
| | HD6432238RW | 256 kbytes | 16 kbytes | |
| | HD6432236B | 128 kbytes | 8 kbytes | |
| | HD6432236BW | 128 kbytes | 8 kbytes | |
| | HD6432236R | 128 kbytes | 8 kbytes | |
| | HD6432236RW | 128 kbytes | 8 kbytes | |
| | HD6432237 | 128 kbytes | 16 kbytes | |
| | HD6432235 | 128 kbytes | 4 kbytes | |
| | HD6432233 | 64 kbytes | 4 kbytes | |
| | HD6432227 | 128 kbytes | 16 kbytes | |
| | HD6432225 | 128 kbytes | 4 kbytes | |
| | HD6432224 | 96 kbytes | 4 kbytes | |
| | HD6432223 | 64 kbytes | 4 kbytes | |

- General I/O ports
  - I/O pins: 72
  - Input-only pins: 10
- Supports various power-down states

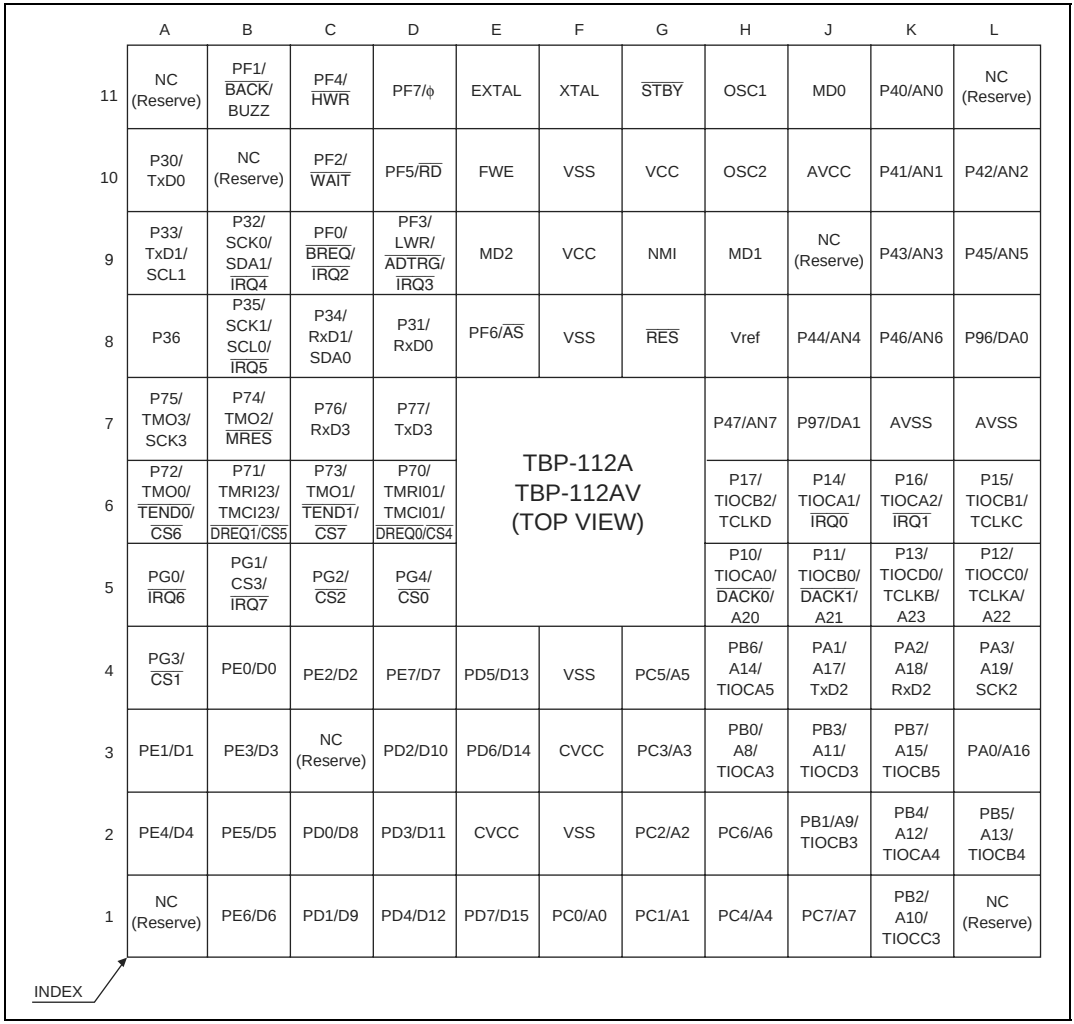



**Figure 1.9 Pin Arrangement of H8S/2239 Group**
**(TBP-112A, TBP-112AV: Top View, Only for HD64F2239)**

**Table 1.3 Pin Arrangements in Each Mode of H8S/2238 Group**

| Pin No. | | | Pin Name | | | | |
|---|---|---|---|---|---|---|---|
| TFP-100B<br>TFP-100BV<br>TFP-100G<br>TFP-100GV<br>FP-100B<br>FP-100BV | FP-100A[*1]<br>FP-100AV[*1] | BP-112[*2]<br>BP-112V[*2]<br>TBP-112A[*2]<br>TBP-112AV[*2] | Mode 4 | Mode 5 | Mode 6 | Mode 7 | Flash Memory Programmable Mode[*4] |
| 1 | 4 | B2 | PE5/D5 | PE5/D5 | PE5/D5 | PE5 | $\overline{OE}$ |
| 2 | 5 | B1 | PE6/D6 | PE6/D6 | PE6/D6 | PE6 | $\overline{WE}$ |
| 3 | 6 | D4 | PE7/D7 | PE7/D7 | PE7/D7 | PE7 | $\overline{CE}$ |
| 4 | 7 | C2 | D8 | D8 | D8 | PD0 | D0 |
| 5 | 8 | C1 | D9 | D9 | D9 | PD1 | D1 |
| 6 | 9 | D3 | D10 | D10 | D10 | PD2 | D2 |
| 7 | 10 | D2 | D11 | D11 | D11 | PD3 | D3 |
| 8 | 11 | D1 | D12 | D12 | D12 | PD4 | D4 |
| 9 | 12 | E4 | D13 | D13 | D13 | PD5 | D5 |
| 10 | 13 | E3 | D14 | D14 | D14 | PD6 | D6 |
| 11 | 14 | E1 | D15 | D15 | D15 | PD7 | D7 |
| 12 | 15 | E2, F3 | CVCC | CVCC | CVCC | CVCC | VCC |
| 13 | 16 | F1 | A0 | A0 | PC0/A0 | PC0 | A0 |
| 14 | 17 | F2, F4 | VSS | VSS | VSS | VSS | VSS |
| 15 | 18 | G1 | A1 | A1 | PC1/A1 | PC1 | A1 |
| 16 | 19 | G2 | A2 | A2 | PC2/A2 | PC2 | A2 |
| 17 | 20 | G3 | A3 | A3 | PC3/A3 | PC3 | A3 |
| 18 | 21 | H1 | A4 | A4 | PC4/A4 | PC4 | A4 |
| 19 | 22 | G4 | A5 | A5 | PC5/A5 | PC5 | A5 |
| 20 | 23 | H2 | A6 | A6 | PC6/A6 | PC6 | A6 |
| 21 | 24 | J1 | A7 | A7 | PC7/A7 | PC7 | A7 |
| 22 | 25 | H3 | PB0/A8/<br>TIOCA3 | PB0/A8/<br>TIOCA3 | PB0/A8/<br>TIOCA3 | PB0/<br>TIOCA3 | A8 |
| 23 | 26 | J2 | PB1/A9/<br>TIOCB3 | PB1/A9/<br>TIOCB3 | PB1/A9/<br>TIOCB3 | PB1/<br>TIOCB3 | A9 |
| 24 | 27 | K1 | PB2/A10/<br>TIOCC3 | PB2/A10/<br>TIOCC3 | PB2/A10/<br>TIOCC3 | PB2/<br>TIOCC3 | A10 |
| 25 | 28 | J3 | PB3/A11/<br>TIOCD3 | PB3/A11/<br>TIOCD3 | PB3/A11/<br>TIOCD3 | PB3/<br>TIOCD3 | A11 |
| 26 | 29 | K2 | PB4/A12/<br>TIOCA4 | PB4/A12/<br>TIOCA4 | PB4/A12/<br>TIOCA4 | PB4/<br>TIOCA4 | A12 |

| | | Pin No. | | | | |
|---|---|---|---|---|---|---|
| | | TFP-100B<br>TFP-100BV<br>TFP-100G<br>TFP-100GV<br>FP-100B | | BP-112*1<br>BP-112V*1<br>TBP-112A*4 | | |
| Type | Symbol | FP-100BV | FP-100A*3<br>FP-100AV*3 | TBP-112AV*4 | I/O | Function |
| DMA controller (DMAC)*2 | $\overline{\text{DREQ1}}$ | 89 | — | B6 | Input | Request DMAC activation. (Supported only by the H8S/2239 Group.) |
| | $\overline{\text{DREQ0}}$ | 90 | | D6 | | |
| | $\overline{\text{TEND1}}$ | 87 | — | C6 | Output | Indicate that the DMAC has ended transmitting data. (Supported only by the H8S/2239 Group.) |
| | $\overline{\text{TEND0}}$ | 88 | | A6 | | |
| | $\overline{\text{DACK1}}$ | 35 | — | J5 | Output | These pins function as single address transmitting acknowledge of DMAC. (Supported only by the H8S/2239 Group.) |
| | $\overline{\text{DACK0}}$ | 34 | | H5 | | |
| 16-bit timer-pulse unit (TPU) | TCLKD | 41 | 44 | H6 | Input | These pins input an external clock. |
| | TCLKC | 39 | 42 | L6 | | |
| | TCLKB | 37 | 40 | K5 | | |
| | TCLKA | 36 | 39 | L5 | | |
| | TIOCA0 | 34 | 37 | H5 | Input/ Output | Pins for the TGRA_0 to TGRD_0 input capture input, output compare output, or PWM output. |
| | TIOCB0 | 35 | 38 | J5 | | |
| | TIOCC0 | 36 | 39 | L5 | | |
| | TIOCD0 | 37 | 40 | K5 | | |
| | TIOCA1 | 38 | 41 | J6 | Input/ Output | Pins for the TGRA_1 and TGRB_1 input capture input, output compare output, or PWM output. |
| | TIOCB1 | 39 | 42 | L6 | | |
| | TIOCA2 | 40 | 43 | K6 | Input/ Output | Pins for the TGRA_2 and TGRB_2 input capture input, output compare output, or PWM output. |
| | TIOCB2 | 41 | 44 | H6 | | |
| | TIOCA3 | 22 | 25 | H3 | Input/ Output | Pins for the TGRA_3 to TGRD_3 input capture input, output compare output, or PWM output. |
| | TIOCB3 | 23 | 26 | J2 | | |
| | TIOCC3 | 24 | 27 | K1 | | |
| | TIOCD3 | 25 | 28 | J3 | | |
| | TIOCA4 | 26 | 29 | K2 | Input/ Output | Pins for the TGRA_4 and TGRB_4 input capture input, output compare output, or PWM output. |
| | TIOCB4 | 27 | 30 | L2 | | |
| | TIOCA5 | 28 | 31 | H4 | Input/ Output | Pins for the TGRA_5 and TGRB_5 input capture input, output compare output, or PWM output. |
| | TIOCB5 | 29 | 32 | K3 | | |

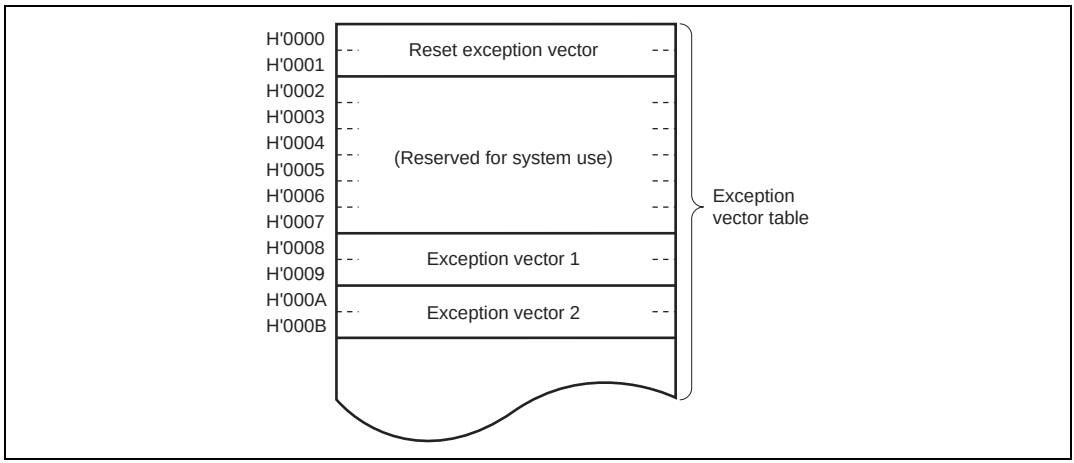



**Figure 2.1 Exception Vector Table (Normal Mode)**

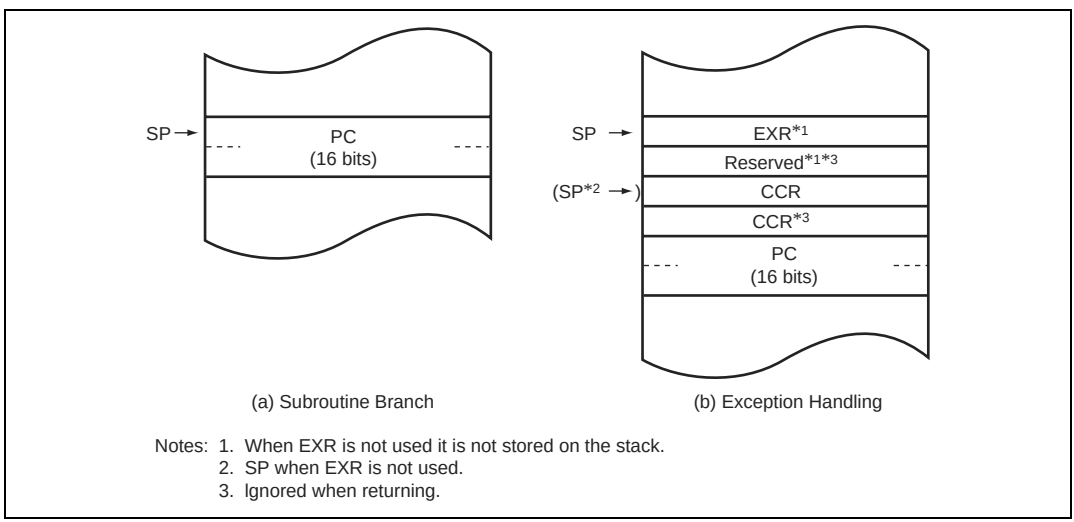



**Figure 2.2 Stack Structure in Normal Mode**

### 2.2.2 Advanced Mode

- Address Space

  Linear access is provided to a maximum 16-Mbyte address space.
- Extended Registers (En)

  The extended registers (E0 to E7) can be used as 16-bit registers, or as the upper 16-bit segments of 32-bit registers or address registers.

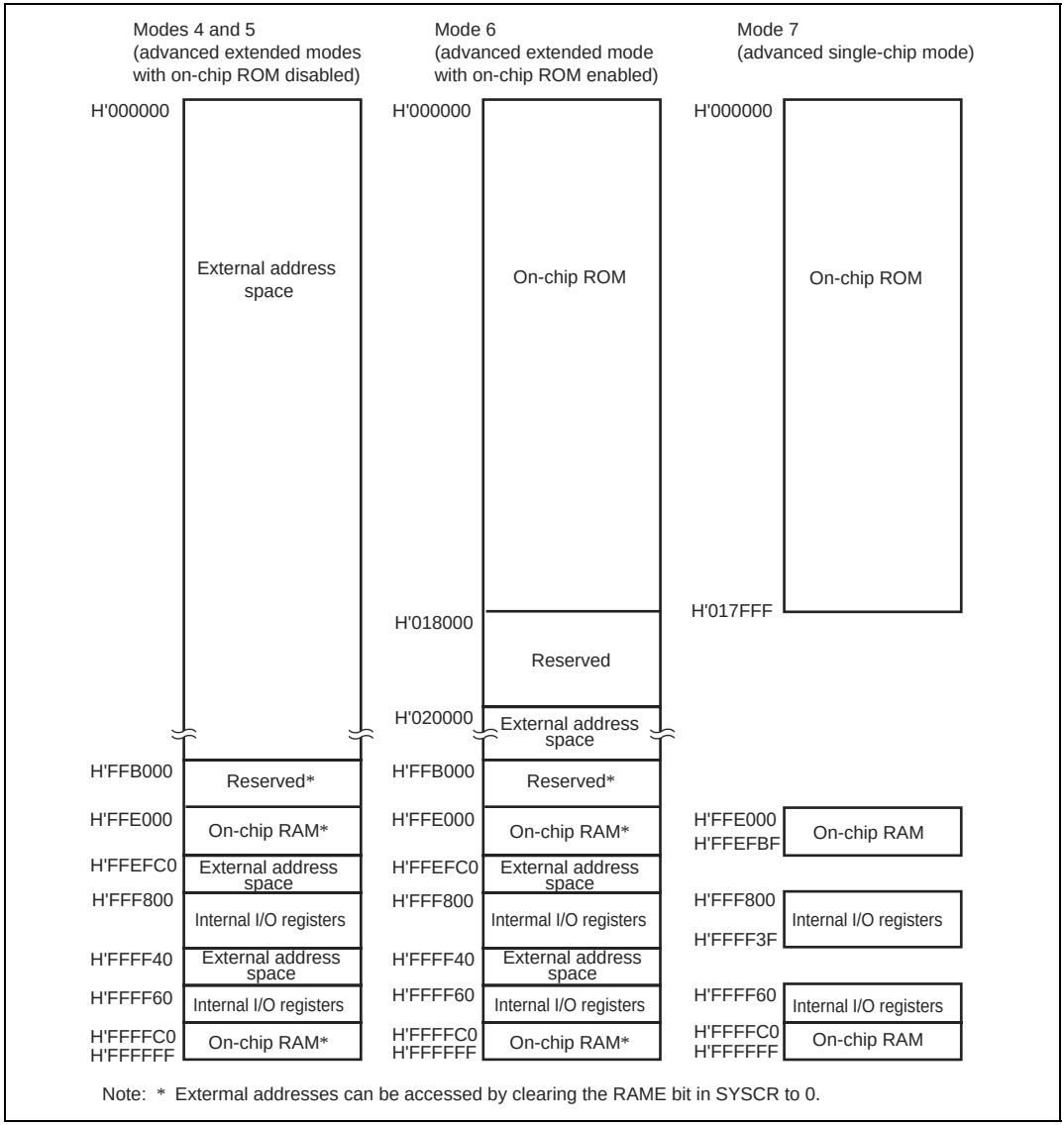



**Figure 3.8 H8S/2224 Memory Map in Each Operating Mode**

IOAR can be used in short address mode but not in full address mode.

### 8.3.3 Execute Transfer Count Registers (ETCRA and ETCRB)

ETCR is a 16-bit readable/writable register that specifies the number of transfers.

The DMA has four ETCR registers: ETCR_0A in channel 0 (channel 0A), ETCR_0B in channel 0 (channel 0B), ETCR_1A in channel 1 (channel 1A), and ETCR_1B in channel 1 (channel 1B).

ETCR is not initialized by a reset or in standby mode.

**Short Address Mode:** The function of ETCR in sequential mode and idle mode differs from that in repeat mode.

In sequential mode and idle mode, ETCR functions as a 16-bit transfer counter. ETCR is decremented by 1 each time a transfer is performed, and when the count reaches H'00, the DTE bit in DMABCRL is cleared, and transfer ends.

In repeat mode, ETCRL functions as an 8-bit transfer counter and ETCRH functions as a transfer count holding register. ETCRL is decremented by 1 each time a transfer is performed, and when the count reaches H'00, ETCRL is loaded with the value in ETCRH. At this point, MAR is automatically restored to the value it had when the count was started. The DTE bit in DMABCRL is not cleared, and so transfers can be performed repeatedly until the DTE bit is cleared by the user.

**Full Address Mode:** The function of ETCR in normal mode differs from that in block transfer mode.

In normal mode, ETCRA functions as a 16-bit transfer counter. ETCRA is decremented by 1 each time a data transfer is performed, and transfer ends when the count reaches H'0000. ETCRB is not used in normal mode.

In block transfer mode, ETCRAL functions as an 8-bit block size counter and ETCRAH functions as a block size holding register. ETCRAL is decremented by 1 each time a 1-byte or 1-word transfer is performed, and when the count reaches H'00, ETCRAL is loaded with the value in ETCRAH. So by setting the block size in ETCRAH and ETCRAL, it is possible to repeatedly transfer blocks consisting of any desired number of bytes or words.

In block transfer mode, ETCRB functions as a 16-bit block transfer counter. ETCRB is decremented by 1 each time a block is transferred, and transfer ends when the count reaches H'0000.

- P15/TIOCB1/TCLKC

  The pin functions are switched as shown below according to the combination of the TPU channel 1 setting, TPSC2 to TPS0 bits in TCR_0, TCR_2, TCR_4, and TCR_5 and the P15DDR bit.

| TPU Channel 1 Setting*1 | Output | Input or Initial Value | |
|---|---|---|---|
| P15DDR | — | 0 | 1 |
| Pin functions | TIOCB1 output pin | P15 input pin | P15 output pin |
| | | TIOCB1 input pin*2 | |
| | TCLKC input pin*3 | | |

Notes: 1. For the setting of the TPU channel, see section 11, 16-Bit Timer Pulse Unit (TPU).
2. This pin functions as TIOCB1 input when TPU channel 1 timer operating mode is set to normal operating or phase counting mode and IOB3 to IOB0 in TIOR_1 are set to10xx.
3. This pin functions as TCLKC input when TPSC2 to TPSC0 in TCR_0 or TCR_2 are set to 110 or TPSC2 to TPSC0 in TCR_4 or TCR_0 are 101 or when channels 2 and 4 are set to phase counting mode.

- P14/TIOCA1/$\overline{\text{IRQ0}}$

  The pin functions are switched as shown below according to the combination of the TPU channel 1 setting and the P14DDR bit.

| TPU Channel 1 Setting*1 | Output | Input or Initial Value | |
|---|---|---|---|
| P14DDR | — | 0 | 1 |
| Pin functions | TIOCA1 output pin | P14 input pin | P14 output pin |
| | | TIOCA1 input pin*2 | |
| | $\overline{\text{IRQ0}}$ input pin*3 | | |

Notes: 1. For the setting of the TPU channel, see section 11, 16-Bit Timer Pulse Unit (TPU).
2. This pin functions as TIOCA1 input when TPU channel 1 timer operating mode is set to normal operating or phase counting mode and IOA3 to IOA0 in TIOR_1 are set to 10xx.
3. When this pin is used as an external interrupt pin, do not specify other functions.

### 10.9.6 Input Pull-Up MOS States in Port D

Port D has a built-in input pull-up MOS function that can be controlled by software. Input pull-up MOS can be used in mode 7 and specified as on or off on an individual bit basis.

Table 10.5 summarizes the input pull-up MOS states in port D.

**Table 10.5 Input Pull-Up MOS States in Port D**

| Pin States | Power-on Reset | Hardware Standby Mode | Manual Reset | Software Standby Mode | In Other Operations |
|---|---|---|---|---|---|
| Data I/O (modes 4 to 6) and port output (mode 7) | OFF | OFF | OFF | OFF | OFF |
| Port input (mode 7) | | | ON/OFF | ON/OFF | ON/OFF |

Legend:
OFF: Input pull-up MOS is always off.
ON/OFF: On when PDDDR = 0 and PDPCR = 1; otherwise off.

## 10.10 Port E

Port E is an 8-bit I/O port and has the following registers.

- Port E data direction register (PEDDR)
- Port E data register (PEDR)
- Port E register (PORTE)
- Port E pull-up MOS control register (PEPCR)

**Example of Phase Counting Mode Setting Procedure:** Figure 11.25 shows an example of the phase counting mode setting procedure.

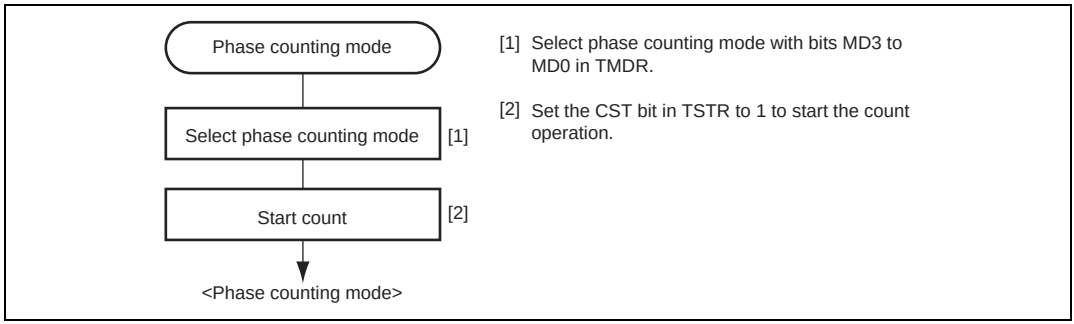



**Figure 11.25 Example of Phase Counting Mode Setting Procedure**

**Examples of Phase Counting Mode Operation:** In phase counting mode, TCNT counts up or down according to the phase difference between two external clocks. There are four modes, according to the count conditions.

1. Phase counting mode 1

   Figure 11.26 shows an example of phase counting mode 1 operation, and table 11.32 summarizes the TCNT up/down-count conditions.

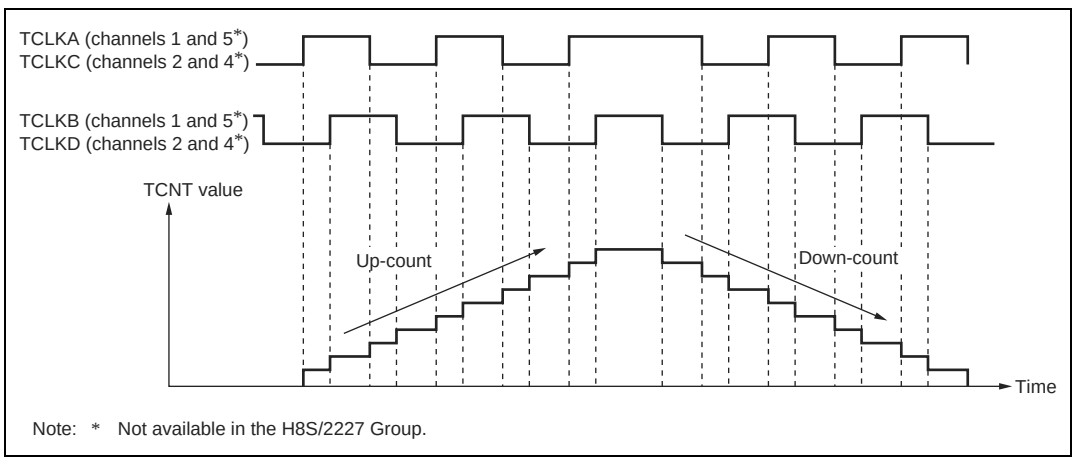



**Figure 11.26 Example of Phase Counting Mode 1 Operation**

# Section 12 8-Bit Timers

The H8S/2258 Group, H8S/2239 Group, and H8S/2238 Group have an on-chip 8-bit timer module with four channels (TMR_0, TMR_1, TMR_2, and TMR_3) operating on the basis of an 8-bit counter.

The H8S/2237 Group and H8S/2227 Group have an on-chip 8-bit timer module with two channels (TMR_0 and TMR_1) operating on the basis of an 8-bit counter.

The 8-bit timer module can be used to count external events and be used as a multifunction timer in a variety of applications, such as generation of counter reset, interrupt requests, and pulse output with an arbitrary duty cycle using a compare-match signal with two registers.

## 12.1 Features

- Selection of clock sources

  Selected from three internal clocks (φ/8, φ/64, and φ/8192) and an external clock.
- Selection of three ways to clear the counters

  The counters can be cleared on compare-match A or B, or by an external reset signal.
- Timer output controlled by two compare-match signals

  The timer output signal in each channel is controlled by two independent compare-match signals, enabling the timer to be used for various applications, such as the generation of pulse output or PWM output with an arbitrary duty cycle.
- Cascading of the two channels
  - TMR_0 and TMR_1 cascading

    The module can operate as a 16-bit timer using TMR_0 as the upper half and channel TMR_1 as the lower half (16-bit count mode).

    TMR_1 can be used to count TMR_0 compare-match occurrences (compare-match count mode).
  - TMR_2* and TMR_3* cascading

    The module can operate as a 16-bit timer using TMR_2 as the upper half and channel TMR_3 as the lower half (16-bit count mode).

    TMR_3 can be used to count TMR_2 compare-match occurrences (compare-match count mode).
- Multiple interrupt sources for each channel

  Two compare-match interrupts and one overflow interrupt can be requested independently.
- Generation of A/D conversion start trigger

  Channel 0 compare-match signal can be used as the A/D conversion start trigger.

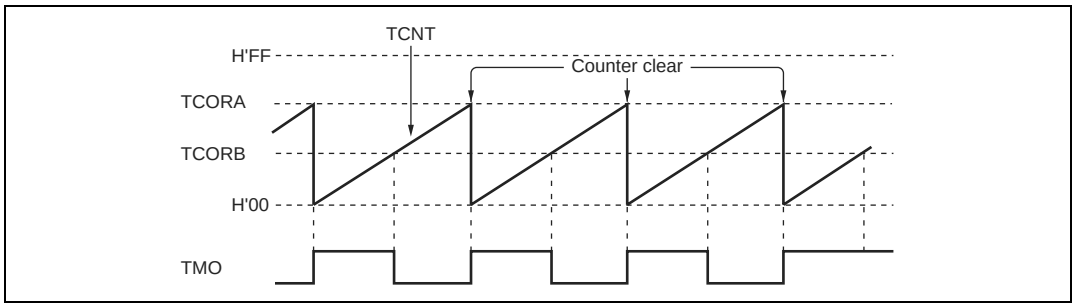



**Figure 12.2 Example of Pulse Output**

## 12.5 Operation Timing

### 12.5.1 TCNT Incrementation Timing

Figure 12.3 shows the TCNT count timing with internal clock source. Figure 12.4 shows the TCNT incrementation timing with external clock source. The pulse width of the external clock for incrementation at signal edge must be at least 1.5 system clock (ϕ) periods, and at least 2.5 states for incrementation at both edges. The counter will not increment correctly if the pulse width is less than these values.

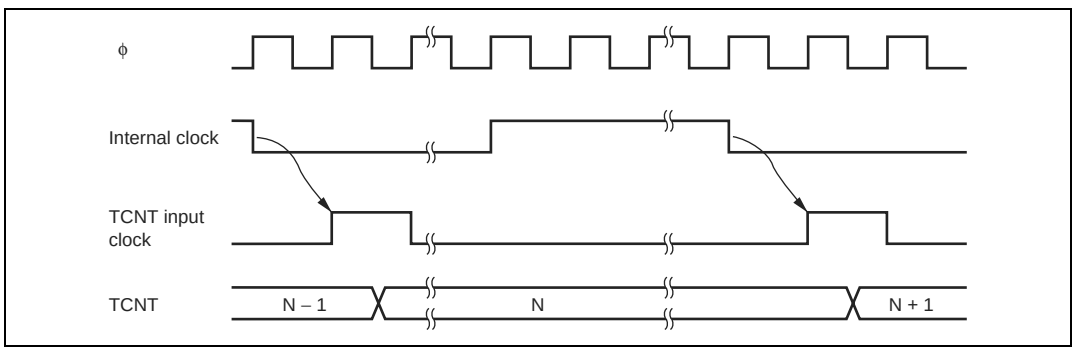


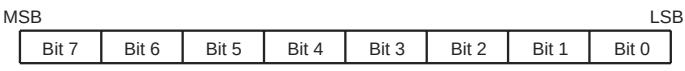

**Figure 12.3 Count Timing for Internal Clock Input**

**Table 14.5 Control Field for Locked Slave Unit**

| Setting Value | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function |
|---|---|---|---|---|---|
| H'0 | 0 | 0 | 0 | 0 | Reads slave status |
| H'4 | 0 | 1 | 0 | 0 | Reads locked address (upper 8 bits) |
| H'5 | 0 | 1 | 0 | 1 | Reads locked address (lower 4 bits) |

### (1) Slave Status Read (Control Bits: H'0, H'6)

The master unit can decide the reason the slave unit does not return the acknowledgement (ACK) by reading the slave status (H'0, H'6). The slave status indicates the result of the last communications that the slave unit performs. All slave units can provide slave status information. Figure 14.3 shows bit configuration of the slave status.




| Bit | Value | Description |
|---|---|---|
| Bit 7, bit 6 | 00 | Mode 0 — Indicates the highest mode supported by a unit.*1 |
| | 01 | Mode 1 |
| | 10 | Mode 2 |
| | 11 | For future use |
| Bit 5 | 0 | Fixed 0 |
| Bit 4*2 | 0 | Slave transmission halted |
| | 1 | Slave transmission enabled |
| Bit 3 | 0 | Fixed 0 |
| Bit 2 | 0 | Unit is unlocked |
| | 1 | Unit is locked |
| Bit 1*3 | 0 | Slave receive buffer is empty |
| | 1 | Slave receive buffer is not empty |
| Bit 0*4 | 0 | Slave transmit buffer is empty |
| | 1 | Slave transmit buffer is not empty |

Notes: 1. Since this LSI can support up to mode 2, bits 6 and 7 are fixed to 10.
2. The value of bit 4 can be selected by the STE bit in the IEBus master unit address register 1 (IEAR1).
3. The slave receive buffer is a buffer which is accessed during data write (control bits: H'8, H'A, H'B, H'E, H'F).
In this LSI, the slave receive buffer corresponds to the IEBus receive buffer register (IERBR); and bit 2 is the value of the RxRDY flag in the IEBus receive status register (IERSR).
4. The slave transmit buffer is a buffer which is accessed during data read (control bits: H'3, H'7).
In this LSI, the slave transmit buffer corresponds to the IEBus transmit buffer register (IETBR) when SRQ = 1 in the IEBus general flag register (IEFLG); and bit 1 is a value which reverses the TxRDY flag in the IEBus transmit/runaway status register (IETSR).

**Figure 14.3 Bit Configuration of Slave Status (SSR)**

[1] Clear the TRS bit in ICCR to 0 to switch from transmit mode to receive mode. Clear the ACKB bit in ICSR to 0 (acknowledge data setting). Clear the IRIC flag to 0, then set the WAIT bit in ICMR to 1.

[2] When ICDR is read (dummy data read), reception is started, and the receive clock is output, and data received, in synchronization with the internal clock.

[3] The IRIC flag is set to 1 by the following two conditions. At that point, an interrupt request is issued to the CPU if the IEIC bit in ICCR is set to 1.

(1) The flag is set at the falling edge of the 8th clock cycle of the receive clock for 1 frame. SCL is automatically held low, in synchronization with the internal clock, until the IRIC flag is cleared.

(2) The flag is set at the rising edge of the 9th clock cycle of the receive clock for 1 frame. The IRTR flag is set to 1, indicating that reception of 1 frame of data has ended. The master device continues to output the receive clock for the receive data.

[4] Read the IRTR flag in ICSR. If the IRTR flag value is 0, the wait state is cancelled by clearing the IRIC flag as described in step [6] below. If the IRTR flag value is 1 and the next receive data is the final receive data, perform the end processing described in step [7] below.

[5] If the IRTR flag value is 1, read the ICDR receive data.

[6] Clear the IRIC flag to 0. The reading of the ICDR flag described in step [5] and the clearing of the IRIC flag to 0 should be performed consecutively, with no interrupt processing occurring between them. During wait operation, clear the IRIC flag to 0 when the value of counter BC2 to BC0 is 2 or greater. If the IRIC flag is cleared to 0 when the value of counter BC2 to BC0 is 1 or 0, it will not be possible to determine when the transfer has completed. If condition [3]-1 is true, the master device drives SDA to low level and returns an acknowledge signal when the receive clock outputs the 9th clock cycle.

Further data can be received by repeating steps [3] through [6].

[7] Set the ACKB bit in ICSR to 1 to set the acknowledge data for the final receive.

[8] Wait for at least 1 clock cycle after the IRIC flag is set to 1 and then wait for the rising edge of the 1st clock cycle of the next receive data.

[9] Set the TSR bit in ICCR to 1 to switch from the receive mode to the transmit mode. The TSR bit setting value at this point becomes valid when the rising edge of the next 9th clock cycle is input.

[10] Read the ICDR receive data.

[11] Clear the IRIC flag to 0. As in step [6], read the ICDR flag and clear the IRIC flag to 0 consecutively, with no interrupt processing occurring between them. During wait operation, clear the IRIC flag to 0 when the value of counter BC2 to BC0 is 2 or greater.

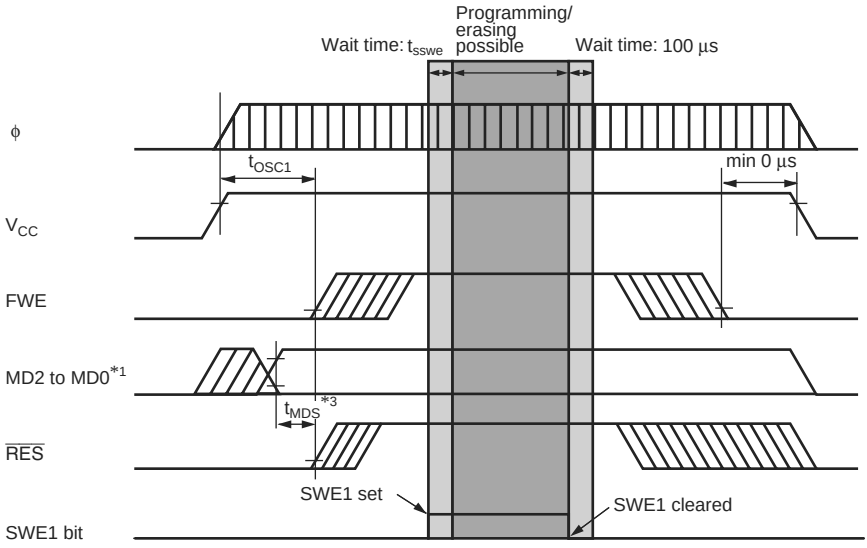
[12] The IRIC flag is set to 1 by the following two conditions.

| This LSI | | | | Socket Adapter (Conversion to 40-Pin Arrangement) | HN27C4096HG (40-Pin) | |
|---|---|---|---|---|---|---|
| Pin No. | | | Pin Name | | Pin No. | Pin Name |
| FP-100B*3,TFP-100B, TFP-100G*4 | FP-100A*1 | BP-112*2 TBP-112A*5 | | | | |
| 13 | 16 | F1 | A0 | | 21 | A0 |
| 15 | 18 | G1 | A1 | | 22 | A1 |
| 16 | 19 | G2 | A2 | | 23 | A2 |
| 17 | 20 | G3 | A3 | | 24 | A3 |
| 18 | 21 | H1 | A4 | | 25 | A4 |
| 19 | 22 | G4 | A5 | | 26 | A5 |
| 20 | 23 | H2 | A6 | | 27 | A6 |
| 21 | 24 | J1 | A7 | | 28 | A7 |
| 22 | 25 | H3 | A8 | | 29 | A8 |
| 23 | 26 | J2 | A9 | | 31 | A9 |
| 24 | 27 | K1 | A10 | | 32 | A10 |
| 25 | 28 | J3 | A11 | | 33 | A11 |
| 26 | 29 | K2 | A12 | | 34 | A12 |
| 27 | 30 | L2 | A13 | | 35 | A13 |
| 28 | 31 | H4 | A14 | | 36 | A14 |
| 29 | 32 | K3 | A15 | | 37 | A15 |
| 30 | 33 | L3 | A16 | | 38 | A16 |
| 31 | 34 | J4 | A17 | | 39 | A17 |
| 32 | 35 | K4 | A18 | | 10 | A18 |
| 4 | 7 | C2 | D0 | | 19 | I/O0 |
| 5 | 8 | C1 | D1 | | 18 | I/O1 |
| 6 | 9 | D3 | D2 | | 17 | I/O2 |
| 7 | 10 | D2 | D3 | | 16 | I/O3 |
| 8 | 11 | D1 | D4 | | 15 | I/O4 |
| 9 | 12 | E4 | D5 | | 14 | I/O5 |
| 10 | 13 | E3 | D6 | | 13 | I/O6 |
| 11 | 14 | E1 | D7 | | 12 | I/O7 |
| 3 | 6 | D4 | $\overline{CE}$ | | 2 | $\overline{CE}$ |
| 1 | 4 | B2 | $\overline{OE}$ | | 20 | $\overline{OE}$ |
| 2 | 5 | B1 | $\overline{WE}$ | | 3 | $\overline{WE}$ |
| 66 | 69 | E10 | FWE | | 4 | FWE |
| 99, 75, 72*1, 62, 61, 60, 54, 53, 12 | 78, 75, 65, 64, 57, 54, 15, 2 | E2, F3, H8, J10, G9, G11, F9, G10, C9, B3 | $V_{CC}$ | | 40, 1 | $V_{CC}$ |
| | | | | | 30, 11 | $V_{SS}$ |
| | | | | | 7, 6, 5 | NC |
| | | | | | 8 | A20 |
| | | | | | 9 | A19 |
| 100, 67, 64, 58, 56, 55, 42, 40, 38, 14 | 70, 67, 61, 59, 58, 45, 43, 41, 17, 3 | F2, F4, J6, K6, K7, L7, J11, H9, H11, F8, F10, E9, A2 | $V_{SS}$ | | | |
| 59 | 62 | G8 | $\overline{RES}$ | Power-on reset circuit | | |
| 63 | 66 | F11 | XTAL | Oscillator circuit | | |
| 65 | 68 | E11 | EXTAL | | | |
| Other than the above | Other than the above | Other than the above | NC (OPEN) | | | |

Legend:
FWE: Flash write enable
I/O7 to 0: Data input/output
A18 to 0: Address input
$\overline{OE}$: Output enable
$\overline{CE}$: Chip enable
$\overline{WE}$: Write enable

Notes: 1. Supported only by the H8S/2258 and H8S/2238B.
2. Supported only by the H8S/2238R.
3. Not supported by the H8S/2227.
4. Not supported by the H8S/2258.
5. Supported only by the H8S/2238R and H8S/2239.

**Figure 20.13 Socket Adapter Pin Correspondence Diagram**



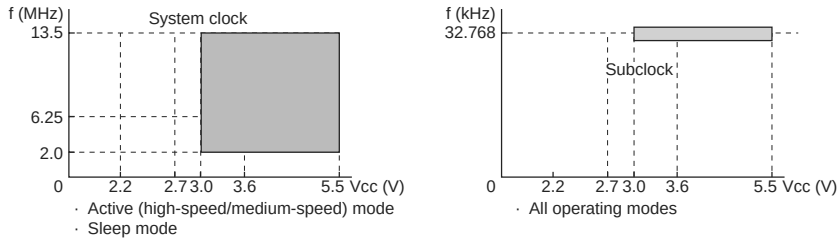

Period during which flash memory access is prohibited ($t_{sswe}$: Wait time after setting SWE1 bit)*2

Period during which flash memory can be programmed (Execution of program in flash memory prohibited, and data reads other than verify operations prohibited)

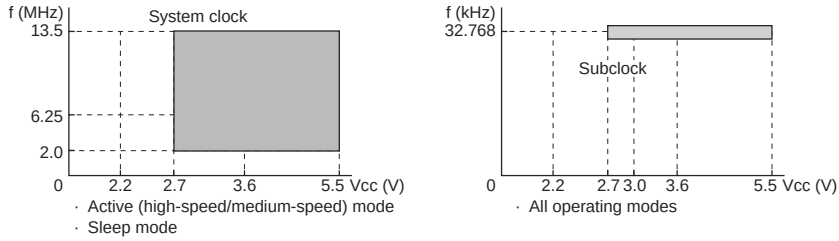
Notes: 1. Except when switching modes, the level of the mode pins (MD2 to MD0) must be fixed until power-off by pulling the pins up or down.
2. See sections 27.2.6, 27.3.6, 27.4.6, 27.5.6 and 27.6.6, Flash Memory Characteristics.
3. Mode programming setup time $t_{MDS}$ (min) = 200 ns.

**Figure 20.15 Power-On/Off Timing (User Program Mode)**

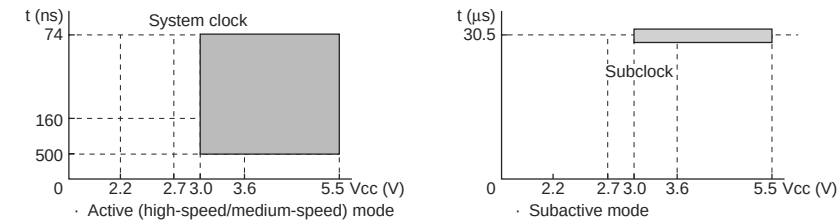
(1) Power supply voltage and oscillation frequency range (F-ZTAT version)



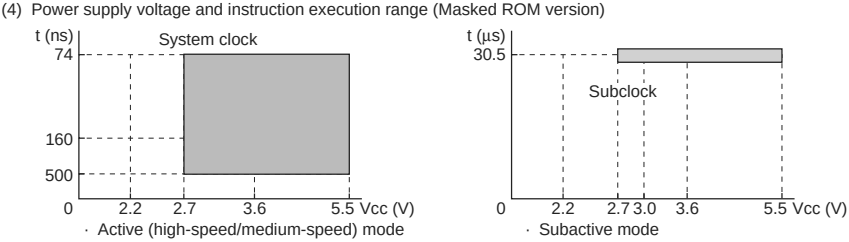

(2) Power supply voltage and oscillation frequency range (Masked ROM version)



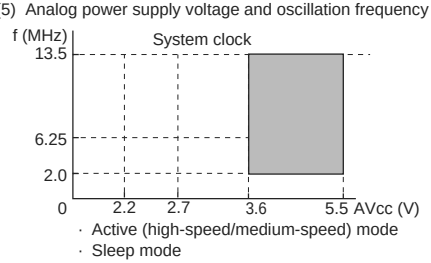

(3) Power supply voltage and instruction execution range (F-ZTAT version)




(4) Power supply voltage and instruction execution range (Masked ROM version)




(5) Analog power supply voltage and oscillation frequency range (F-ZTAT version, Masked ROM version)




Note: See sections 27.4.4, A/D Convesion Characteristics and 27.4.5, D/A Convesion Characteristics for the operation range of AVcc.

**Figure 27.3 Power Supply Voltage and Operating Ranges (H8S/2238B and H8S/2236B)**

| Item | Symbol | Condition A | | Condition B | | Condition C | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| External clock output stabilization delay time | $t_{DEXT}$ | 500 | — | 500 | — | 1000 | — | µs | Figure 27.11 |
| Subclock oscillation stabilization time | $t_{OSC3}$ | — | 2 | — | 2 | — | 3 | s | |
| Subclock oscillator frequency | $f_{SUB}$ | 32.768 | 32.768 | 32.768 | 32.768 | 32.768 | 32.768 | kHz | |
| Subclock ($\phi_{SUB}$) cycle time | $t_{SUB}$ | 30.5 | 30.5 | 30.5 | 30.5 | 30.5 | 30.5 | µs | |