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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2239fa20iv

- Compact package

Package	(Code)*6	Body Size	Pin Pitch
TQFP-100	TFP-100B, TFP-100BV	14.0 × 14.0 mm	0.5 mm
TQFP-100*1	TFP-100G, TFP-100GV	12.0 × 12.0 mm	0.4 mm
QFP-100*2	FP-100A, FP-100AV	14.0 × 20.0 mm	0.65 mm
QFP-100*3	FP-100B, FP-100BV	14.0 × 14.0 mm	0.5 mm
LFBGA-112*4	BP-112, BP-112V	10.0 × 10.0 mm	0.8 mm
TFBGA-112*5	TBP-112A, TBP-112AV	10.0 × 10.0 mm	0.8 mm

Notes: 1. Not supported by the H8S/2258 Group.
2. Supported only by the H8S/2258 Group, H8S/2238B, H8S/2236B, H8S/2237 Group, and HD6432227.
3. Not supported by the HD64F2227.
4. Supported only by the HD64F2238R.
5. Supported only by theHD64F2238R and HD64F2239.
6. Package code ending in the letter V designate Pb-free Product.

- DMACR_0B and DMACR_1B

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved This bit can be read from or written to. However, the write value should always be 0.
6	DAID	0	R/W	Destination Address Increment/Decrement
5	DAIDE	0	R/W	Destination Address Increment/Decrement Enable These bits specify whether destination address register MARB is to be incremented, decremented, or left unchanged, when data transfer is performed. 00: MARB is fixed 01: MARB is incremented after a data transfer • When DTSZ = 0, MARB is incremented by 1 • When DTSZ = 1, MARB is incremented by 2 10: MARB is fixed 11: MARB is decremented after a data transfer • When DTSZ = 0, MARB is decremented by 1 • When DTSZ = 1, MARB is decremented by 2
4	—	0	R/W	Reserved This bit can be read from or written to. However, the write value should always be 0.

Transfer Mode		Transfer Source	Remarks
Full address mode	Normal mode (1) Auto-request • Transfer request is internally held • Number of transfers (1 to 65,536) is continuously sent • Burst/cycle steal transfer can be selected	• Auto-request	• Max. 2-channel operation, combining channels A and B
	(2) External request • 1-byte or 1-word transfer for a single transfer request • Number of transfers: 1 to 65,536	• External request	
	Block transfer mode • Transfer of 1-block, size selected for a single transfer request • Number of transfers: 1 to 65,536 • Source or destination can be selected as block area • Block size: 1 to 256 bytes or word	• TPU channel 0 to 5 compare match/input capture A interrupt • SCI transmit-data-empty interrupt • SCI receive-data-full interrupt • A/D converter conversion end interrupt • External request	

11.3.5 Timer Status Register (TSR)

The TSR registers indicate the status of each channel. The TPU of the H8S/2227 Group has a total of three TSR registers, one each for channels 0 to 2. In other groups, the TPU has a total of six TSR registers, one each for channels 0 to 5.

Bit	Bit Name	Initial value	R/W	Description
7	TCFD	1	R	Count Direction Flag Status flag that shows the direction in which TCNT counts in channels 1, 2, 4*3, and 5*3. In channels 0 and 3*3, bit 7 is reserved. It is always read as 1 and cannot be modified. 0: TCNT counts down 1: TCNT counts up
6	—	1	—	Reserved This bit is always read as 1 and cannot be modified.
5	TCFU	0	R/(W)*1	Underflow Flag Status flag that indicates that TCNT underflow has occurred when channels 1, 2, 4*3, and 5*3 are set to phase counting mode. In channels 0 and 3*3, bit 5 is reserved. It is always read as 0 and cannot be modified. [Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF) [Clearing condition] When 0 is written to TCFU after reading TCFU = 1
4	TCFV	0	R/(W)*1	Overflow Flag Status flag that indicates that TCNT overflow has occurred. [Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000) [Clearing condition] When 0 is written to TCFV after reading TCFV = 1

12.3.3 Time Constant Register B (TCORB)

TCORB is an 8-bit readable/writable register. TCORB_0 and TCORB_1 (TCORB_2 and TCORB_3)* comprise a single 16-bit register, so they can be accessed together by word access.

TCORB is continually compared with the value in TCNT. When a match is detected, the corresponding compare-match flag B (CMFB) in TCSR is set. Note, however, that comparison is disabled during the T2 state of a TCORB write cycle.

The timer output from the TMO pin can be freely controlled by the compare-match signal B and the settings of output select bits OS1 and OS0 in TCSR.

The initial value of TCORB is H'FF.

Note: * Not available in the H8S/2237 Group and H8S/2227 Group.

12.3.4 Timer Control Register (TCR)

TCR selects the TCNT clock source and the time at which TCNT is cleared, and controls interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	CMIEB	0	R/W	Compare-Match Interrupt Enable B Selects whether the CMFB interrupt request (CMIB) is enabled or disabled when the CMFB flag in TCSR is set to 1. 0: CMFB interrupt request (CMIB) is disabled 1: CMFB interrupt request (CMIB) is enabled
6	CMIEA	0	R/W	Compare-Match Interrupt Enable A Selects whether the CMFA interrupt request (CMIA) is enabled or disabled when the CMFA flag in TCSR is set to 1. 0: CMFA interrupt request (CMIA) is disabled 1: CMFA interrupt request (CMIA) is enabled
5	OVIE	0	R/W	Timer Overflow Interrupt Enable Selects whether the OVF interrupt request (OVI) is enabled or disabled when the OVF flag in TCSR is set to 1. 0: OVF interrupt request (OVI) is disabled 1: OVF interrupt request (OVI) is enabled

14.1.3 Transfer Data (Data Field Contents)

The data filed contents are specified by the control bits.

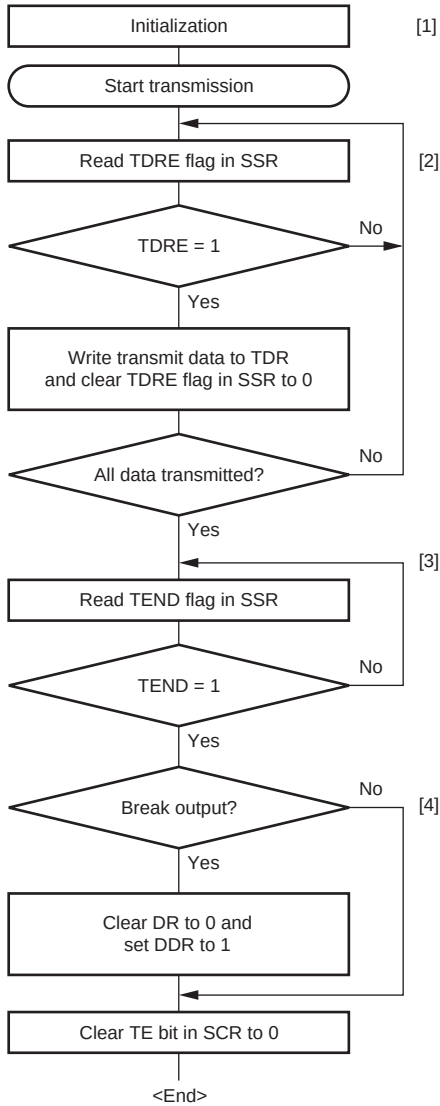
Table 14.4 Control Bit Contents

Setting Value	Bit 3*1	Bit 2	Bit 1	Bit 0	Function*2
H'0	0	0	0	0	Reads slave status (SSR)
H'1	0	0	0	1	Undefined — do not use
H'2	0	0	1	0	Undefined — do not use
H'3	0	0	1	1	Reads data and locks
H'4	0	1	0	0	Reads locked address (lower 8 bits)
H'5	0	1	0	1	Reads locked address (upper 4 bits)
H'6	0	1	1	0	Reads slave status (SSR) and unlocks
H'7	0	1	1	1	Reads data
H'8	1	0	0	0	Undefined — do not use
H'9	1	0	0	1	Undefined — do not use
H'A	1	0	1	0	Writes command and locks
H'B	1	0	1	1	Writes data and locks
H'C	1	1	0	0	Undefined — do not use
H'D	1	1	0	1	Undefined — do not use
H'E	1	1	1	0	Writes command
H'F	1	1	1	1	Writes data

Notes: 1. According to the value of bit 3 (MSB), the transfer directions of the message length bits in the following message length field and data in the data field vary.
When bit 3 is 1: Data is transferred from the master unit to the slave unit.
When bit 3 is 0: Data is transferred from the slave unit to the master unit.
2. H'3, H'6, H'A, and H'B are control bits to specify lock setting and cancellation.
When the undefined values of H'1, H'2, H'8, H'9, H'C, and H'D are transmitted, the acknowledge bit is not returned.

When the control bits received from another unit which locked are not included in table 14.5, the slave unit which has been locked by the master unit rejects acceptance of the control bits and does not return the acknowledge bit.

Figure 15.10 shows a sample flowchart for data transmission.



[1] SCI initialization:
The TxD pin is automatically designated as the transmit data output pin.
After the TE bit is set to 1, a frame of 1s is output, and transmission is enabled.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:
To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and then clear the TDRE flag to 0. Checking and clearing of the TDRE flag is automatic when the DMAC*1 or the DTC*2 is activated by a transmit-data-empty interrupt (TXI) request, and data is written to TDR.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, set DR for the port corresponding to the TxD pin to 0, clear DDR to 1, then clear the TE bit in SCR to 0.

Notes: 1. Supported only by the H8S/2239 Group.
2. The case, in which the DTC automatically checks and clears the TDRE flag, occurs only when DISEL in DTC is 0 with the transfer counter not being 0. Therefore, the TDRE flag should be cleared by CPU when DISEL is 1, or when DISEL is 0 with the transfer counter being 0.

Figure 15.10 Sample Serial Transmission Flowchart

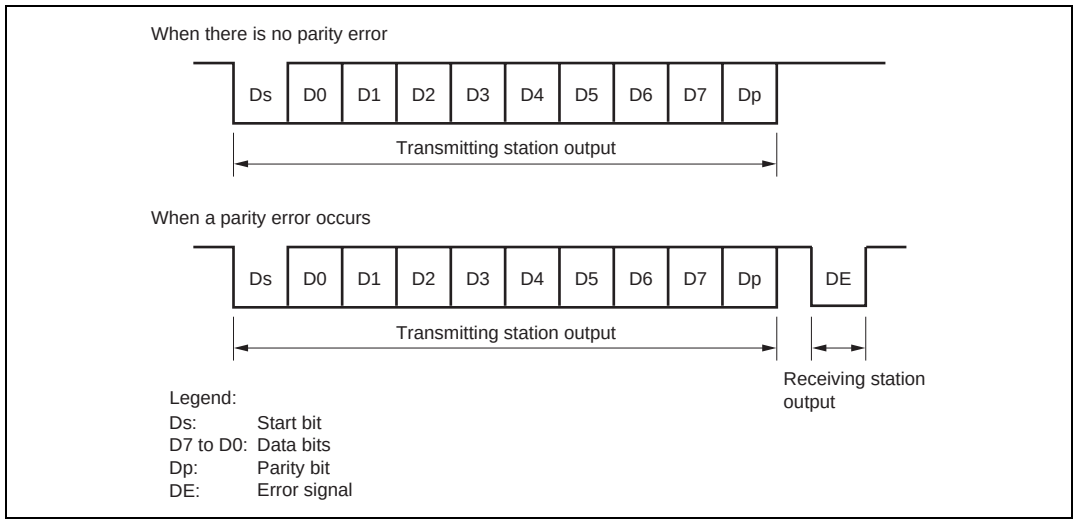


Figure 15.25 Normal Smart Card Interface Data Format

Data transfer with other types of IC cards (direct convention and inverse convention) are performed as described in the following.

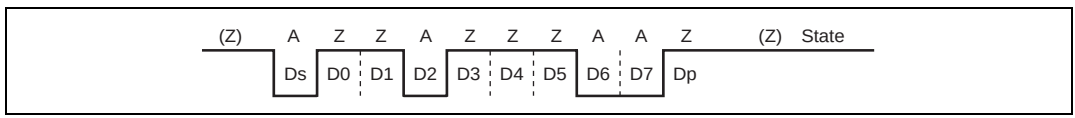


Figure 15.26 Direct Convention (SDIR = SINV = O/$\overline{E}$ = 0)

With the direction convention type IC and the above sample start character, the logic 1 level corresponds to state Z and the logic 0 level to state A, and transfer is performed in LSB-first order. The start character data above is H'3B. For the direct convention type, clear the SDIR and SINV bits in SCMR to 0. According to Smart Card regulations, clear the O/$\overline{E}$ bit in SMR to 0 to select even parity mode.

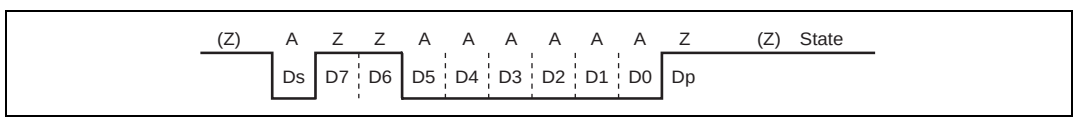


Figure 15.27 Inverse Convention (SDIR = SINV = O/$\overline{E}$ = 1)

With the inverse convention type, the logic 1 level corresponds to state A and the logic 0 level to state Z, and transfer is performed in MSB-first order. The start character data for the above is H'3F. For the inverse convention type, set the SDIR and SINV bits in SCMR to 1. According to Smart Card regulations, even parity mode is the logic 0 level of the parity bit, and corresponds to

ICE is 1. For details on the module stop control register, refer to section 24.1.2, Module Stop Control Registers A to C (MSTPCRA to MSTPCRC).

- I²C bus data register_0 (ICDR_0)*
- Slave address register_0 (SAR_0)*
- Second slave address register_0 (SARX_0)*
- I²C bus mode register_0 (ICMR_0)*
- I²C bus control register_0 (ICCR_0)*
- I²C bus status register_0 (ICSR_0)*
- I²C bus data register_1 (ICDR_1)*
- Slave address register_1 (SAR_1)*
- Second slave address register_1 (SARX_1)*
- I²C bus mode register_1 (ICMR_1)*
- I²C bus control register_1 (ICCR_1)*
- I²C bus status register_1 (ICSR_1)*
- DDC switch register (DDCSWR)
- Serial control register X (SCRX)

Note: * Some of the registers in the I²C bus interface are allocated to the same addresses of other registers. The IICE bit in serial control register X (SCRX) selects each register.

16.3.1 I²C Bus Data Register (ICDR)

ICDR is an 8-bit readable/writable register that is used as a transmit data register when transmitting and a receive data register when receiving. ICDR is divided internally into a shift register (ICDRS), receive buffer (ICDRR), and transmit buffer (ICDRT). Data transfers among the three registers are performed automatically in coordination with changes in the bus state, and affect the status of internal flags such as TDRE and RDRF. When TDRE is 1 and the transmit buffer is empty, TDRE shows that the next transmit data can be written from the CPU. When RDRF is 1, it shows that the valid receive data is stored in the receive buffer.

If I²C is in transmit mode and the next data is in ICDRT (the TDRE flag is 0) following transmission/reception of one frame of data using ICDRS, data is transferred automatically from ICDRT to ICDRS. If I²C is in receive mode and no previous data remains in ICDRR (the RDRF flag is 0) following transmission/reception of one frame of data using ICDRS, data is transferred automatically from ICDRS to ICDRR.

If the number of bits in a frame, excluding the acknowledge bit, is less than 8, transmit data and receive data are stored differently. Transmit data should be written justified toward the MSB side

11. Notes on ICDR Reads and ICCR Access in Slave Transmit Mode

In a transmit operation in the slave mode of the I²C bus interface, do not read the ICDR register or read or write to the ICCR register during the period indicated by the shaded portion in figure 16.25.

Normally, when interrupt processing is triggered in synchronization with the rising edge of the 9th clock cycle, the period in question has already elapsed when the transition to interrupt processing takes place, so there is no problem with reading the ICDR register or reading or writing to the ICCR register.

To ensure that the interrupt processing is performed properly, one of the following two conditions should be applied.

(1) Make sure that reading received data from the ICDR register, or reading or writing to the ICCR register, is completed before the next slave address receive operation starts.

(2) Monitor the BC2 to BC0 counter in the ICMR register and, when the value of BC2 to BC0 is 000 (8th or 9th clock cycle), allow a waiting time of at least 2 transfer clock cycles in order to involve the problem period in question before reading from the ICDR register, or reading or writing to the ICCR register.

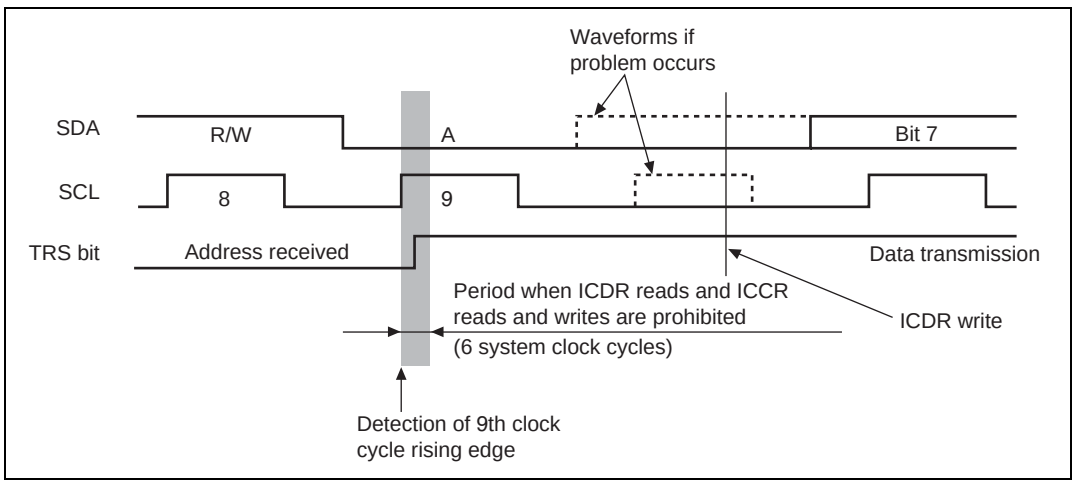


Figure 16.25 ICDR Read and ICCR Access Timing in Slave Transmit Mode

Do Not Set or Clear the SWE1 Bit during Execution of a Program in Flash Memory: Wait for at least 100 µs after clearing the SWE1 bit before executing a program or reading data in flash memory.

When the SWE1 bit is set, data in flash memory can be rewritten. Access flash memory only for verify operations (verification during programming/erasing). Also, do not clear the SWE1 bit during programming, erasing, or verifying. Similarly, when using the RAM emulation function while a high level is being input to the FWE pin, the SWE1 bit must be cleared before executing a program or reading data in flash memory.

However, the RAM area overlapping flash memory space can be read and written to regardless of whether the SWE1 bit is set or cleared.

Do Not Use Interrupts while Flash Memory Is Being Programmed or Erased: All interrupt requests, including NMI, should be disabled during FWE application to give priority to program/erase operations.

Do Not Perform Additional Programming. Erase the Memory before Reprogramming: In on-board programming, perform only one programming operation on a 128-byte programming unit block. In programmer mode, too, perform only one programming operation on a 128-byte programming unit block. Programming should be carried out with the entire programming unit block erased.

Before Programming, Check That the Chip Is Correctly Mounted in the PROM Programmer: Overcurrent damage to the device can result if the index marks on the PROM programmer socket, socket adapter, and chip are not correctly aligned.

Do Not Touch the Socket Adapter or Chip during Programming: Touching either of these can cause contact faults and write errors.

Reset the Flash Memory before Turning on the Power: To reset the flash memory during oscillation stabilization period, the reset signal must be input for at least 100 µs.

Apply the Reset Signal while SWE Is Low to Reset the Flash Memory during its operation: The reset signal is applied at least 100 µs after the SWE bit has been cleared.

Section 22 PROM

The PROM version can be set to PROM mode and programmed with a PROM programmer.

22.1 PROM Mode Setting

The PROM version (HD6472237) suspends its microcomputer functions when placed in PROM mode, enabling the on-chip PROM to be programmed. This programming can be done with a PROM programmer set up in the same way as for the HN27C101 (V_{PP} = 12.5 V) EPROM. Use of a socket adapter to convert from 100 pins to 32 pins enables programming with a commercial PROM programmer.

Caution is required when selecting the PROM programmer, as this LSI does not support page mode.

Table 22.1 shows how PROM mode is selected.

Table 22.1 Selecting PROM Mode

Pin Names	Setting
MD2, MD1, MD0	Low
$\overline{\text{STBY}}$	
PA2, PA1	High

22.2 Socket Adapter and Memory Map

Programs can be written and verified by attaching a socket adapter to convert from 100 pins to 32 pins to the PROM programmer. Figure 22.1 shows the wiring of the socket adapter, and table 22.2 gives ordering information for the socket adapter. Figure 22.2 shows the memory map in PROM mode.

23.9.2 Note on Board Design

When designing the board, place the crystal resonator and its load capacitors as close as possible to the EXTAL, XTAL, OSC1, and OSC2 pins. Make wires as short as possible. Other signal lines should be routed away from the oscillator circuit, as shown in figure 23.11. This is to prevent induction from interfering with correct oscillation.

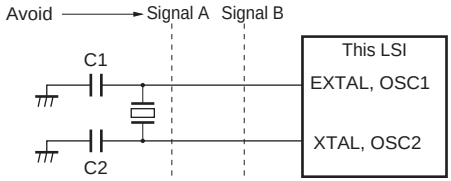


Figure 23.11 Note on Board Design of Oscillator Circuit

24.9 Subactive Mode

24.9.1 Transition to Subactive Mode

When the SLEEP instruction is executed in high-speed mode with the SSBY bit in SBYCR = 1, the DTON bit in LPWRCR = 1, the LSON bit = 1, and the PSS bit in TCSR_1 (WDT_1) = 1, CPU operation shifts to subactive mode. When an interrupt occurs in watch mode, and if the LSON bit of LPWRCR is 1, a transition is made to subactive mode. And if an interrupt occurs in subsleep mode, a transition is made to subactive mode.

In subactive mode, the CPU operates at low speed on the subclock, and the program is executed step by step. Peripheral modules other than PBC, TMR_0 to TMR_3, WDT_0, and WDT_1, and system clock oscillator are also stopped.

When operating the CPU in subactive mode, the SCKCR SCK2 to SCK0 bits must be set to 0.

24.9.2 Exiting Subactive Mode

Subactive mode is exited by the SLEEP instruction or the $\overline{\text{RES}}$, $\overline{\text{MRES}}$ or $\overline{\text{STBY}}$ pin.

- Exiting Subactive Mode by SLEEP Instruction

  When the SLEEP instruction is executed with the SSBY bit in SBYCR = 1, the DTON bit in LPWRCR = 0, and the PSS bit in TCSR_1 (WDT_1) = 1, the CPU exits subactive mode and a transition is made to watch mode. When the SLEEP instruction is executed with the SSBY bit in SBYCR = 0, the LSON bit in LPWRCR = 1, and the PSS bit in TCSR_1 (WDT_1) = 1, a transition is made to subsleep mode. Finally, when the SLEEP instruction is executed with the SSBY bit in SBYCR = 1, the DTON bit in LPWRCR = 1, the LSON bit = 0, and the PSS bit in TCSR_1 (WDT_1) = 1, a direct transition is made to high-speed mode (SCK2 to SCK0 all 0).
- Exiting Subactive Mode by $\overline{\text{RES}}$ Pin or $\overline{\text{MRES}}$ Pin

  For exiting subactive mode by the RES or MRES pin, see section 24.4.2, Clearing Software Standby Mode.
- Exiting Subactive Mode by $\overline{\text{STBY}}$ Pin

  When the $\overline{\text{STBY}}$ pin level is driven low, a transition is made to hardware standby mode.

Register Name	Abbreviation	Bit No.	Address*1	Module	Data Bus Width	Access State
I²C bus status register_1	ICSR_1	8	H'FF81*3	IIC_1	8	2
Serial control register_1	SCR_1	8	H'FF82	SCI_1	8	2
Transmit data register_1	TDR_1	8	H'FF83	SCI_1	8	2
Serial status register_1	SSR_1	8	H'FF84	SCI_1	8	2
Receive data register_1	RDR_1	8	H'FF85	SCI_1	8	2
Smart card mode register_1	SCMR_1	8	H'FF86*3	SCI_1	8	2
I²C bus data register_1	ICDR_1	8	H'FF86*3	IIC_1	8	2
Second slave address register_1	SARX_1	8	H'FF86*3	IIC_1	8	2
I²C bus mode register_1	ICMR_1	8	H'FF87	IIC_1	8	2
Slave address register_1	SAR_1	8	H'FF87	IIC_1	8	2
Serial mode register_2	SMR_2	8	H'FF88	SCI_2	8	2
Bit rate register_2	BRR_2	8	H'FF89	SCI_2	8	2
Serial control register_2	SCR_2	8	H'FF8A	SCI_2	8	2
Transmit data register_2	TDR_2	8	H'FF8B	SCI_2	8	2
Serial status register_2	SSR_2	8	H'FF8C	SCI_2	8	2
Receive data register_2	RDR_2	8	H'FF8D	SCI_2	8	2
Smart card mode register_2	SCMR_2	8	H'FF8E	SCI_2	8	2
A/D data register AH	ADDRAH	8	H'FF90	A/D	8	2
A/D data register AL	ADDRAL	8	H'FF91	A/D	8	2
A/D data register BH	ADDRBH	8	H'FF92	A/D	8	2
A/D data register BL	ADDRBL	8	H'FF93	A/D	8	2
A/D data register CH	ADDRCH	8	H'FF94	A/D	8	2
A/D data register CL	ADDRCL	8	H'FF95	A/D	8	2
A/D data register DH	ADDRDH	8	H'FF96	A/D	8	2
A/D data register DL	ADDRDL	8	H'FF97	A/D	8	2
A/D control/status register	ADCSR	8	H'FF98	A/D	8	2
A/D control register	ADCR	8	H'FF99	A/D	8	2
Timer control/status register_1	TCSR_1	8	H'FFA2	WDT_1	16	2
Timer counter_1	TCNT_1	8	H'FFA2 (write)	WDT_1	16	2
Timer counter_1	TCNT_1	8	H'FFA3 (read)	WDT_1	16	2
Flash memory control register 1	FLMCR1	8	H'FFA8	FLASH	8	2

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
IPRF	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	INT
IPRG	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRH	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRI	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRJ	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRK	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRL	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRO	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
ABWCR	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0	BSC
ASTCR	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0	
WCRH	W71	W70	W61	W60	W51	W50	W41	W40	
WCRL	W31	W30	W21	W20	W11	W10	W01	W00	
BCRH	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	—	—	—	
BCRL	BRLE	—	—	—	—	—	—	WAITE	
RAMER	—	—	—	—	RAMS	RAM2	RAM1	RAM0	FLASH
MAR_0A	—	—	—	—	—	—	—	—	DMAC
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
IOAR_0A	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
ETCR_0A	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
MAR_0B	—	—	—	—	—	—	—	—	
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
IOAR_0B	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
ETCR_0B	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Table 27.27 DC Characteristics (2)

Condition A (F-ZTAT version): V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.6 V to 5.5 V,
V_{ref} = 3.6 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)*1

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
	NMI		—	—	30	pF	
	P32 to P35		—	—	20	pF	
	All input pins except the above		—	—	15	pF	
Current dissipation*2	Normal operation	I_{CC}*4	—	23 V_{CC} = 3.0 V	40 V_{CC} = 5.5 V	mA	f = 13.5 MHz
	Sleep mode		—	18 V_{CC} = 3.0 V	30 V_{CC} = 5.5 V	mA	f = 13.5 MHz
	All modules stopped		—	13	—	mA	f = 13.5 MHz, V_{CC} = 3.0 V (reference values)
	Medium-speed mode (ϕ/32)		—	13	—	mA	f = 13.5 MHz, V_{CC} = 3.0 V (reference values)
	Subactive mode		—	80	180	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used
	Subsleep mode		—	60	130	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used
	Watch mode		—	8	40	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used

27.5 Electrical Characteristics of H8S/2238R and H8S/2236R

27.5.1 Absolute Maximum Ratings

Table 27.38 lists the absolute maximum ratings.

Table 27.38 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +4.3	V
	CV_{CC}	–0.3 to +4.3	V
Input voltage (except ports 4 and 9)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (ports 4 and 9)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75*1	°C
		Wide-range specifications: –40 to +85*2	
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum rating are exceeded.

Notes: 1. When the operating voltage in read is V_{CC} = 2.7 V to 3.6 V, the operating temperature ranges for flash memory programming/erasing are T_a = –20°C to +75°C. When the operating voltage in read is V_{CC} = 2.2 V to 3.6 V, the operating temperature ranges for flash memory programming/erasing are T_a = –20°C to +50°C.

2. The operating temperature ranges for flash memory programming/erasing are T_a = –40°C to +80°C (regular specifications).