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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2239fa20v

Section 22 PROM

Section 23 Clock Pulse Generator

Section 24 Power-Down Modes

Section 25 Power Supply Circuit

Section 27 Electrical Characteristics

5.5 Operation

5.5.1 Interrupt Control Modes and Interrupt Operation

Interrupt operations in this LSI differ depending on the interrupt control mode.

NMI interrupts are accepted at all times except in the reset state and the hardware standby state. In the case of IRQ interrupts and on-chip peripheral module interrupts, an enable bit is provided for each interrupt. Clearing an enable bit to 0 disables the corresponding interrupt request. Interrupt sources for which the enable bits are set to 1 are controlled by the interrupt controller.

Table 5.3 shows the interrupt control modes.

The interrupt controller performs interrupt control according to the interrupt control mode set by the INTM1 and INTM0 bits in SYSCR, the priorities set in IPR, and the masking state indicated by the I bit in the CPU's CCR, and bits I2 to I0 in EXR.

Table 5.3 Interrupt Control Modes

Interrupt Control Mode	SYSCR		Priority Setting Registers	Interrupt Mask Bits	Description
	INTM1	INTM0			
0	0	0	—	I	Interrupt mask control is performed by the I bit.
—		1	—	—	Setting prohibited
2	1	0	IPR	I2 to I0	8-level interrupt mask control is performed by bits I2 to I0. 8 priority levels can be set with IPR.
—		1	—	—	Setting prohibited

16-Bit 3-State Access Space: Figures 7.15 to 7.17 show bus timings for a 16-bit 3-state access space. When a 16-bit access space is accessed , the upper half (D15 to D8) of the data bus is used for the even address, and the lower half (D7 to D0) for the odd address.

Wait states can be inserted.

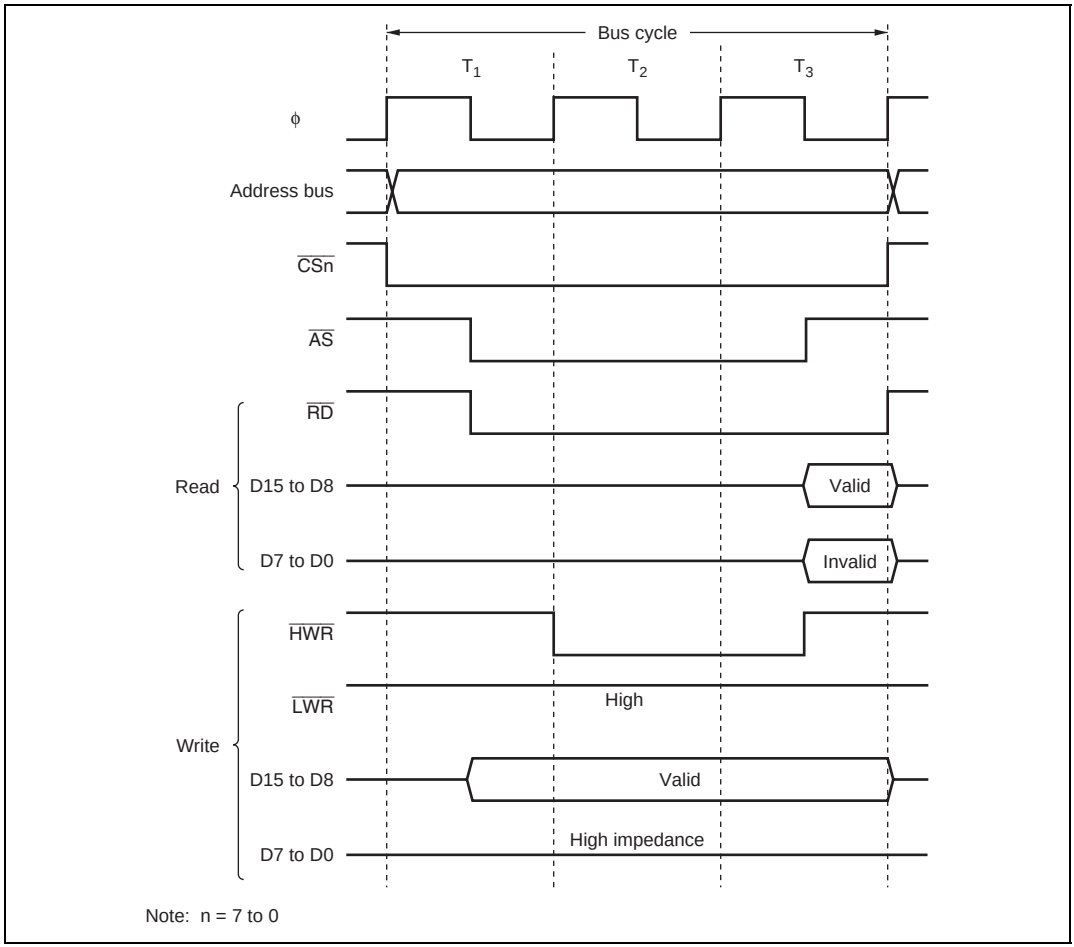
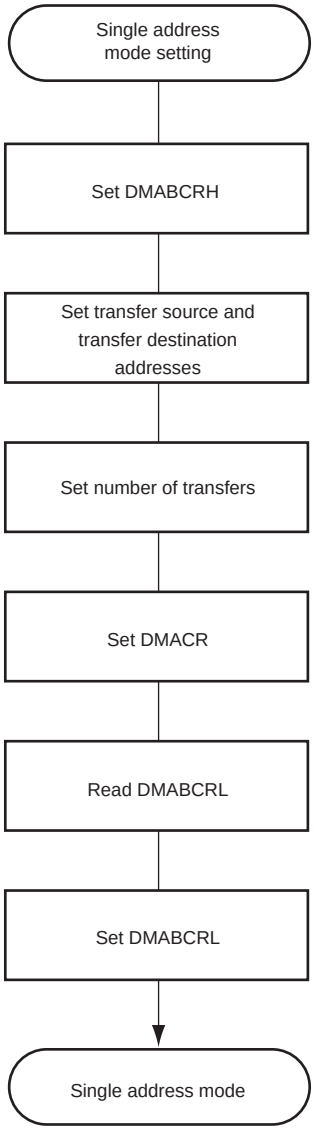


Figure 7.15 Bus Timing for 16-Bit 3-State Access Space (1) (Even Address Byte Access)



[1] Set each bit in DMABCRH.
- Clear the FAE bit to 0 to select short address mode.
- Set the SAE bit to 1 to select single address mode.
- Specify enabling or disabling of internal interrupt clearing with the DTA bit.

[2] Set the transfer source address/transfer destination address in MAR.

[3] Set the number of transfers in ETCR.

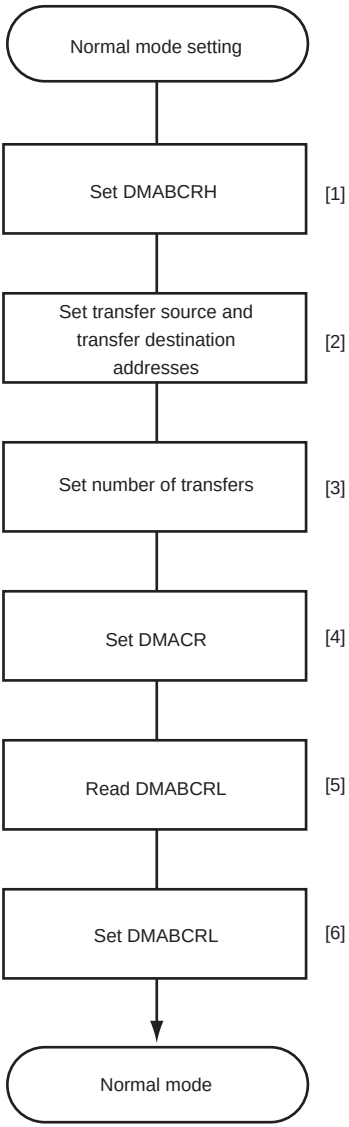
[4] Set each bit in DMACR.
- Set the transfer data size with the DTSZ bit.
- Specify whether MAR is to be incremented or decremented with the DTID bit.
- Clear the RPE bit to 0 to select sequential mode.
- Specify the transfer direction with the DTDIR bit.
- Select the activation source with bits DTF3 to DTF0.

[5] Read the DTE bit in DMABCRL as 0.

[6] Set each bit in DMABCRL.
- Specify enabling or disabling of transfer end interrupts with the DTIE bit.
- Set the DTE bit to 1 to enable transfer.

Figure 8.11 Example of Single Address Mode Setting Procedure (when Sequential Mode Is Specified)

Figure 8.13 shows an example of the setting procedure for normal mode.



[1] Set each bit in DMABCRH.
- Set the FAE bit to 1 to select full address mode.
- Specify enabling or disabling of internal interrupt clearing with the DTA bit.

[2] Set the transfer source address in MARA, and the transfer destination address in MARB.

[3] Set the number of transfers in ETCRA.

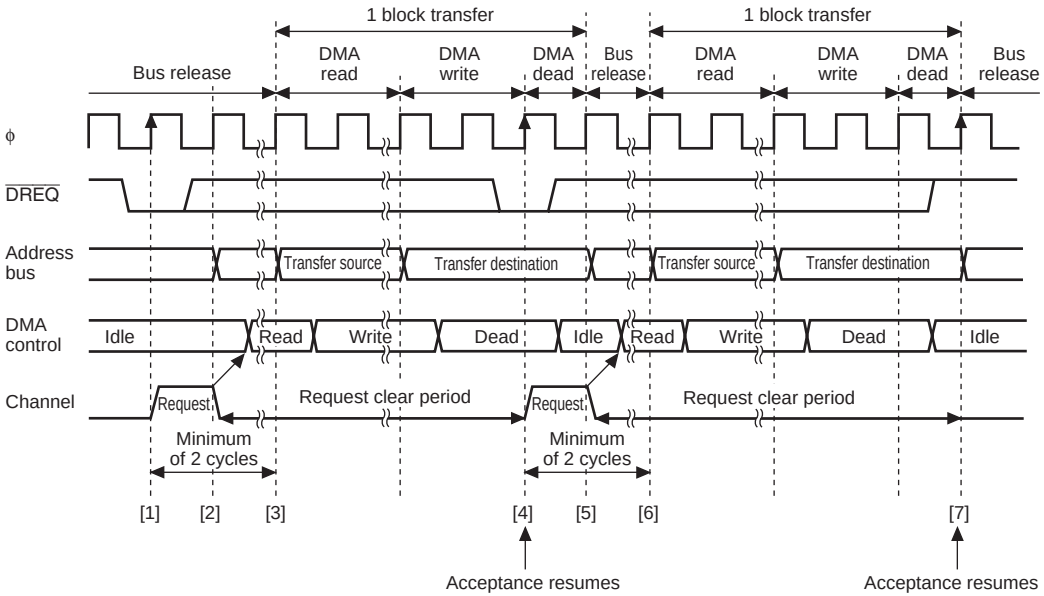
[4] Set each bit in DMACRA and DMACRB.
- Set the transfer data size with the DTSZ bit.
- Specify whether MARA is to be incremented, decremented, or fixed, with the SAID and SAIDE bits.
- Clear the BLKE bit to 0 to select normal mode.
- Specify whether MARB is to be incremented, decremented, or fixed, with the DAID and DAIDE bits.
- Select the activation source with bits DTF3 to DTF0.

[5] Read DTE = 0 and DTME = 0 in DMABCRL.

[6] Set each bit in DMABCRL.
- Specify enabling or disabling of transfer end interrupts with the DTIE bit.
- Set both the DTME bit and the DTE bit to 1 to enable transfer.

Figure 8.13 Example of Normal Mode Setting Procedure

Figure 8.26 shows an example of block transfer mode transfer activated by $\overline{\text{DREQ}}$ pin low level.



[1] Acceptance after transfer enabling; the $\overline{\text{DREQ}}$ pin low level is sampled on the rising edge of ϕ, and the request is held.
[2] [5] The request is cleared at the next bus break, and activation is started in the DMAC.
[3] [6] The DMA cycle is started.
[4] [7] Acceptance is resumed after the dead cycle is completed.
(As in [1], the $\overline{\text{DREQ}}$ pin low level is sampled on the rising edge of ϕ, and the request is held.)

Note: In write data buffer mode, bus breaks from [2] to [7] may be hidden, and not visible.

Figure 8.26 Example of $\overline{\text{DREQ}}$ Pin Low Level Activated Block Transfer Mode Transfer

$\overline{\text{DREQ}}$ pin sampling is performed every cycle, with the rising edge of the next ϕ cycle after the end of the DMABCR write cycle for setting the transfer enabled state as the starting point.

When the $\overline{\text{DREQ}}$ pin low level is sampled while acceptance by means of the $\overline{\text{DREQ}}$ pin is possible, the request is held in the DMAC. Then, when activation is initiated in the DMAC, the request is cleared. After the end of the dead cycle, acceptance resumes, $\overline{\text{DREQ}}$ pin low level sampling is performed again, and this operation is repeated until the transfer ends.

- P74/TMO2/$\overline{\text{MRES}}$

  The pin functions are switched as shown below according to the combination of OS3 to OS0 bits in TCSR_2 of TMR_2*, the MRESE bit in SYSCR, and the P74DDR bit.

MRESE	0			1
OS3 to OS0*	All bits are 0		Any bit is 1	—
P74DDR	0	1	—	0
Pin functions	P74 input pin	P74 output pin	TMO2* output	$\overline{\text{MRES}}$ input

Note: * Not available in the H8S/2237 Group and H8S/2227 Group.

- P73/TMO1/$\overline{\text{TEND1}}$/$\overline{\text{CS7}}$

  The pin functions are switched as shown below according to the combination of operating mode, the TEE1 bit in DMATCR of DMAC*, OS3 to OS0 bits in TCSR_1 of TMR_1, and the P73DDR bit.

Operating mode	Modes 4 to 6				Mode 7			
TEE1*	0			1	0			1
OS3 to OS0	All bits are 0		Any bit is 1	—	All bits are 0		Any bit is 1	—
P73DDR	0	1	—	—	0	1	—	—
Pin functions	P73 input pin	$\overline{\text{CS7}}$ output pin	TMO1 output pin	$\overline{\text{TEND1}}$* output pin	P73 input pin	P73 output pin	TMO1 output pin	$\overline{\text{TEND1}}$* output pin

Note: * Supported only by the H8S/2239 Group.

- P72/TMO0/$\overline{\text{TEND0}}$/$\overline{\text{CS6}}$

  The pin functions are switched as shown below according to the combination of operating mode the TEE0 bit in DMATCR of DMAC*, OS3 to OS0 bits in TCSR_0 of TMR_0, and the P72DDR bit.

Operating mode	Modes 4 to 6				Mode 7			
TEE0*	0			1	0			1
OS3 to OS0	All bits are 0		Any bit is 1	—	All bits are 0		Any bit is 1	—
P72DDR	0	1	—	—	—		—	—
Pin functions	P72 input pin	$\overline{\text{CS6}}$ output pin	TMO0 output pin	$\overline{\text{TEND0}}$* output pin	P72 input pin	P72 output pin	TMO0 output pin	$\overline{\text{TEND0}}$* output pin

Note: * Supported only by the H8S/2239 Group.

Table 11.25 TIORL_3

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_3 Function*2**	**TIOCC3 Pin Function*2**
0	0	0	0	Output compare register*1	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	0	0	0	Input capture register*1	Capture input source is TIOCC3 pin Input capture at rising edge
			1		Capture input source is TIOCC3 pin Input capture at falling edge
		1	×		Capture input source is TIOCC3 pin Input capture at both edges
	1	×	×		Capture input source is channel 4/count clock Input capture at TCNT_4 count-up/count-down

Legend: ×: Don't care

Notes: 1. When the BFA bit in TMDR_3 is set to 1 and TGRC_3 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

2. Not available in the H8S/2227 Group.

14.3.12 IEBus Receive Control Field Register (IERCTL)

IERCTL indicates the control field value in slave/broadcast reception. This register is enabled when slave/broadcast receive starts, and the contents are changed at the timing of setting the RxS flag in IERSR.

This register cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0.
3	RCTL3	0	R	IEBus Receive Control Field Indicate the control field value in slave/broadcast reception.
2	RCTL2	0	R	
1	RCTL1	0	R	
0	RCTL0	0	R	

14.3.13 IEBus Receive Message Length Register (IERBFL)

IERBFL indicates the message length field in slave/broadcast reception. This register is enabled when slave/broadcast receive starts, and the contents are changed at the timing of setting the RxS flag in IERSR.

This register cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	RBFL7	0	R	IEBus Receive Message Length Indicate the contents of message length field in slave/broadcast reception.
6	RBFL6	0	R	
5	RBFL5	0	R	
4	RBFL4	0	R	
3	RBFL3	0	R	
2	RBFL2	0	R	
1	RBFL1	0	R	
0	RBFL0	0	R	

15.3.10 Serial Expansion Mode Register (SEMR_0)

SEMR_0 is an 8-bit register that expands SCI_0 functions; such as setting of the base clock, selecting of the clock source, and automatic setting of the transfer rate.

Note: Supported only by the H8S/2239 Group only.

Bit	Bit Name	Initial Value	R/W	Description
7	SSE	0	R/W	SCI_0 Select Enable This bit enables or disables the SCI_0 select function when an external clock is input in clocked synchronous mode. When 1 is set to the PG1/$\overline{\text{IRQ7}}$ pin, while the SCI_0 select function is enabled, the TxD0 output becomes Hi-Z and the SCK0 input in this LSI is fixed high making the SCI_0 data transfer terminated. The SSE setting is valid when the external clock input is selected (CKE in SCR = 0) in clocked synchronous mode (C/$\overline{\text{A}}$ in SMR = 1). 0: SCI_0 select is disabled. 1: SCI_0 select is enabled. When then PG1/$\overline{\text{IRQ7}}$ pin = 1, the TxD0 output becomes Hi-Z and the SCK0 clock input is fixed high.
6 to 4	—	Undefined	—	Reserved These bits are always read as 0, and cannot be modified.
3	ABCS	0	R/W	Asynchronous Base Clock Select Selects the 1-bit-interval base clock in asynchronous mode. The ABCS setting is valid in asynchronous mode (C/$\overline{\text{A}}$ in SMR = 0). 0: Operates on a base clock with a frequency of 16 times the transfer rate. 1: Operates on a base clock with a frequency of 8 times the transfer rate.

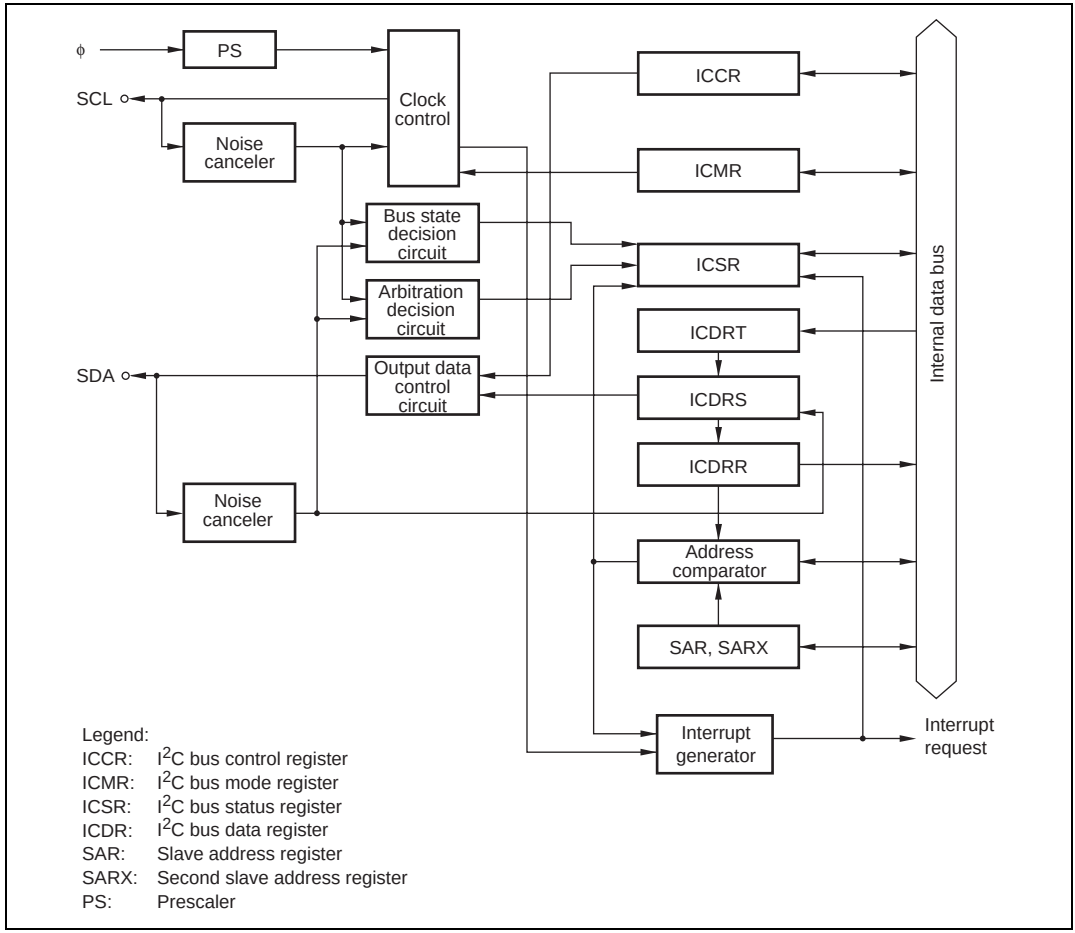


Figure 16.1 Block Diagram of I²C Bus Interface

Bit	Bit Name	Initial Value	R/W	Description
3	ACKE	0	R/W	Acknowledge Bit Judgement Selection 0: The value of the acknowledge bit is ignored, and continuous transfer is performed. The value of the received acknowledge bit is not indicated by the ACKB bit, which is always 0. 1: If the acknowledge bit is 1, continuous transfer is interrupted. In this LSI, the DTC can be used to perform continuous transfer. The DTC is activated when the IRTR interrupt flag is set to 1 (IRTR us one of two interrupt flags, the other being IRIC). When the ACKE bit is 0, the TDRE, IRIC, and IRTR flags are set on completion of data transmission, regardless of the acknowledge bit. When the ACKE bit is 1, the TDRE, IRIC, and IRTR flags are set on completion of data transmission when the acknowledge bit is 0, and the IRIC flag alone is set on completion of data transmission when the acknowledge bit is 1. When the DTC is activated, the TDRE, IRIC, and IRTR flags are cleared to 0 after the specified number of data transfers have been executed. Consequently, interrupts are not generated during continuos data transfer, but if data transmission is completed with a 1 acknowledge bit when the ACKE bit is set to 1, the DTC is not activated and an interrupt is generated, if enabled. Depending on the receiving device, the acknowledge bit may be significant, in indicating completion of processing of the received data, for instance, or may be fixed at 1 and have no significance.
2	BBSY	0	R/W	Bus Busy In slave mode, reading the BBSY flag enables to confirm whether the I²C bus is occupied or released. The BBSY flag is set to 0 when the SDA level changes from high to low under the condition of SCl = high, assuming that the start condition has been issued. The BBSY flag is cleared to 0 when the SDA level changes from low to high under the condition of SCl = high, assuming that the start condition has been issued. Writing to the BBSY flag in slave mode is disabled. In master mode, the BBSY flag is used to issue start and stop conditions. Write 1 to BBSY and 0 to SCP to issue a start condition. Follow this procedure when also re-transmitting a start condition. To issue a start/stop condition, use the MOV instruction. The I²C bus interface must be set in master transmit mode before the issue of a start condition.

The reception procedure and operations in slave receive mode are described below.

[1] Set the ICE bit in ICCR to 1. Set the MLS bit in ICMR and the MST and TRS bits in ICCR according to the operating mode.

[2] When the start condition output by the master device is detected, the BBSY flag in ICCR is set to 1.

[3] When the slave address matches in the first frame following the start condition, the device operates as the slave device specified by the master device. If the 8th data bit (R/$\overline{W}$) is 0, the TRS bit in ICCR remains cleared to 0, and slave receive operation is performed.

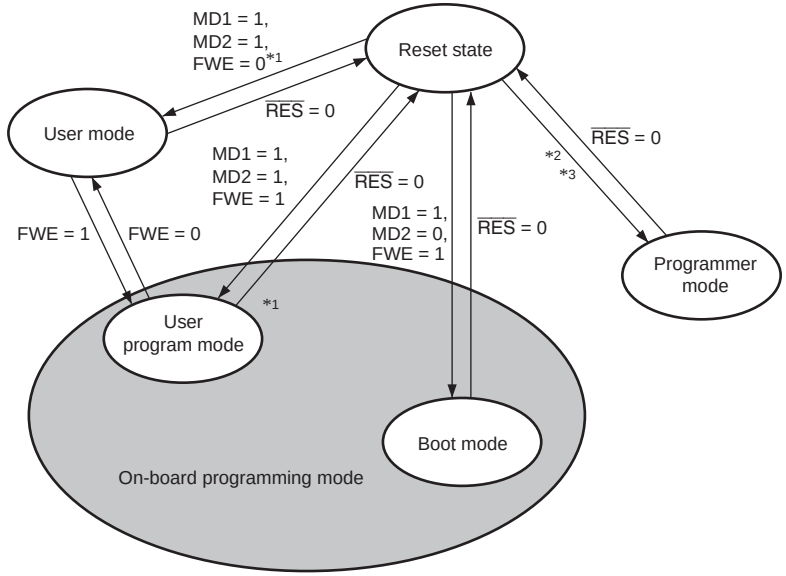
[4] At the 9th clock pulse of the receive frame, the slave device drives SDA low and returns an acknowledge signal. At the same time, the IRIC flag in ICCR is set to 1. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU. If the RDRF internal flag has been cleared to 0, it is set to 1, and the receive operation continues. If the RDRF internal flag has been set to 1, the slave device drives SCL low from the fall of the receive clock until data is read into ICDR.

[5] Read ICDR and clear the IRIC flag in ICCR to 0. The RDRF flag is cleared to 0. Read the IRDR flag and clear the IRIC flag to 0 consecutively, with no interrupt processing occurring between them. If the time needed to transmit one byte of data elapses before the IRIC flag is cleared, it will not be possible to determine when the transfer has completed.

Receive operations can be performed continuously by repeating steps [4] and [5]. When SDA is changed from low to high when SCL is high, and the stop condition is detected, the BBSY flag in ICCR is cleared to 0.

The differences between boot mode and user program mode are shown in table 20.1.

Figure 20.3 shows the operation flow for boot mode and figure 20.4 shows that for user program mode.



Notes: Only make a transition between user mode and user program mode when the CPU is not accessing the flash memory.

1. RAM emulation possible
2. In the H8S/2258, H8S/2239, H8S/2238B, and H8S/2238R, MD0 = 0, MD1 = 0, MD2 = 0, P14 = 0, P16 = 0, PF0 = 1.
3. In the H8S/2227 Group, MD0 = 0, MD1 = 0, MD2 = 0, P14 = 0, P16 = 0, PF0 = 1, PF3 = 1.

Figure 20.2 Flash Memory State Transitions

Table 20.1 Differences between Boot Mode and User Program Mode

	Boot Mode	User Program Mode
Total erase	Yes	Yes
Block erase	No	Yes
Programming control program*	Program/program-verify	Program/program-verify/erase/ erase-verify/emulation

Note: * To be provided by the user, in accordance with the recommended algorithm.

20.8.2 Erase/Erase-Verify

When erasing flash memory, the erase/erase-verify flowchart shown in figure 20.12 should be followed.

1. Prewriting (setting erase block data to all 0) is not necessary.
2. Erasing is performed in block units. Make only a single-bit specification in the erase block register 1 and 2 (EBR1 and EBR2). To erase multiple blocks, each block must be erased in turn.
3. The time during which the E1 bit is set to 1 is the flash memory erase time.
4. The watchdog timer (WDT) is set to prevent overprogramming due to program runaway, etc. Set a value greater than ($t_{sesu} + t_{se} + t_{ce} + t_{cesu}$) ms as the WDT overflow period.
5. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower 1 bit are B'0. Verify data can be read in words from the address to which a dummy write was performed.
5. If the read data is not erased successfully, set erase mode again, and repeat the erase/erase-verify sequence as before. The maximum number of repetitions of the erase/erase-verify sequence is (N).

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TGRD_3	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	TPU_3
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR_4	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU_4
TMDR_4	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_4	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_4	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_4	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_4	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRA_4	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRB_4	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR_5	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU_5
TMDR_5	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_5	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_5	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_5	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_5	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRA_5	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRB_5	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TSTR	—	—	CST5	CST4	CST3	CST2	CST1	CST0	TPU
TSYR	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	
IPRA	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	INT
IPRB	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRC	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRD	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRE	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TSR_0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA	TPU_0
TCNT_0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRA_0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRB_0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRC_0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRD_0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR_1	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU_1
TMDR_1	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_1	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_1	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_1	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_1	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRA_1	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRB_1	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR_2	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU_2
TMDR_2	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_2	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_2	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_2	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_2	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRA_2	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Register Name	Reset	Manual Reset	High-speed	Medium-speed	Sleep	Module Stop	Watch	Sub-active	Sub-sleep	Software Standby	Hardware Standby	Module
IPRA	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	INT
IPRB	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRC	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRD	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRE	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRF	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRG	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRH	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRI	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRJ	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRK	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRL	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
IPRO	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
ABWCR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	BSC
ASTCR	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
WCRH	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
WCRL	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
BCRH	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
BCRL	Initialized	—	—	—	—	—	—	—	—	—	Initialized	
RAMER	Initialized	—	—	—	—	—	—	—	—	—	Initialized	FLASH
MAR_0A	—	—	—	—	—	—	—	—	—	—	—	DMAC
IOAR_0A	—	—	—	—	—	—	—	—	—	—	—	
ETCR_0A	—	—	—	—	—	—	—	—	—	—	—	
MAR_0B	—	—	—	—	—	—	—	—	—	—	—	
IOAR_0B	—	—	—	—	—	—	—	—	—	—	—	
ETCR_0B	—	—	—	—	—	—	—	—	—	—	—	
MAR_1A	—	—	—	—	—	—	—	—	—	—	—	
IOAR_1A	—	—	—	—	—	—	—	—	—	—	—	
ETCR_1A	—	—	—	—	—	—	—	—	—	—	—	
MAR_1B	—	—	—	—	—	—	—	—	—	—	—	
IOAR_1B	—	—	—	—	—	—	—	—	—	—	—	
ETCR_1B	—	—	—	—	—	—	—	—	—	—	—	

Table 27.15 Permissible Output Currents

Condition A (F-ZTAT version): V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications)

Condition B (Masked ROM version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V, V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications) T_a = –40°C to +85°C (wide-range specifications)

Condition C (F-ZTAT version): V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	SCL1, SCL0, SDA1, SDA0	V_{CC} = 2.7 V to 3.6 V	I_{OL}	—	—	10	mA
	Output pins other than above ones	V_{CC} = 2.2 V to 3.6 V	I_{OL}	—	—	0.5	
		V_{CC} = 2.7 V to 3.6 V		—	—	1.0	
Permissible output low current (total)	Total of all output pins	V_{CC} = 2.2 V to 3.6 V	$\sum I_{OL}$	—	—	30	mA
		V_{CC} = 2.7 V to 3.6 V		—	—	60	
Permissible output high current (per pin)	All output pins	V_{CC} = 2.2 V to 3.6 V	$-I_{OH}$	—	—	0.5	mA
		V_{CC} = 2.7 V to 3.6 V		—	—	1.0	
Permissible output high current (total)	Total of all output pins	V_{CC} = 2.2 V to 3.6 V	$\sum -I_{OH}$	—	—	15	mA
		V_{CC} = 2.7 V to 3.6 V		—	—	30	

Note: To protect chip reliability, do not exceed the output current values in table 27.15.

Table 27.39 DC Characteristics (2)

Condition A (F-ZTAT version): V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V,
V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20°C to +75°C (regular specifications)
T_a = –40°C to +85°C (wide-range specifications)*1

Condition B (F-ZTAT version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V,
V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20°C to +75°C (regular specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25 °C
	NMI		—	—	30	pF	
	P32 to P35		—	—	20	pF	
	All input pins other than above ones		—	—	15	pF	
Current consumption*2	Normal operation	I_{CC}*4	—	20 V_{CC} = 3.0 V	37 V_{CC} = 3.6 V	mA	f = 13.5 MHz
			—	10 V_{CC} = 3.0 V	18 V_{CC} = 3.6 V	mA	f = 6.25 MHz
	Sleep mode		—	15 V_{CC} = 3.0 V	29 V_{CC} = 3.6 V	mA	f = 13.5 MHz
			—	7.5 V_{CC} = 3.0 V	14 V_{CC} = 3.6 V	mA	f = 6.25 MHz
	All modules stopped		—	15	—	mA	f = 13.5 MHz, V_{CC} = 3.0 V (reference value)
	Medium-speed mode (ϕ/32)		—	13	—	mA	f = 13.5 MHz, V_{CC} = 3.0 V (reference value)
	Subactive mode		—	70	180	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used
	Subsleep mode		—	50	130	µA	V_{CC} = 3.0 V, When 32.768 kHz crystal resonator is used