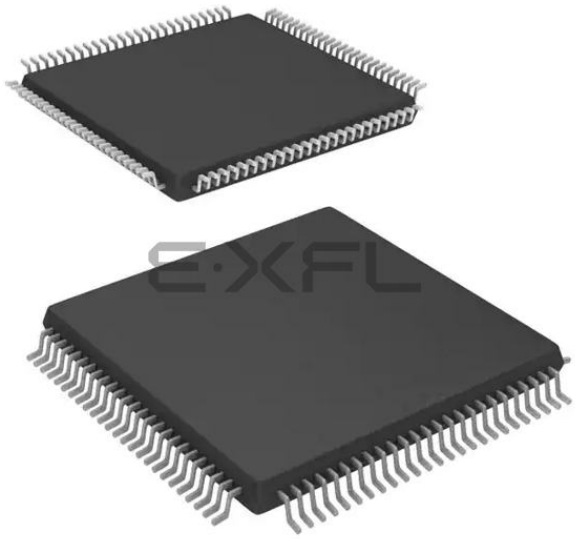

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2239te16v

4.8 Usage Note

When accessing word data or longword data, this LSI assumes that the lowest address bit is 0. The stack should always be accessed by word transfer instruction or longword transfer instruction, and the value of the stack pointer (SP, ER7) should always be kept even. Use the following instructions to save registers:

```
PUSH.W   Rn    (or MOV.W Rn, @-SP)
PUSH.L   ERn   (or MOV.L ERn, @-SP)
```

Use the following instructions to restore registers:

```
POP.W    Rn    (or MOV.W @SP+, Rn)
POP.L    ERn   (or MOV.L @SP+, ERn)
```

Setting SP to an odd value may lead to a malfunction. Figure 4.3 shows an example of what happens when the SP value is odd.

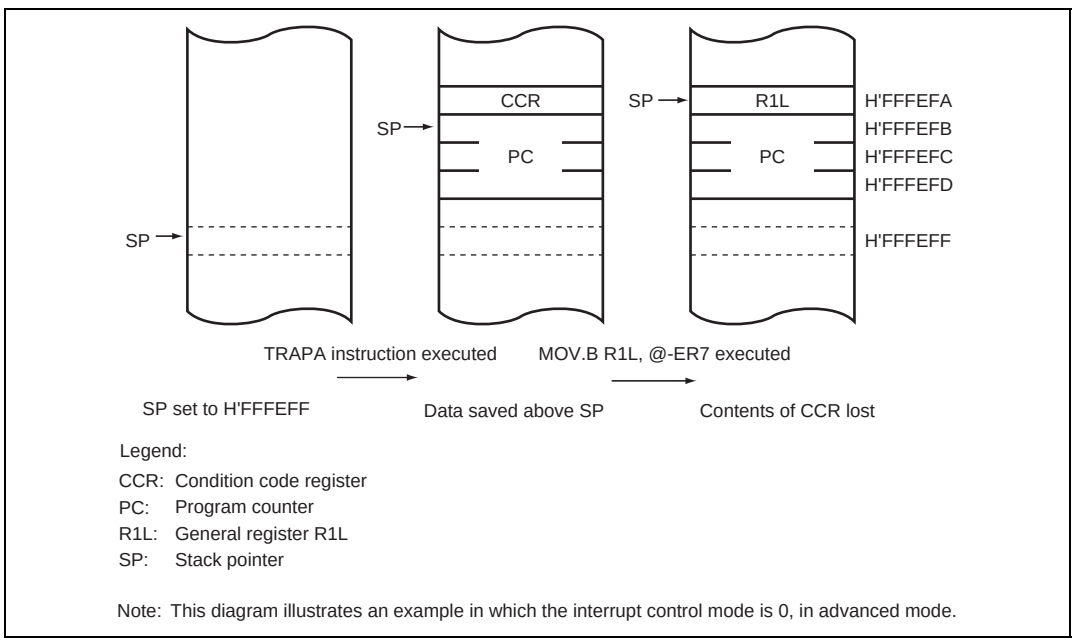
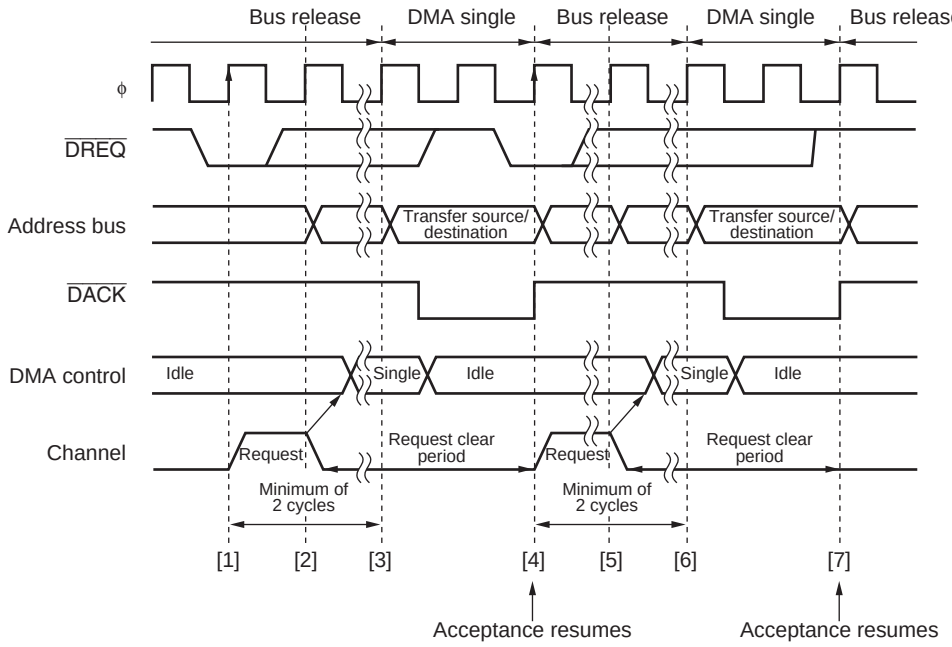


Figure 4.3 Operation When SP Value Is Odd

Figure 8.31 shows an example of single address mode transfer activated by the $\overline{\text{DREQ}}$ pin falling edge.



[1] Acceptance after transfer enabling; the $\overline{\text{DREQ}}$ pin low level is sampled on the rising edge of φ, and the request is held.

[2] [5] The request is cleared at the next bus break, and activation is started in the DMAC.

[3] [6] Start of DMA cycle; $\overline{\text{DREQ}}$ pin high level sampling on the rising edge of φ starts.

[4] [7] When the $\overline{\text{DREQ}}$ pin high level has been sampled, acceptance is resumed after the single cycle is completed. (As in [1], the $\overline{\text{DREQ}}$ pin low level is sampled on the rising edge of φ, and the request is held.)

Note: In write data buffer mode, bus breaks from [2] to [7] may be hidden, and not visible.

Figure 8.31 Example of $\overline{\text{DREQ}}$ Pin Falling Edge Activated Single Address Mode Transfer

$\overline{\text{DREQ}}$ pin sampling is performed every cycle, with the rising edge of the next φ cycle after the end of the DMABCR write cycle for setting the transfer enabled state as the starting point.

When the $\overline{\text{DREQ}}$ pin low level is sampled while acceptance by means of the $\overline{\text{DREQ}}$ pin is possible, the request is held in the DMAC. Then, when activation is initiated in the DMAC, the request is cleared, and $\overline{\text{DREQ}}$ pin high level sampling for edge detection is started. If $\overline{\text{DREQ}}$ pin high level sampling has been completed by the time the DMA single cycle ends, acceptance

- DTC enable registers A to G, and I (DTCERA to DTCERG, and DTCERI)
- DTC vector register (DTVECR)

9.2.1 DTC Mode Register A (MRA)

MRA selects the DTC operating mode.

Bit	Bit Name	Initial Value	R/W	Description
7	SM1	Undefined	—	Source Address Mode 1 and 0
6	SM0	Undefined	—	These bits specify an SAR operation after a data transfer. 0×: SAR is fixed 10: SAR is incremented after a transfer (by +1 when Sz = 0; by +2 when Sz = 1) 11: SAR is decremented after a transfer (by –1 when Sz = 0; by –2 when Sz = 1)
5	DM1	Undefined	—	Destination Address Mode 1 and 0
4	DM0	Undefined	—	These bits specify a DAR operation after a data transfer. 0×: DAR is fixed 10: DAR is incremented after a transfer (by +1 when Sz = 0; by +2 when Sz = 1) 11: DAR is decremented after a transfer (by –1 when Sz = 0; by –2 when Sz = 1)
3	MD1	Undefined	—	DTC Mode 1 and 0
2	MD0	Undefined	—	These bits specify the DTC transfer mode. 00: Normal mode 01: Repeat mode 10: Block transfer mode 11: Setting prohibited
1	DTS	Undefined	—	DTC Transfer Mode Select Specifies whether the source side or the destination side is set to be a repeat area or block area, in repeat mode or block transfer mode. 0: Destination side is repeat area or block area 1: Source side is repeat area or block area

10.4 Port 7

Port 7 is an 8-bit I/O port and has the following registers.

- Port 7 data direction register (P7DDR)
- Port 7 data register (P7DR)
- Port 7 register (PORT7)

10.4.1 Port 7 Data Direction Register (P7DDR)

P7DDR specifies input or output of the port 7 pins using the individual bits. P7DDR cannot be read; if it is, an undefined value will be read. This register is a write-only register, and cannot be written by bit manipulation instruction. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7	P77DDR	0	W	When a pin is specified as a general purpose I/O port, setting this bit to 1 makes the corresponding port 7 pin an output pin. Clearing this bit to 0 makes the pin an input pin.
6	P76DDR	0	W	
5	P75DDR	0	W	
4	P74DDR	0	W	
3	P73DDR	0	W	
2	P72DDR	0	W	
1	P71DDR	0	W	
0	P70DDR	0	W	

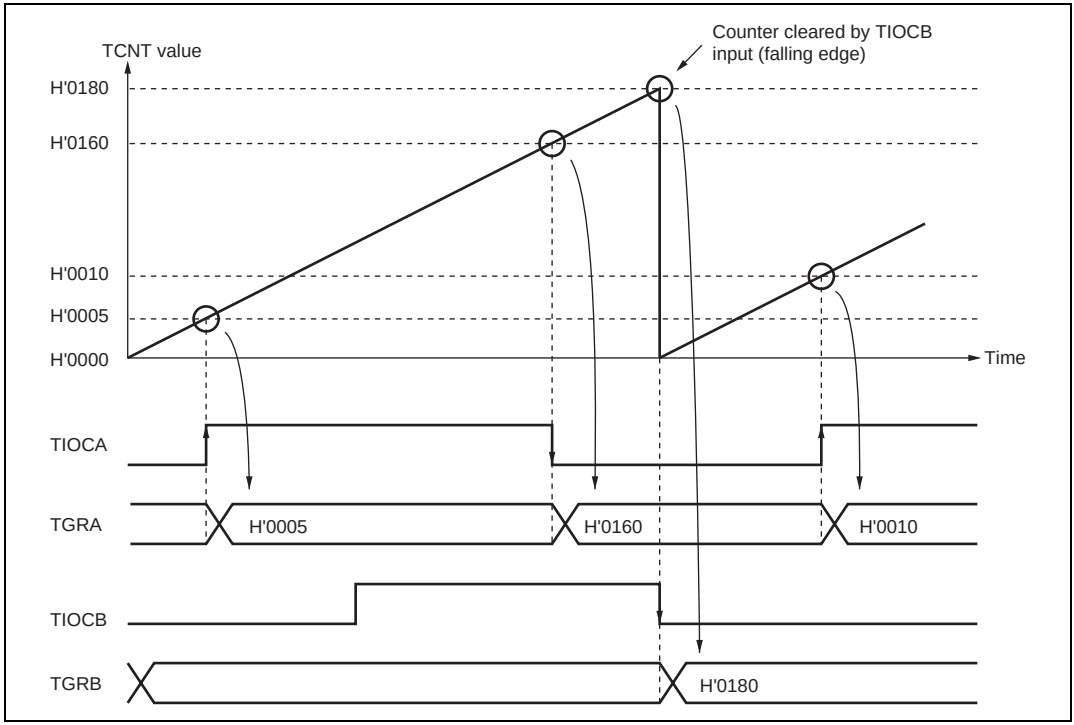


Figure 11.10 Example of Input Capture Operation

11.4.2 Synchronous Operation

In synchronous operation, the values in multiple TCNT counters can be rewritten simultaneously (synchronous presetting). Also, multiple of TCNT counters can be cleared simultaneously (synchronous clearing) by making the appropriate setting in TCR.

Synchronous operation enables TGR to be incremented with respect to a single time base.

Channels 0 to 2 (H8S/2227 Group) or 0 to 5 (groups other than H8S/2227) can all be designated for synchronous operation.

Example of Synchronous Operation Setting Procedure: Figure 11.11 shows an example of the synchronous operation setting procedure.

Figure 11.24 shows examples of PWM waveform output with 0% duty cycle and 100% duty cycle in PWM mode.

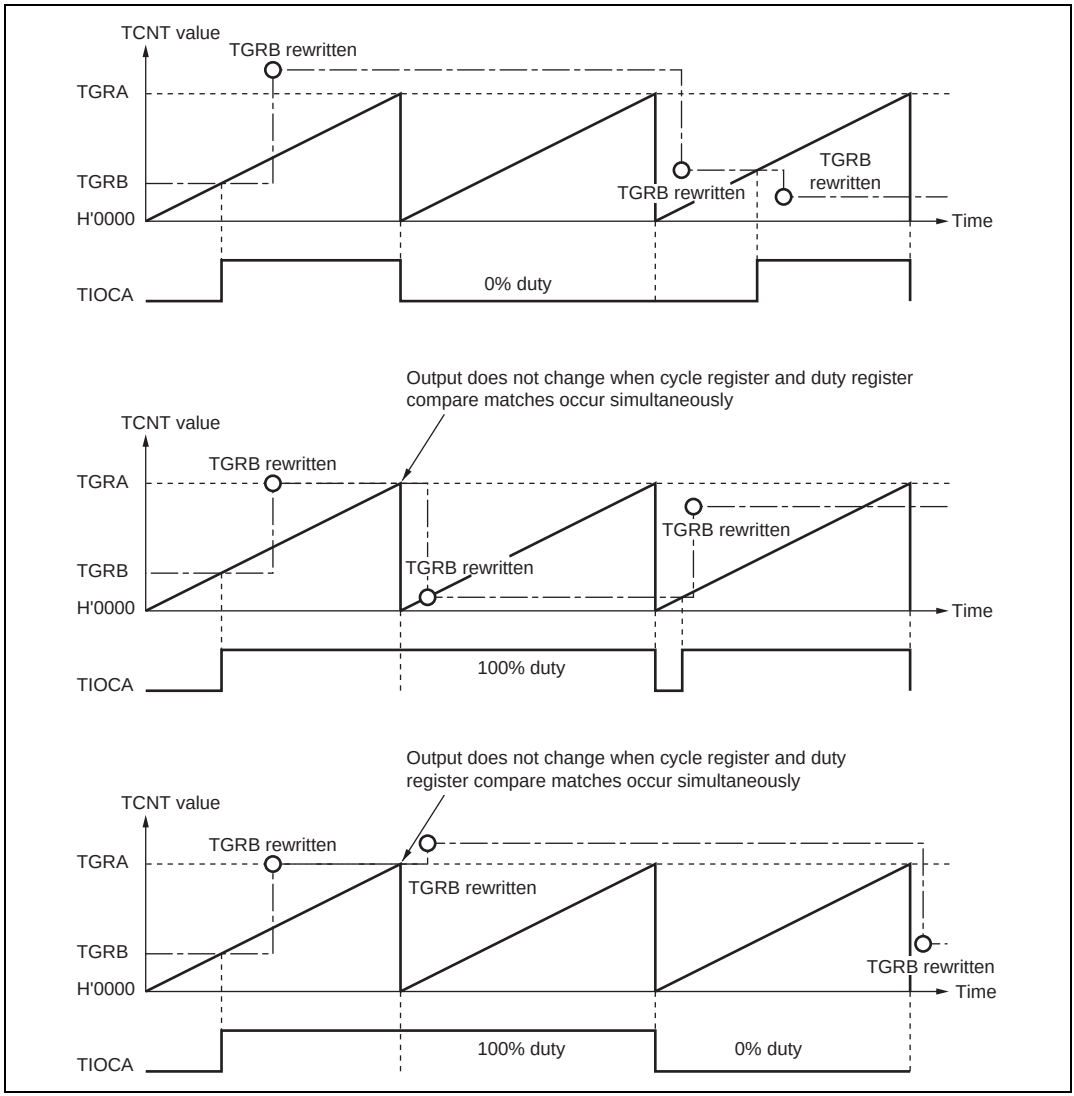


Figure 11.24 Example of PWM Mode Operation (3)

Bit	Bit Name	Initial Value	R/W	Description
3	OS3	0	R/W	Output Select 3 and 2
2	OS2	0	R/W	These bits specify how the timer output level is to be changed by a compare-match B of TCORB and TCNT. 00: No change when compare-match B occurs 01: 0 is output when compare-match B occurs 10: 1 is output when compare-match B occurs 11: Output is inverted when compare-match B occurs (toggle output)
1	OS1	0	R/W	Output Select 1 and 0
0	OS0	0	R/W	These bits specify how the timer output level is to be changed by a compare-match A of TCORA and TCNT. 00: No change when compare-match A occurs 01: 0 is output when compare-match A occurs 10: 1 is output when compare-match A occurs 11: Output is inverted when compare-match A occurs (toggle output)

Notes: 1. Not available in the H8S/2237 Group and H8S/2227 Group.
2. Only 0 can be written to this bit, to clear the flag.

14.3.7 IEBus Slave Address Setting Register 2 (IESA2)

IESA2 sets the upper 8 bits of the communications destination slave unit address. For slave communications, it is not necessary to set this register.

Bit	Bit Name	Initial Value	R/W	Description
7	ISA11	0	R/W	Upper 8 Bits of IEBus Slave Address
6	ISA10	0	R/W	Set upper 8 bits of the communications destination slave unit address
5	ISA9	0	R/W	
4	ISA8	0	R/W	
3	ISA7	0	R/W	
2	ISA6	0	R/W	
1	ISA5	0	R/W	
0	ISA4	0	R/W	

14.3.8 IEBus Transmit Message Length Register (IETBFL)

IETBFL sets the message length for master or slave transmission.

Bit	Bit Name	Initial Value	R/W	Description
7	TBFL7	0	R/W	Transmit Message Length
6	TBFL6	0	R/W	Set the message length for master or slave transmission.
5	TBFL5	0	R/W	
4	TBFL4	0	R/W	If a value exceeding the maximum transmit bytes for one frame is set in IETBFL, communications are performed with two or more frames in some communications modes. In this case, in or after the second frame, the message length value should be the number of bytes of the remaining communications data, however, the initial IETBFL setting remains unchanged. Therefore, for the second frame or after, re-set the number of bytes of the remaining communications data.
3	TBFL3	0	R/W	
2	TBFL2	0	R/W	
1	TBFL1	0	R/W	
0	TBFL0	0	R/W	

15.3.4 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first transfers transmit data from TDR to TSR, then sends the data to the TxD pin. TSR cannot be directly accessed by the CPU.

15.3.5 Serial Mode Register (SMR)

SMR is used to set the SCI's serial transfer format and select the baud rate generator clock source.

Some bit functions of SMR differ between normal serial communication interface mode and Smart Card interface mode.

- Normal Serial Communication Interface Mode (When SMIF in SCMR is 0)

Bit	Bit Name	Initial Value	R/W	Description
7	C/$\overline{A}$	0	R/W	Communication Mode 0: Asynchronous mode 1: Clocked synchronous mode
6	CHR	0	R/W	Character Length (enabled only in asynchronous mode) 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length. LSB-first is fixed and the MSB (bit 7) of TDR is not transmitted in transmission. In clocked synchronous mode, a fixed data length of 8 bits is used.
5	PE	0	R/W	Parity Enable (enabled only in asynchronous mode) When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception. For a multiprocessor format, parity bit addition and checking are not performed regardless of the PE bit setting.

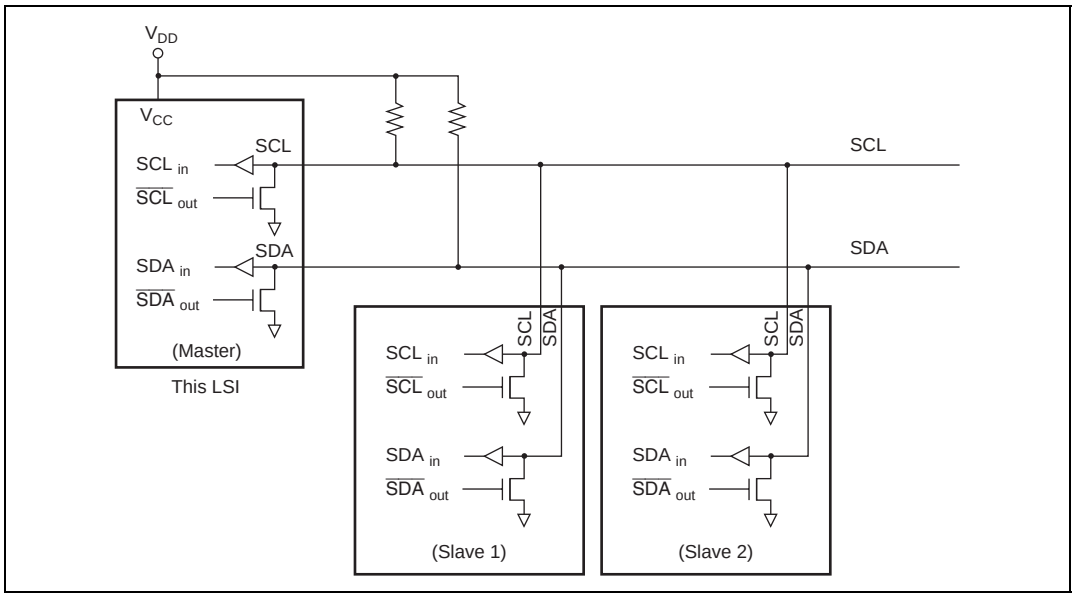


Figure 16.2 I²C Bus Interface Connections (Example: This LSI as Master)

16.2 Input/Output Pins

Table 16.1 shows the pin configuration for the I²C bus interface.

Table 16.1 Pin Configuration

Name	Abbreviation*	I/O	Function
Serial clock	SCL0	I/O	IIC_0 serial clock input/output
Serial data	SDA0	I/O	IIC_0 serial data input/output
Serial clock	SCL1	I/O	IIC_1 serial clock input/output
Serial data	SDA1	I/O	IIC_1 serial data input/output

Note: * Pin names SCL and SDA are used in the text for all channels, omitting the channel designation.

16.3 Register Descriptions

The I²C bus interface has the following registers. Registers ICDR and SARX and registers ICMR and SAR are allocated to the same addresses. Accessible addresses differ depending on the ICE bit in ICCR. SAR and SARX are accessed when ICE is 0, and ICMR and ICDR are accessed when

Table 16.2 Transfer Format

SAR	SARX	
FS	**FSX**	**I²C Transfer Format**
0	0	SAR and SARX are used as the slave addresses with the I²C bus format.
0	1	Only SAR is used as the slave address with the I²C bus format.
1	0	Only SARX is used as the slave address with the I²C bus format.
1	1	Clock synchronous serial format (SAR and SARX are invalid)

16.3.4 I²C Bus Mode Register (ICMR)

ICMR sets the transfer format and transfer rate. It can only be accessed when the ICE bit in ICCR is 1.

Bit	Bit Name	Initial Value	R/W	Description
7	MLS	0	R/W	MSB-First/LSB-First Select 0: MSB-first 1: LSB-first Set this bit to 0 when the I²C bus format is used.
6	WAIT	0	R/W	Wait Insertion Bit This bit is valid only in master mode with the I²C bus format. When WAIT is set to 1, after the fall of the clock for the final data bit, the IRIC flag is set to 1 in ICCR, and a wait state begins (with SCL at the low level). When the IRIC flag is cleared to 0 in ICCR, the wait ends and the acknowledge bit is transferred. If WAIT is cleared to 0, data and acknowledge bits are transferred consecutively with no wait inserted. The IRIC flag in ICCR is set to 1 on completion of the acknowledge bit transfer, regardless of the WAIT setting.
5	CKS2	0	R/W	Serial Clock Select 2 to 0
4	CKS1	0	R/W	This bit is valid only in master mode.
3	CKS0	0	R/W	These bits select the required transfer rate, together with the IICX 1 and IICX0 bit in SCRX. Refer to table 16.3.

[1] Clear the TRS bit in ICCR to 0 to switch from transmit mode to receive mode. Clear the ACKB bit in ICSR to 0 (acknowledge data setting). Clear the IRIC flag to 0, then set the WAIT bit in ICMR to 1.

[2] When ICDR is read (dummy data read), reception is started, and the receive clock is output, and data received, in synchronization with the internal clock.

[3] The IRIC flag is set to 1 by the following two conditions. At that point, an interrupt request is issued to the CPU if the IEIC bit in ICCR is set to 1.

(1) The flag is set at the falling edge of the 8th clock cycle of the receive clock for 1 frame. SCL is automatically held low, in synchronization with the internal clock, until the IRIC flag is cleared.

(2) The flag is set at the rising edge of the 9th clock cycle of the receive clock for 1 frame. The IRTR flag is set to 1, indicating that reception of 1 frame of data has ended. The master device continues to output the receive clock for the receive data.

[4] Read the IRTR flag in ICSR. If the IRTR flag value is 0, the wait state is cancelled by clearing the IRIC flag as described in step [6] below. If the IRTR flag value is 1 and the next receive data is the final receive data, perform the end processing described in step [7] below.

[5] If the IRTR flag value is 1, read the ICDR receive data.

[6] Clear the IRIC flag to 0. The reading of the ICDR flag described in step [5] and the clearing of the IRIC flag to 0 should be performed consecutively, with no interrupt processing occurring between them. During wait operation, clear the IRIC flag to 0 when the value of counter BC2 to BC0 is 2 or greater. If the IRIC flag is cleared to 0 when the value of counter BC2 to BC0 is 1 or 0, it will not be possible to determine when the transfer has completed. If condition [3]-1 is true, the master device drives SDA to low level and returns an acknowledge signal when the receive clock outputs the 9th clock cycle.

Further data can be received by repeating steps [3] through [6].

[7] Set the ACKB bit in ICSR to 1 to set the acknowledge data for the final receive.

[8] Wait for at least 1 clock cycle after the IRIC flag is set to 1 and then wait for the rising edge of the 1st clock cycle of the next receive data.

[9] Set the TSR bit in ICCR to 1 to switch from the receive mode to the transmit mode. The TSR bit setting value at this point becomes valid when the rising edge of the next 9th clock cycle is input.

[10] Read the ICDR receive data.

[11] Clear the IRIC flag to 0. As in step [6], read the ICDR flag and clear the IRIC flag to 0 consecutively, with no interrupt processing occurring between them. During wait operation, clear the IRIC flag to 0 when the value of counter BC2 to BC0 is 2 or greater.

[12] The IRIC flag is set to 1 by the following two conditions.

The reception procedure and operations in slave receive mode are described below.

[1] Set the ICE bit in ICCR to 1. Set the MLS bit in ICMR and the MST and TRS bits in ICCR according to the operating mode.

[2] When the start condition output by the master device is detected, the BBSY flag in ICCR is set to 1.

[3] When the slave address matches in the first frame following the start condition, the device operates as the slave device specified by the master device. If the 8th data bit (R/$\overline{W}$) is 0, the TRS bit in ICCR remains cleared to 0, and slave receive operation is performed.

[4] At the 9th clock pulse of the receive frame, the slave device drives SDA low and returns an acknowledge signal. At the same time, the IRIC flag in ICCR is set to 1. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU. If the RDRF internal flag has been cleared to 0, it is set to 1, and the receive operation continues. If the RDRF internal flag has been set to 1, the slave device drives SCL low from the fall of the receive clock until data is read into ICDR.

[5] Read ICDR and clear the IRIC flag in ICCR to 0. The RDRF flag is cleared to 0. Read the IRDR flag and clear the IRIC flag to 0 consecutively, with no interrupt processing occurring between them. If the time needed to transmit one byte of data elapses before the IRIC flag is cleared, it will not be possible to determine when the transfer has completed.

Receive operations can be performed continuously by repeating steps [4] and [5]. When SDA is changed from low to high when SCL is high, and the stop condition is detected, the BBSY flag in ICCR is cleared to 0.

13. Notes on ICDR Reads in Transmit Mode and ICDR Writes in Receive Mode

When attempting to read ICDR in the transmit mode (TRS = 1) or write to ICDR in the receive mode (TRS = 0) under certain conditions, the SCL pin may not be held low after the completion of the transmit or receive operation and a clock may not be output to the SCL bus line before the ICDR register access operation can take place properly.

When accessing ICDR, always change the setting to the transmit mode before performing a read operation, and always change the setting to the receive mode before performing a write operation.

14. Notes on ACKE Bit and TRS Bit in Slave Mode

When using the I²C bus interface, if an address is received in the slave mode immediately after 1 is received as an acknowledge bit (ACKB = 1) in the transmit mode (TRS = 1), an interrupt may be generated at the rising edge of the 9th clock cycle if the address does not match.

When performing slave mode operations using the IIC bus interface module, make sure to do the following.

(1) When a 1 is received as an acknowledge bit for the final transmit data after completing a series of transmit operations, clear the ACKE bit in the ICCR register to 0 to initialize the ACKB bit to 0.

(2) In the slave mode, change the setting to the receive mode (TRS = 0) before the start condition is input. To ensure that the switch from the slave transmit mode to the slave receive mode is accomplished properly, end the transmission as described in figure 16.17.

15. Notes on Arbitration Lost in Master Mode

The I²C bus interface recognizes the data in transmit/receive frame as an address when arbitration is lost in master mode and a transition to slave receive mode is automatically carried out.

When arbitration is lost not in the first frame but in the second frame or subsequent frame, transmit/receive data that is not an address is compared with the value set in the SAR or SARX register as an address. If the receive data matches with the address in the SAR or SARX register, the I²C bus interface erroneously recognizes that the address call has occurred. (See figure 16.27.)

In multi-master mode, a bus conflict could happen. When The I²C bus interface is operated in master mode, check the state of the AL bit in the ICSR register every time after one frame of data has been transmitted or received.

When arbitration is lost during transmitting the second frame or subsequent frame, take avoidance measures.

20.9 Program/Erase Protection

There are three kinds of flash memory program/erase protection; hardware protection, software protection, and error protection.

20.9.1 Hardware Protection

Hardware protection refers to a state in which programming/erasing of flash memory is forcibly disabled or aborted because of a transition to reset or standby mode. Flash memory control register 1 (FLMCR1), flash memory control register 2 (FLMCR2), erase block register 1 (EBR1), and erase block register 2 (EBR2) are initialized. In a reset via the $\overline{\text{RES}}$ pin, the reset state is not entered unless the $\overline{\text{RES}}$ pin is held low until oscillation stabilizes after powering on. In the case of a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width specified in the AC Characteristics section.

20.9.2 Software Protection

Software protection can be implemented against programming/erasing of all flash memory blocks by clearing the SWE1 bit in FLMCR1. When software protection is in effect, setting the P1 or E1 bit in FLMCR1 does not cause a transition to program mode or erase mode. By setting the erase block register 1 and 2 (EBR1 and EBR2), erase protection can be set for individual blocks. When EBR1 and EBR2 are set to H'00, erase protection is set for all blocks. By setting bit RAMS in RAMER, programming/erase protection is set for all blocks.

20.9.3 Error Protection

In error protection, an error is detected when CPU runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the program/erase algorithm, and the program/erase operation is aborted. Aborting the program/erase operation prevents damage to the flash memory due to overprogramming or overerasing.

When the following errors are detected during programming/erasing of flash memory, the FLER bit in FLMCR2 is set to 1, and the error protection state is entered.

- When the flash memory of the relevant address area is read during programming/erasing (including vector read and instruction fetch)
- Immediately after exception handling (excluding a reset) during programming/erasing
- When a SLEEP instruction is executed during programming/erasing
- When the CPU releases the bus to the DMAC* or DTC during programming/erasing

Note: * Supported only by the H8S/2239 Group.

27.2.2 DC Characteristics

Table 27.2 lists the DC characteristics. Table 27.3 lists the permissible output currents. Table 27.4 lists the bus driving characteristics.

Table 27.2 DC Characteristics (1)

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{ref} = 4.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)*1

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	$\overline{IRQ0}$ to $\overline{IRQ7}$	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.8$	V	
		$VT^+ - VT^-$	$V_{CC} \times 0.05$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0, FWE	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL, Ports 1, 3, 7, and A to G		$V_{CC} \times 0.8$	—	V_{CC} + 0.3	V	
	Ports 4 and 9		$V_{CC} \times 0.8$	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0, FWE	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, Ports 1, 3, 4, 7, 9, and A to G		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins*3 except P34 and P35	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
	P34 and P35*2		V_{CC} – 2.7	—	—	V	I_{OH} = –100 µA
Output low voltage	All output pins*3	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA
			—	—	0.4	V	I_{OL} = 0.8 mA

Table 27.16 Bus Driving Characteristics

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)*,
Objective pins: SCL1, SCL0, SDA1, SDA0

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	VT^-	$V_{CC} \times 0.3$	—	—	V	V_{CC} = 2.7 V to 3.6 V
	VT^+	—	—	$V_{CC} \times 0.7$	V	V_{CC} = 2.7 V to 3.6 V
	$VT^+ - VT^-$	$V_{CC} \times 0.05$	—	—	V	V_{CC} = 2.7 V to 3.6 V
Input high voltage	V_{IH}	$V_{CC} \times 0.7$	—	V_{CC} + 0.5	V	V_{CC} = 2.7 V to 3.6 V
Input low voltage	V_{IL}	–0.5	—	$V_{CC} \times 0.3$	V	V_{CC} = 2.7 V to 3.6 V
Output low voltage	V_{OL}	—	—	0.5	V	I_{OL} = 6 mA, V_{CC} = 3.0 V to 3.6 V
		—	—	0.4	V	I_{OL} = 3 mA
Input capacitance	C_{in}	—	—	20	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
Three states leakage current (off)	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
SCL, SDA output falling time	t_{of}	20 + 0.1 Cb	—	250	ns	V_{CC} = 2.7 V to 3.6 V

Note: * If the A/D or D/A converter is not used, the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Even if the A/D or D/A converter is not used, connect the AV_{CC} and V_{ref} pins to V_{CC} and supply 2.0 V to 3.6 V. In this case, $V_{ref} \leq AV_{CC}$.

27.3.4 A/D Conversion Characteristics

Table 27.23 lists the A/D conversion characteristics.

Table 27.23 A/D Conversion Characteristics

Condition A (F-ZTAT version and masked ROM version):
V_{CC} = 2.7 V to 3.6 V*, AV_{CC} = 2.7 V to 3.6 V*,
V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 16.0 MHz,
T_a = –20°C to +75°C (regular specifications)

Condition B (Masked ROM version): V_{CC} = 2.2 V to 3.6 V*, AV_{CC} = 2.2 V to 3.6 V*,
V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 6.25 MHz,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Condition C (F-ZTAT version and masked ROM version):
V_{CC} = 3.0 V to 3.6 V*, AV_{CC} = 3.0 V to 3.6 V*,
V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ϕ = 10.0 to 20.0 MHz,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

	Conditions A, C			Condition B			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	bits
Conversion time	8.1	—	—	20.9	—	—	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	5	—	—	5	kΩ
Nonlinearity error	—	—	±6.0	—	—	±6.0	LSB
Offset error	—	—	±4.0	—	—	±4.0	LSB
Full-scale error	—	—	±4.0	—	—	±4.0	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	—	—	±8.0	LSB

Note: * AN0 and AN1 can be used only when V_{CC} = AV_{CC}.

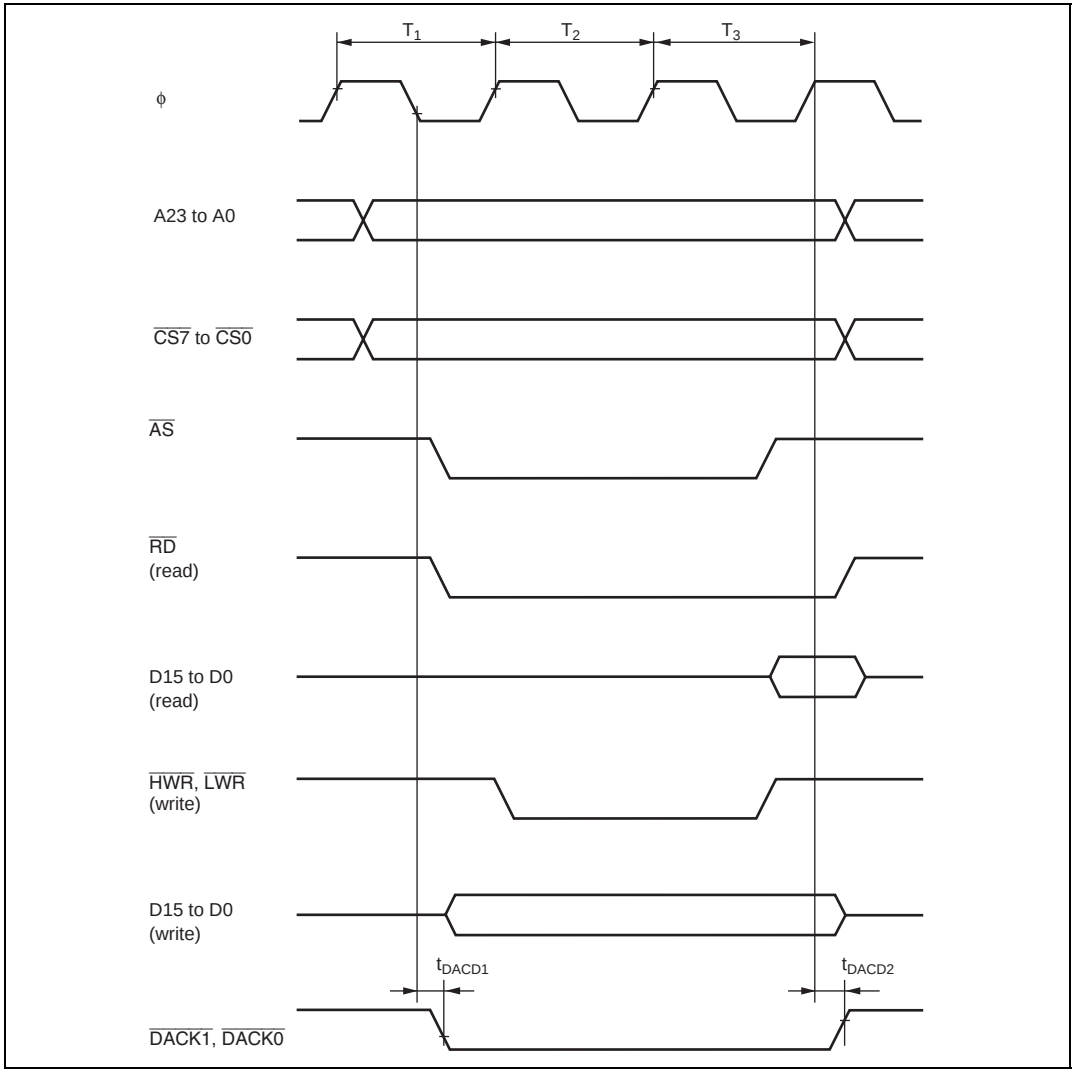


Figure 27.21 DMAC Single Address Transfer Timing (Three-State Access)