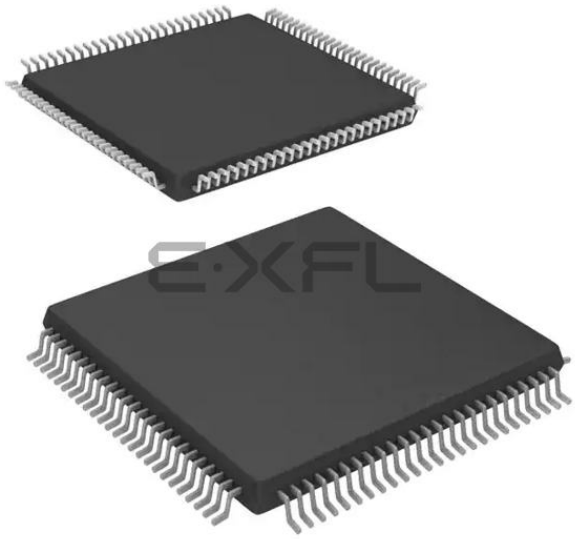

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

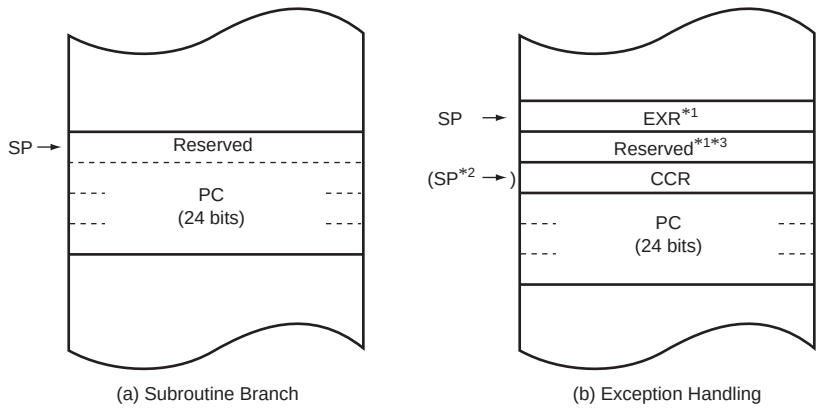
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2239te20v

Type	Symbol	Pin No. TFP-100B TFP-100BV FP-100B FP-100BV	Pin No. FP-100A FP-100AV	I/O	Function
16-bit timer-pulse unit (TPU)	TIOCA3 TIOCB3 TIOCC3 TIOCD3	22 23 24 25	25 26 27 28	Input/ Output	Pins for the TGRA_3 to TGRD_3 input capture input, output compare output, or PWM output.
	TIOCA4 TIOCB4	26 27	29 30	Input/ Output	Pins for the TGRA_4 and TGRB_4 input capture input, output compare output, or PWM output.
	TIOCA5 TIOCB5	28 29	31 32	Input/ Output	Pins for the TGRA_5 and TGRB_5 input capture input, output compare output, or PWM output.
8-bit timer	TMO3 to TMO0	88 to 85	91 to 88	Output	Compare-match output pins.
	TMCI23 TMCI01	89 90	92 93	Input	Pins for external clock input to the counter.
	TMRI23 TMRI01	89 90	92 93	Input	Counter reset input pins.
Watchdog timer (WDT)	BUZZ	74	77	Output	This pin outputs the pulse that is divided by watchdog timer.
Serial communi-cation interface (SCI)/ smart card interface	TxD3 TxD2 TxD1 TxD0	83 31 79 76	86 34 82 79	Output	Data output pins.
	RxD3 RxD2 RxD1 RxD0	84 32 80 77	87 35 83 80	Input	Data input pins.
	SCK3 SCK2 SCK1 SCK0	85 33 81 78	88 36 84 81	Input/ Output	Clock input/output pins. SCK1 outputs NMOS push/pull.
I^2C bus interface (IIC) (optional)	SCL1 SCL0	79 81	82 84	Input/ Output	I^2C clock input/output pins. These pins drive bus. The output of SCL0 is NMOS open drain.
	SDA1 SDA0	78 80	81 83	Input/ Output	I^2C data input/output pins. These pins drive bus. The output of SDA0 is NMOS open drain.

- Stack Structure

  In advanced mode, when the program counter (PC) is pushed onto the stack in a subroutine call, and the PC, condition-code register (CCR), and extended control register (EXR) are pushed onto the stack in exception handling, they are stored as shown in figure 2.4. When EXR is invalid, it is not pushed onto the stack. For details, see section 4, Exception Handling.



(a) Subroutine Branch (b) Exception Handling

Notes: 1. When EXR is not used it is not stored on the stack.
2. SP when EXR is not used.
3. Ignored when returning.

Figure 2.4 Stack Structure in Advanced Mode

4.3.3 Interrupts after Reset

If an interrupt is accepted after a reset and before the stack pointer (SP) is initialized, the PC and CCR will not be saved correctly, leading to a program crash. To prevent this, all interrupt requests, including NMI, are disabled immediately after a reset. Since the first instruction of a program is always executed immediately after the reset state ends, make sure that this instruction initializes the stack pointer (example: MOV.L #xx,SP).

4.3.4 State of On-Chip Peripheral Modules after Reset Release

After reset release, MSTPCRA is initialized to H'3F, MSTPCRB and MSTPCRC are initialized to H'FF, and all modules except the DMAC* and DTC enter module stop mode. Consequently, on-chip peripheral module registers cannot be read or written to. Register reading and writing is enabled when the module stop mode is exited.

Note: * Supported only by the H8S/2239 Group.

4.4 Traces

Traces are enabled in interrupt control mode 2. Trace mode is not activated in interrupt control mode 0, irrespective of the state of the T bit. For details of interrupt control modes, see section 5, Interrupt Controller.

If the T bit in EXR is set to 1, trace mode is activated. In trace mode, a trace exception occurs on completion of each instruction. Trace mode is not affected by interrupt masking. Table 4.4 shows the state of CCR and EXR after execution of trace exception handling. Trace mode is canceled by clearing the T bit in EXR to 0. Interrupts are accepted even within the trace exception handling routine.

The T bit saved on the stack retains its value of 1, and when control is returned from the trace exception handling routine by the RTE instruction, trace mode resumes. Trace exception handling is not carried out after execution of the RTE instruction.

The interrupt source selected is the interrupt with the highest priority level, and whose priority level set in IPR is higher than the mask level.

Table 5.5 Interrupts Selected in Each Interrupt Control Mode (2)

Interrupt Control Mode	Selected Interrupts
0	All interrupts
2	Highest-priority-level (IPR) interrupt whose priority level is greater than the mask level (IPR > I2 to I0).

Default Priority Determination: When an interrupt is selected by 8-level control, its priority is determined and a vector number is generated.

If the same value is set for IPR, acceptance of multiple interrupts is enabled, and so only the interrupt source with the highest priority according to the preset default priorities is selected and has a vector number generated.

Interrupt sources with a lower priority than the accepted interrupt source are held pending.

Table 5.6 shows operations and control signal functions in each interrupt control mode.

Table 5.6 Operations and Control Signal Functions in Each Interrupt Control Mode

Interrupt Control Mode	Setting		Interrupt Acceptance Control		8-Level Control			Default Priority Determination	T (Trace)
	INTM1	INTM0		I		I2 to I0	IPR		
0	0	0	O	IM	X	—	—*2	O	—
2	1	0	X	—*1	O	IM	PR	O	T

Legend:
O: Interrupt operation control performed.
X: No operation (All interrupts enabled).
IM: Used as interrupt mask bit.
PR: Sets priority.
—: Not used.
Notes: 1. Set to 1 when interrupt is accepted.
2. Keep the initial setting.

IOAR can be used in short address mode but not in full address mode.

8.3.3 Execute Transfer Count Registers (ETCRA and ETCRB)

ETCR is a 16-bit readable/writable register that specifies the number of transfers.

The DMA has four ETCR registers: ETCR_0A in channel 0 (channel 0A), ETCR_0B in channel 0 (channel 0B), ETCR_1A in channel 1 (channel 1A), and ETCR_1B in channel 1 (channel 1B).

ETCR is not initialized by a reset or in standby mode.

Short Address Mode: The function of ETCR in sequential mode and idle mode differs from that in repeat mode.

In sequential mode and idle mode, ETCR functions as a 16-bit transfer counter. ETCR is decremented by 1 each time a transfer is performed, and when the count reaches H'00, the DTE bit in DMABCRL is cleared, and transfer ends.

In repeat mode, ETCRL functions as an 8-bit transfer counter and ETCRH functions as a transfer count holding register. ETCRL is decremented by 1 each time a transfer is performed, and when the count reaches H'00, ETCRL is loaded with the value in ETCRH. At this point, MAR is automatically restored to the value it had when the count was started. The DTE bit in DMABCRL is not cleared, and so transfers can be performed repeatedly until the DTE bit is cleared by the user.

Full Address Mode: The function of ETCR in normal mode differs from that in block transfer mode.

In normal mode, ETCRA functions as a 16-bit transfer counter. ETCRA is decremented by 1 each time a data transfer is performed, and transfer ends when the count reaches H'0000. ETCRB is not used in normal mode.

In block transfer mode, ETCRAL functions as an 8-bit block size counter and ETCRAH functions as a block size holding register. ETCRAL is decremented by 1 each time a 1-byte or 1-word transfer is performed, and when the count reaches H'00, ETCRAL is loaded with the value in ETCRAH. So by setting the block size in ETCRAH and ETCRAL, it is possible to repeatedly transfer blocks consisting of any desired number of bytes or words.

In block transfer mode, ETCRB functions as a 16-bit block transfer counter. ETCRB is decremented by 1 each time a block is transferred, and transfer ends when the count reaches H'0000.

9.7 Examples of Use of the DTC

9.7.1 Normal Mode

An example is shown in which the DTC is used to receive 128 bytes of data via the SCI.

1. Set MRA to a fixed source address (SM1 = SM0 = 0), incrementing destination address (DM1 = 1, DM0 = 0), normal mode (MD1 = MD0 = 0), and byte size (Sz = 0). The DTS bit can have any value. Set MRB for one data transfer by one interrupt (CHNE = 0, DISEL = 0). Set the SCI RDR address in SAR, the start address of the RAM area where the data will be received in DAR, and 128 (H'0080) in CRA. CRB can be set to any value.
2. Set the start address of the register information at the DTC vector address.
3. Set the corresponding bit in DTCER to 1.
4. Set the SCI to the appropriate receive mode. Set the RIE bit in SCR to 1 to enable the reception complete (RXI) interrupt. Since the generation of a receive error during the SCI reception operation will disable subsequent reception, the CPU should be enabled to accept receive error interrupts.
5. Each time the reception of one byte of data has been completed on the SCI, the RDRF flag in SSR is set to 1, an RXI interrupt is generated, and the DTC is activated. The receive data is transferred from RDR to RAM by the DTC. DAR is incremented and CRA is decremented. The RDRF flag is automatically cleared to 0.
6. When CRA becomes 0 after the 128 data transfers have been completed, the RDRF flag is held at 1, the DTCE bit is cleared to 0, and an RXI interrupt request is sent to the CPU. The interrupt handling routine will perform wrap-up processing.

9.7.2 Software Activation

An example is shown in which the DTC is used to transfer a block of 128 bytes of data by means of software activation. The transfer source address is H'1000 and the destination address is H'2000. The vector number is H'60, so the vector address is H'04C0.

1. Set MRA to incrementing source address (SM1 = 1, SM0 = 0), incrementing destination address (DM1 = 1, DM0 = 0), block transfer mode (MD1 = 1, MD0 = 0), and byte size (Sz = 0). The DTS bit can have any value. Set MRB for one block transfer by one interrupt (CHNE = 0). Set the transfer source address (H'1000) in SAR, the destination address (H'2000) in DAR, and 128 (H'8080) in CRA. Set 1 (H'0001) in CRB.
2. Set the start address of the register information at the DTC vector address (H'04C0).
3. Check that the SWDTE bit in DTVECR is 0. Check that there is currently no transfer activated by software.

10.4.2 Port 7 Data Register (P7DR)

P7DR stores output data for port 7 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P77DR	0	R/W	Output data for a pin is stored when the pin is specified as a general purpose output port.
6	P76DR	0	R/W	
5	P75DR	0	R/W	
4	P74DR	0	R/W	
3	P73DR	0	R/W	
2	P72DR	0	R/W	
1	P71DR	0	R/W	
0	P70DR	0	R/W	

10.4.3 Port 7 Register (PORT7)

PORT7 shows the pin states. This register cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	P77	—*	R	If a port 1 read is performed while P7DDR bits are set to 1, the P7DR values are read. If a port 1 read is performed while P7DDR bits are cleared to 0, the pin states are read.
6	P76	—*	R	
5	P75	—*	R	
4	P74	—*	R	
3	P73	—*	R	
2	P72	—*	R	
1	P71	—*	R	
0	P70	—*	R	

Note: * Determined by the states of pins P77 to P70.

12.6 Operation with Cascaded Connection

If bits CKS2 to CKS0 in one of TCR_0 and TCR_1 (TCR_2 and TCR_3)* are set to B'100, the 8-bit timers of the two channels are cascaded. With this configuration, a single 16-bit timer can be used (16-bit timer mode) or compare-matches of 8-bit channel 0 (channel 2)* can be counted by the timer of channel 1 (channel 3)* (compare-match count mode). In the case that channel 0 is connected to channel 1 in cascade, the timer operates as described below.

Note: * Not available in the H8S/2237 Group and H8S/2227 Group.

12.6.1 16-Bit Count Mode

When bits CKS2 to CKS0 in TCR_0 are set to B'100, the timer functions as a single 16-bit timer with channel 0 occupying the upper 8 bits and channel 1 occupying the lower 8 bits.

- Setting of compare-match flags
  - The CMF flag in TCSR_0 is set to 1 when a 16-bit compare-match occurs.
  - The CMF flag in TCSR_1 is set to 1 when a lower 8-bit compare-match occurs.
- Counter clear specification
  - If the CCLR1 and CCLR0 bits in TCR_0 have been set for counter clear at compare-match, the 16-bit counter (TCNT_0 and TCNT_1 together) is cleared when a 16-bit compare-match occurs. The 16-bit counter (TCNT_0 and TCNT_1 together) is cleared even if counter clear by the TMRI01 pin has also been set.
  - The settings of the CCLR1 and CCLR0 bits in TCR_1 are ignored. The lower 8 bits cannot be cleared independently.
- Pin output
  - Control of output from the TMO0 pin by bits OS3 to OS0 in TCSR_0 is in accordance with the 16-bit compare-match conditions.
  - Control of output from the TMO1 pin by bits OS3 to OS0 in TCSR_1 is in accordance with the lower 8-bit compare-match conditions.

12.6.2 Compare-Match Count Mode

When bits CKS2 to CKS0 in TCR_1 are B'100, TCNT_1 counts compare-match A for channel 0. Channels 0 and 1 are controlled independently. Conditions such as setting of the CMF flag, generation of interrupts, output from the TMO pin, and counter clearing are in accordance with the settings for each channel.

Bit	Bit Name	Initial Value	R/W	Description
0	ACK	0	R/W	Acknowledge bit Status Indicates the data received in the acknowledge bit of the data field. • Acknowledge bit other than in the data field The IEB terminates the transmission and enters the wait state if a NAK is received. In this case, this bit and the TxE flag are set to 1. • Acknowledge bit in the data field The IEB retransmits data up to the maximum number of bytes defined by communications mode until an ACK is received from the receive unit if a NAK is received from the receive unit during data field transmission. In this case, when an ACK is received from the receive unit during retransmission, this flag is not set and transmission will be continued. When transmission is terminated without receiving an ACK, this flag is set to 1. Note: This flag is invalid in broadcast communications. [Setting condition] When the acknowledge bit of 1 (NAK) is detected [Clearing condition] When writing 0 after reading ACK = 1

14.6.7 Notes on DTC Specification

When transmit or receive data is transferred by the DTC, bit 5 (for transmission) or bit 6 (for reception) in DTCERG must be set by the bit manipulation instruction (such as BSET or BCLR). In this case, other bits (bits 7 and 4 to 0) in DTCERG must not be set to 1.

14.6.8 Error Handling in Transmission

Figure 14.15 shows the operation when a timing error occurs.

When a timing error occurs in data transmission (1), there is a possibility that the next data is already transferred to the transmit buffer by the DTC and the TxRDY flag that is the DTC initiation source is already cleared to 0 (2).

In this case, if retransfer is performed, data remained in the transmit buffer (previous frame data) is transmitted as the first byte data of the data field (3).

To avoid this error, in master transmission, the first byte data in the data field should be written to the transmit buffer by software instead of using the DTC. After that, data can be transferred by the DTC. In this case, the SAR (transfer source address) and CRA (transfer counter) should be specified as follows.

- An address of the on-chip memory that stores the second byte data → SAR
- The number of bytes specified by message length –1 → CRA

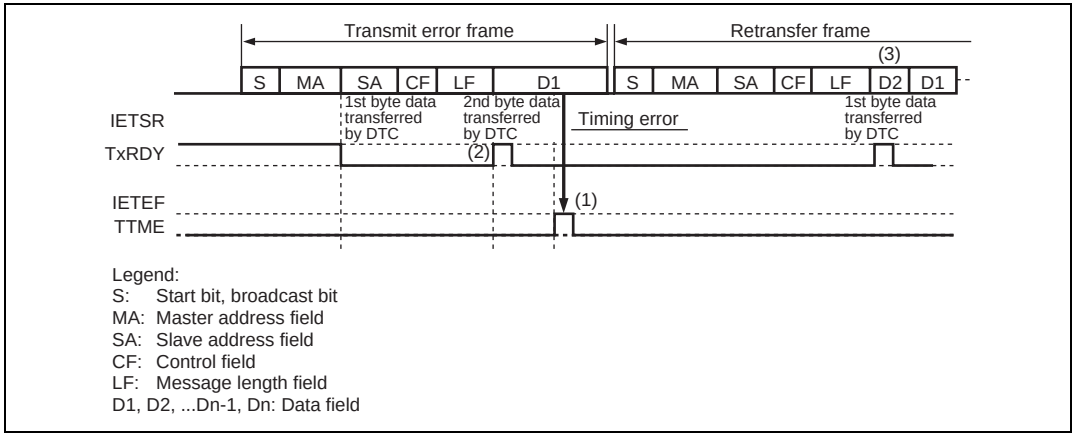


Figure 14.15 Error Processing in Transfer

Section 15 Serial Communication Interface (SCI)

This LSI has independent serial communication interfaces (SCIs). The SCI can handle both asynchronous and clocked synchronous serial communication. Serial data communication can be carried out using standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or an Asynchronous Communication Interface Adapter (ACIA). A function is also provided for serial communication between processors (multiprocessor communication function). The SCI also supports an IC card (Smart Card) interface conforming to ISO/IEC 7816-3 (Identification Card) as a serial communication interface extended function.

15.1 Features

- The number of on-chip channels

  H8S/2258 Group, H8S/2239 Group, H8S/2238 Group, and H8S/2237 Group: Four channels (channels 0, 1, 2, and 3)

  H8S/2227 Group: Three channels (channels 0, 1, and 3)
- Choice of asynchronous or clocked synchronous serial communication mode
- Full-duplex communication capability

  The transmitter and receiver are mutually independent, enabling transmission and reception to be executed simultaneously.

  Double-buffering is used in both the transmitter and the receiver, enabling continuous transmission and continuous reception of serial data.
- On-chip baud rate generator allows any bit rate to be selected

  External clock can be selected as a transfer clock source (except for in Smart Card interface mode).
- Choice of LSB-first or MSB-first transfer (except in the case of asynchronous mode 7-bit data)
- Four interrupt sources

  Transmit-end, transmit-data-empty, receive-data-full, and receive error — that can issue requests.

  The transmit-data-empty interrupt and receive data full interrupts can be used to activate the data transfer controller (DTC) or the direct memory access controller (DMAC) (H8S/2239 Group only).
- Module stop mode can be set

Asynchronous mode

- Data length: 7 or 8 bits
- Stop bit length: 1 or 2 bits

16.4.8 Operation Using the DTC

The I²C bus format provides for selection of the slave device and transfer direction by means of the slave address and the R/$\overline{W}$ bit, confirmation of reception with acknowledge bit, indication of the last frame, and so on. Therefore, continuous data transfer using the DTC must be carried out in conjunction CPU processing by means of interrupts.

Table 16.5 shows some example of processing using the DTC. These examples assume that the number of transfer data bytes is know in slave mode.

Table 16.5 Flags and Transfer States

Item	Master Transmit Mode	Master Receive Mode	Slave Transmit Mode	Slave Receive Mode
Slave address + R/$\overline{W}$ bit Transmission/ reception	Transmission by DTC (ICDR write)	Transmission by CPU (ICDR write)	Reception by CPU (ICDR read)	Reception by CPU (ICDR read)
Dummy data read	—	Processing by CPU (ICDR read)	—	—
Actual data transmission/reception	Transmission by DTC (ICDR write)	Reception by DTC (ICDR read)	Transmission by DTC (ICDR write)	Reception by DTC (ICDR read)
Dummy data (H'FF) write	—	—	Processing by DTC (ICDR write)	—
Last frame processing	Not necessary	Reception by CPU (ICDR read)	Not necessary	Reception by CPU (ICDR read)
Transfer request processing after last frame processing	1st time: Clearing by CPU 2nd time: End condition issuance by CPU	Not necessary	Automatic clearing on detection of end condition during transmission of dummy data (H'FF)	Not necessary
Setting of number of DTC transfer data frames	Transmission: Actual data count + 1 (+ 1 equivalent to slave address + R/$\overline{W}$ bits)	Reception: Actual data count	Transmission: Actual data count + 1 (+ 1 equivalent to dummy data (H'FF))	Reception: Actual data count

17.3.3 A/D Control Register (ADCR)

The ADCR enables A/D conversion started by an external trigger signal.

Bit	Bit Name	Initial Value	R/W	Description
7	TRGS1	0	R/W	Timer Trigger Select 1 and 0
6	TRGS0	0	R/W	Enables the start of A/D conversion by a trigger signal. Only set bits TRGS0 and TRGS1 while conversion is stopped (ADST = 0). 00: A/D conversion start by software is enabled 01: A/D conversion start by TPU conversion start trigger is enabled 10: A/D conversion start by 8-bit timer conversion start trigger is enabled 11: A/D conversion start by external trigger pin ($\overline{\text{ADTRG}}$) is enabled
5, 4	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
3	CKS1	0	R/W	Clock Select 1 and 0
2	CKS0	0	R/W	These bits specify the A/D conversion time. The conversion time should be changed only when ADST = 0. Specify a setting that gives a value within the range shown in table 27.10 (H8S/2258 Group), table 27.23 (H8S/2239 Group), table 27.35 (H8S/2238B and H8S/ 2236B), table 27.47 (H8S/2238R and H8S/ 2236R), or table 27.57 (H8S/2237 Group and H8S/2227 Group). 00: Conversion time = 530 states (max) 01: Conversion time = 266 states (max) 10: Conversion time = 134 states (max) 11: Conversion time = 68 states (max)
1, 0	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TGRD_3	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	TPU_3
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR_4	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU_4
TMDR_4	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_4	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_4	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_4	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_4	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRA_4	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRB_4	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR_5	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU_5
TMDR_5	—	—	—	—	MD3	MD2	MD1	MD0	
TIOR_5	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0	
TIER_5	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_5	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_5	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRA_5	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TGRB_5	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TSTR	—	—	CST5	CST4	CST3	CST2	CST1	CST0	TPU
TSYR	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0	
IPRA	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	INT
IPRB	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRC	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRD	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	
IPRE	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0	

Register Name	Reset	Manual Reset	High-speed	Medium-speed	Sleep	Module Stop	Watch	Sub-active	Sub-sleep	Software Standby	Hardware Standby	Module
BRR_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	SCI_0
ICSR_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	IIC_0
SCR_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	SCI_0
TDR_0	Initialized	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	
SSR_0	Initialized	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	
RDR_0	Initialized	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	
SCMR_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
ICDR_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	IIC_0
SARX_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
ICMR_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
SAR_0	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
SMR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	SCI_1
ICCR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	IIC_1
BRR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	SCI_1
ICSR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	IIC_1
SCR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	SCI_1
TDR_1	Initialized	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	
SSR_1	Initialized	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	
RDR_1	Initialized	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	
SCMR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
ICDR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	IIC_1
SARX_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
ICMR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
SAR_1	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
SMR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	SCI_2
BRR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
SCR_2	Initialized	Initialized	—	—	—	—	—	—	—	—	Initialized	
TDR_2	Initialized	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	
SSR_2	Initialized	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	
RDR_2	Initialized	Initialized	—	—	—	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	
SCMR_2	Initialized	—	—	—	—	—	—	—	—	—	Initialized	

27.2.3 AC Characteristics

Figure 27.6 shows the test conditions for the AC characteristics.

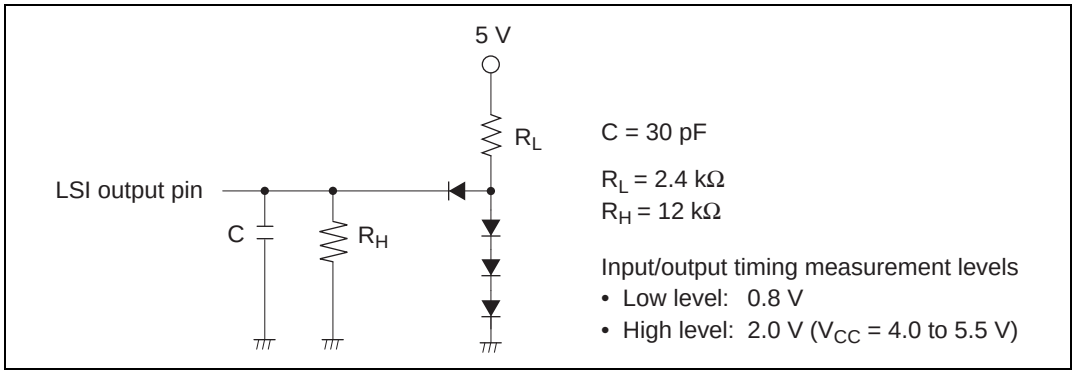


Figure 27.6 Output Load Circuit

Table 27.29 Bus Drive Characteristics

Condition A (F-ZTAT version): V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.6 V to 5.5 V,
V_{ref} = 3.6 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)*

Condition B (Masked ROM version): V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 3.6 V to 5.5 V,
V_{ref} = 3.6 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)*

Applicable Pins: SCL1 and SCL0, SDA1 and SDA0

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	VT^-	$V_{CC} \times 0.3$	—	—	V	V_{CC} = 2.7 V to 5.5 V
	VT^+	—	—	$V_{CC} \times 0.7$		V_{CC} = 2.7 V to 5.5 V
	$VT^+ – VT^-$	0.4	—	—		V_{CC} = 4.0 V to 5.5 V
		$V_{CC} \times 0.05$	—	—		V_{CC} = 2.7 V to 4.0 V
Input high voltage	V_{IH}	$V_{CC} \times 0.7$	—	V_{CC} + 0.5	V	V_{CC} = 2.7 V to 5.5 V
Input low voltage	V_{IL}	–0.5	—	$V_{CC} \times 0.3$	V	V_{CC} = 2.7 V to 5.5 V
Output low voltage	V_{OL}	—	—	0.5	V	I_{OL} = 8 mA, V_{CC} = 4.0 V to 5.5 V
		—	—	0.4		I_{OL} = 3 mA
Input capacitance	C_{in}	—	—	20	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
Three-state leakage current (off state)	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
SCL, SDA output fall time	t_{Of}	20 + 0.1 Cb	—	250	ns	V_{CC} = 2.7 V to 5.5 V

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open. Apply a voltage between 2.0 V and 5.5 V to the AV_{CC} and V_{ref} pins by connecting them to V_{CC}, for instance. Set $V_{ref} \leq AV_{CC}$.

(3) Bus Timing

Table 27.44 lists the bus timing.

Table 27.44 Bus Timing

Condition A (F-ZTAT version and masked ROM version):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V,
V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ϕ = 2 to 13.5 MHz,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Condition B (F-ZTAT version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V,
V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ϕ = 2 to 6.25 MHz,
T_a = –20°C to +75°C (regular specifications)

Condition C (Masked ROM version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V,
V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ϕ = 2 to 6.25 MHz,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Conditions B, C			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address delay time	t_{AD}	—	50	—	90	ns	Figures 27.14 to 27.18
Address setup time	t_{AS}	0.5 × t_{cyc} – 30	—	0.5 × t_{cyc} – 60	—	ns	
Address hold time	t_{AH}	0.5 × t_{cyc} – 15	—	0.5 × t_{cyc} – 30	—	ns	
$\overline{CS}$ delay time	t_{CSD}	—	50	—	90	ns	
$\overline{AS}$ delay time	t_{ASD}	—	50	—	90	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	50	—	90	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	50	—	90	ns	
Read data setup time	t_{RDS}	30	—	50	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	1.0 × t_{cyc} – 65	—	1.0 × t_{cyc} – 90	ns	

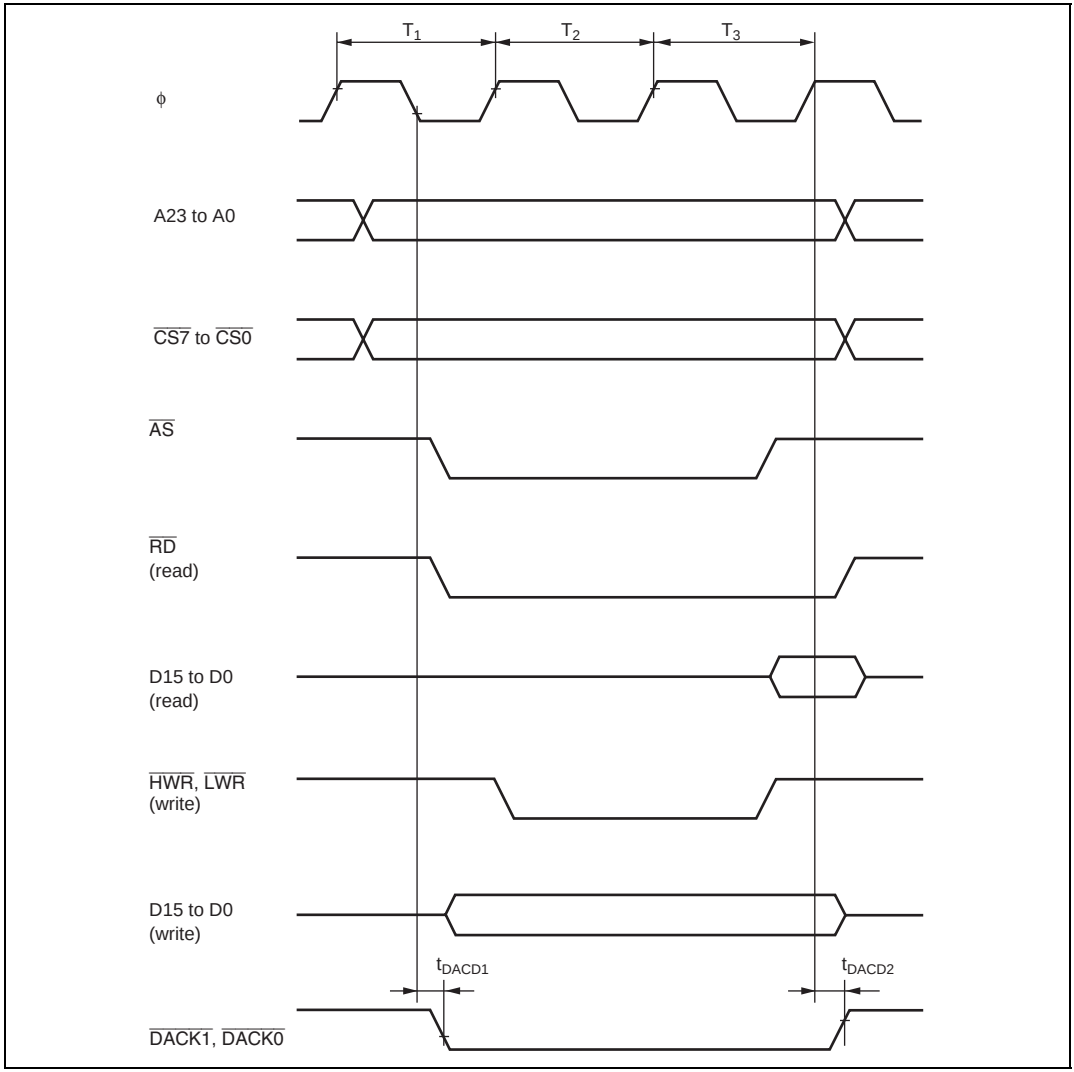
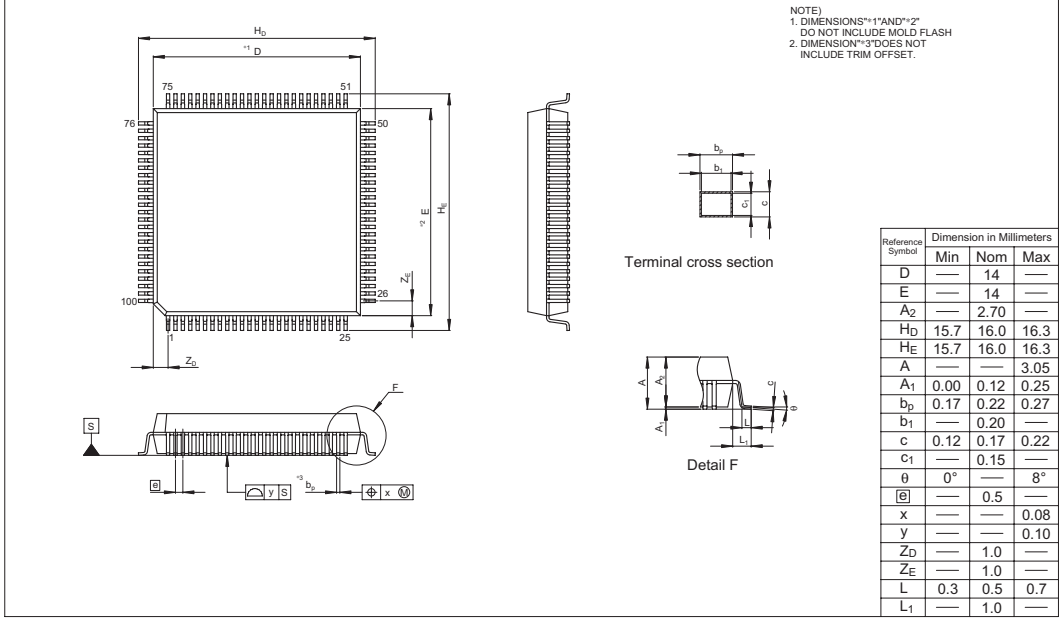


Figure 27.21 DMAC Single Address Transfer Timing (Three-State Access)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x14-0.50	PRQP0100KA-A	FP-100B/FP-100BV	1.2g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	14	—
E	—	14	—
A_2	—	2.70	—
H_D	15.7	16.0	16.3
H_E	15.7	16.0	16.3
A	—	—	3.05
A_1	0.00	0.12	0.25
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.12	0.17	0.22
c_1	—	0.15	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure C.4 FP-100B Package Dimensions