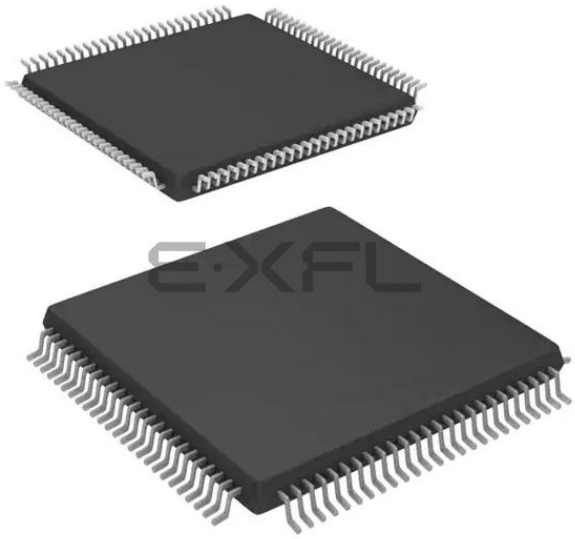

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | H8S/2000 |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | I²C, SCI, SmartCard |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 72 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df2239tf16v |

### 8.5.6 Normal Mode

In normal mode, transfer is performed with channels A and B used in combination. Normal mode can be specified by setting the FAE bit in DMABCRH to 1 and clearing the BLKE bit in DMACRA to 0. In normal mode, MAR is updated after data transfer of a byte or word in response to a single transfer request, and this is executed the number of times specified in ETCRA. The transfer source is specified by MARA, and the transfer destination by MARB. Table 8.9 summarizes register functions in normal mode.

**Table 8.9 Register Functions in Normal Mode**

| Register | Function | Initial Setting | Operation |
|---|---|---|---|
|  | Source address register | Start address of transfer source | Incremented/decremented every transfer, or fixed |
|  | Destination address register | Start address of transfer destination | Incremented/decremented every transfer, or fixed |
|  | Transfer counter | Number of transfers | Decremented every transfer; transfer ends when count reaches H'0000 |

MARA and MARB specify the start addresses of the transfer source and transfer destination, respectively, as 24 bits. MAR can be incremented or decremented by 1 or 2 each time a byte or word is transferred, or can be fixed. Incrementing, decrementing, or holding a fixed value can be set separately for MARA and MARB.

The number of transfers is specified by ETCRA as 16 bits. ETCRA is decremented by 1 each time a transfer is performed, and when its value reaches H'0000 the DTE bit in DMABCRL is cleared and transfer ends. If the DTIE bit in DMABCRL is set to 1 at this time, an interrupt request is sent to the CPU or DTC. The maximum number of transfers, when H'0000 is set in ETCRA, is 65,536.

### 8.5.8 Basic Bus Cycles

An example of the basic DMAC bus cycle timing is shown in figure 8.18. In this example, word-size transfer is performed from 16-bit, 2-state access space to 8-bit, 3-state access space. When the bus is transferred from the CPU to the DMAC, a source address read and destination address write are performed. The bus is not released in response to another bus request, etc., between these read and write operations. As like CPU cycles, DMA cycles conform to the bus controller settings.

The address is not output to the external address bus in an access to on-chip memory or an internal I/O register.

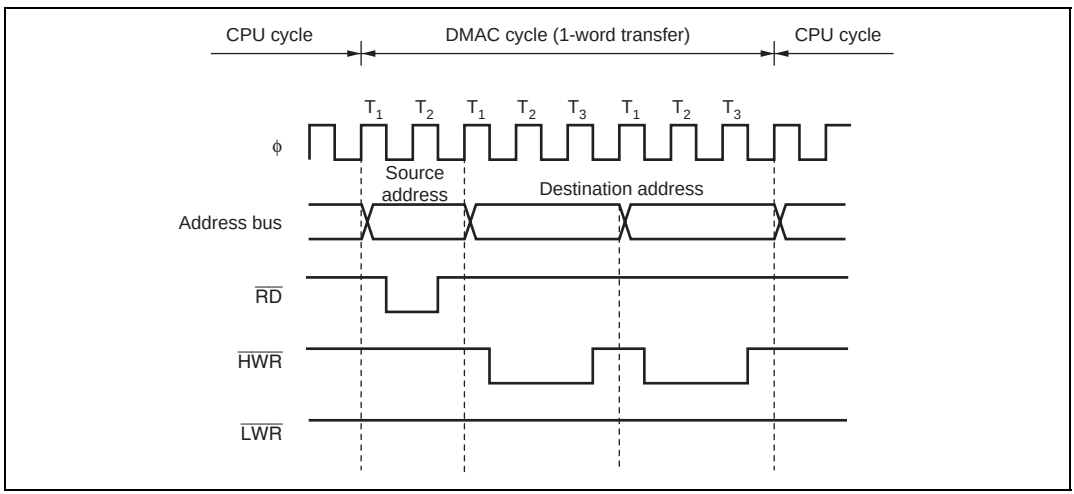
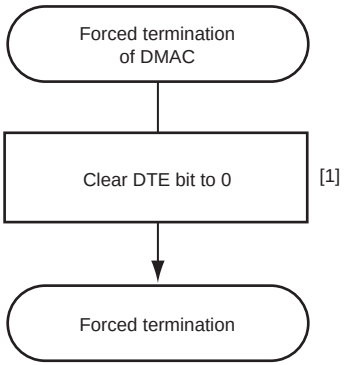



**Figure 8.18 Example of DMA Transfer Bus Timing**

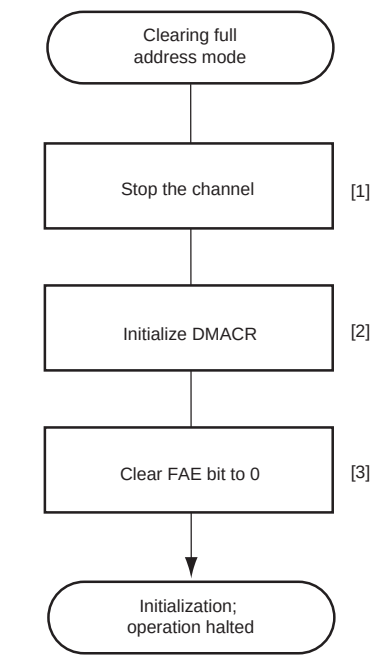



[1] Clear the DTE bit in DMABCRL to 0.
To prevent interrupt generation after forced termination of DMAC operation, clear the DTIE bit to 0 at the same time.

**Figure 8.35 Example of Procedure for Forcibly Terminating DMAC Operation**

### 8.5.15 Clearing Full Address Mode

Figure 8.36 shows the procedure for releasing and initializing a channel designated for full address mode. After full address mode has been cleared, the channel can be set to another transfer mode using the appropriate setting procedure.




[1] Clear both the DTE bit and DTME bit in DMABCRL to 0, or wait until the transfer ends and the DTE bit is cleared to 0, then clear the DTME bit to 0. Also clear the corresponding DTIE bit to 0 at the same time.

[2] Clear all bits in DMACRA and DMACRB to 0.

[3] Clear the FAE bit in DMABCRH to 0.

**Figure 8.36 Example of Procedure for Clearing Full Address Mode**

### 10.4.2 Port 7 Data Register (P7DR)

P7DR stores output data for port 7 pins.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | P77DR | 0 | R/W | Output data for a pin is stored when the pin is specified as a general purpose output port. |
| 6 | P76DR | 0 | R/W | |
| 5 | P75DR | 0 | R/W | |
| 4 | P74DR | 0 | R/W | |
| 3 | P73DR | 0 | R/W | |
| 2 | P72DR | 0 | R/W | |
| 1 | P71DR | 0 | R/W | |
| 0 | P70DR | 0 | R/W | |

### 10.4.3 Port 7 Register (PORT7)

PORT7 shows the pin states. This register cannot be modified.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | P77 | —* | R | If a port 1 read is performed while P7DDR bits are set to 1, the P7DR values are read. If a port 1 read is performed while P7DDR bits are cleared to 0, the pin states are read. |
| 6 | P76 | —* | R | |
| 5 | P75 | —* | R | |
| 4 | P74 | —* | R | |
| 3 | P73 | —* | R | |
| 2 | P72 | —* | R | |
| 1 | P71 | —* | R | |
| 0 | P70 | —* | R | |

Note: * Determined by the states of pins P77 to P70.

### 10.9.2 Port D Data Register (PDDR)

PDDR stores output data for port D pins.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | PD7DR | 0 | R/W | Output data for a pin is stored when the pin is specified as a general purpose output port. |
| 6 | PD6DR | 0 | R/W | |
| 5 | PD5DR | 0 | R/W | |
| 4 | PD4DR | 0 | R/W | |
| 3 | PD3DR | 0 | R/W | |
| 2 | PD2DR | 0 | R/W | |
| 1 | PD1DR | 0 | R/W | |
| 0 | PD0DR | 0 | R/W | |

### 10.9.3 Port D Register (PORTD)

PORTD shows port D pin states. This register cannot be modified.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | PD7 | —* | R | If a port D read is performed while PDDDR bits are set to 1, the PDDR values are read. If a port D read is performed while PDDDR bits are cleared to 0, the pin states are read. |
| 6 | PD6 | —* | R | |
| 5 | PD5 | —* | R | |
| 4 | PD4 | —* | R | |
| 3 | PD3 | —* | R | |
| 2 | PD2 | —* | R | |
| 1 | PD1 | —* | R | |
| 0 | PD0 | —* | R | |

Note: * Determined by the states of pins PD7 to PD0.

**Table 11.24 TIORH_3**

| | | | | Description | |
|---|---|---|---|---|---|
| **Bit 3 IOA3** | **Bit 2 IOA2** | **Bit 1 IOA1** | **Bit 0 IOA0** | **TGRA_3 Function*** | **TIOCA3 Pin Function*** |
| 0 | 0 | 0 | 0 | Output compare register | Output disabled |
| | | | 1 | | Initial output is 0 output<br>0 output at compare match |
| | | 1 | 0 | | Initial output is 0 output<br>1 output at compare match |
| | | | 1 | | Initial output is 0 output<br>Toggle output at compare match |
| | 1 | 0 | 0 | | Output disabled |
| | | | 1 | | Initial output is 1 output<br>0 output at compare match |
| | | 1 | 0 | | Initial output is 1 output<br>1 output at compare match |
| | | | 1 | | Initial output is 1 output<br>Toggle output at compare match |
| 1 | 0 | 0 | 0 | Input capture register | Capture input source is TIOCA3 pin<br>Input capture at rising edge |
| | | | 1 | | Capture input source is TIOCA3 pin<br>Input capture at falling edge |
| | | 1 | × | | Capture input source is TIOCA3 pin<br>Input capture at both edges |
| | 1 | × | × | | Capture input source is channel 4/count clock<br>Input capture at TCNT_4 count-up/count-down |

Legend: ×: Don't care

Note: * Not available in the H8S/2227 Group.

2. Examples of waveform output operation

Figure 11.7 shows an example of 0 output/1 output.

In this example, TCNT has been designated as a free-running counter, and settings have been made so that 1 is output by compare match A, and 0 is output by compare match B. When the set level and the pin level match, the pin level does not change.

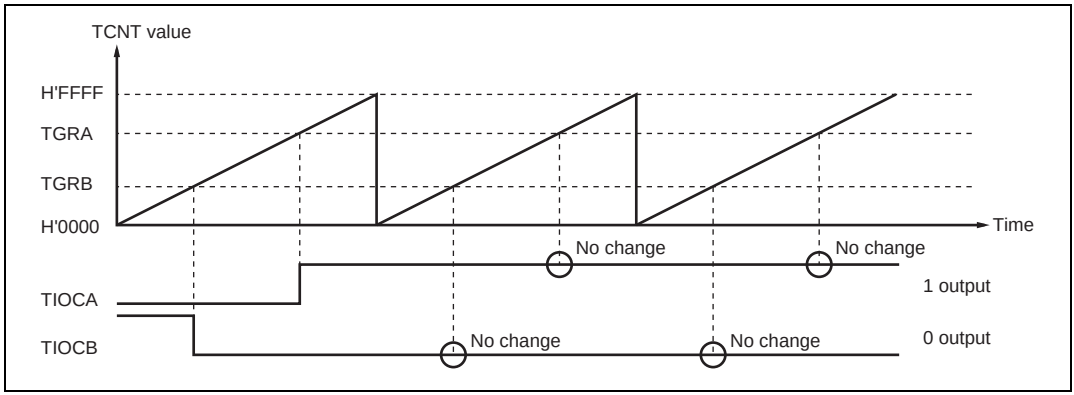



**Figure 11.7 Example of 0 Output/1 Output Operation**

Figure 11.8 shows an example of toggle output.

In this example TCNT has been designated as a periodic counter (with counter clearing performed by compare match B), and settings have been made so that output is toggled by both compare match A and compare match B.

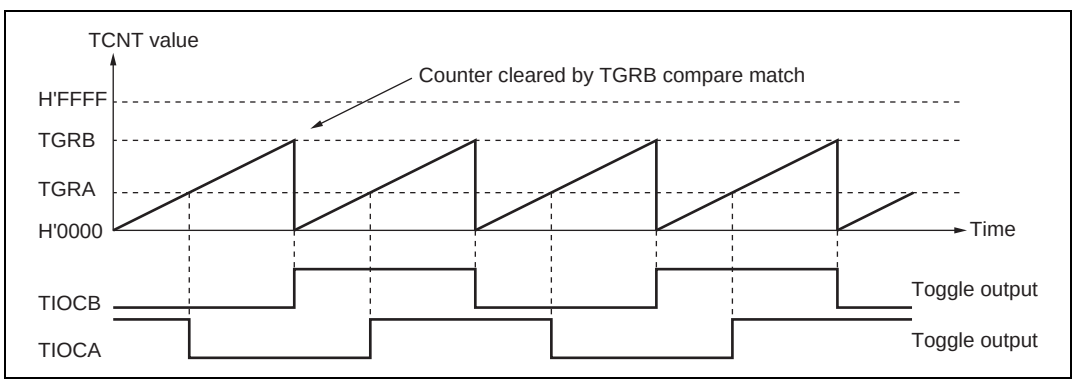



**Figure 11.8 Example of Toggle Output Operation**

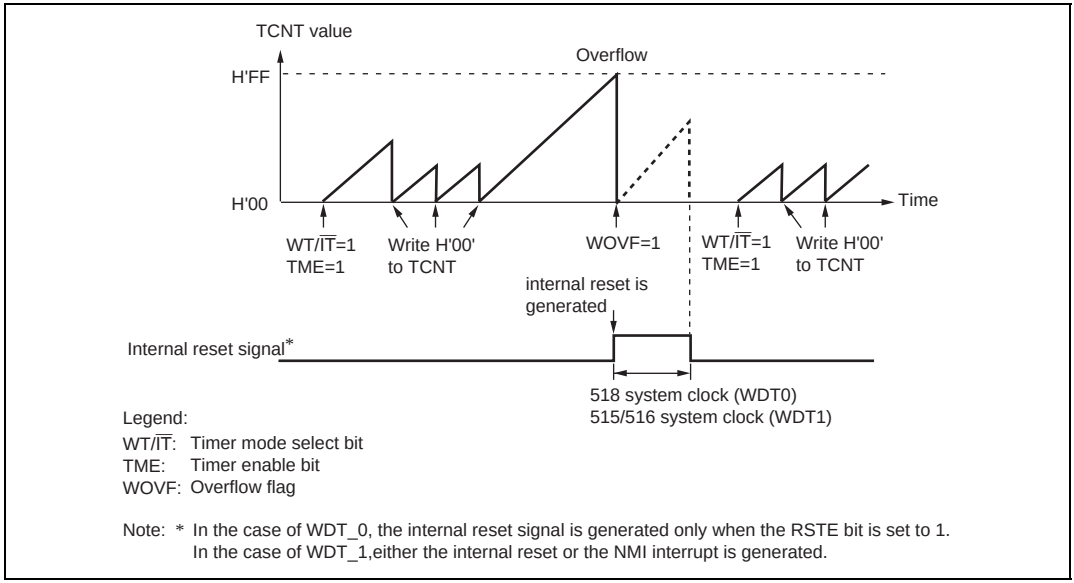



**Figure 13.2 Watchdog Timer Mode Operation**

### 13.4.2 Interval Timer Mode

To use the WDT as a watchdog timer, set the WT/$\overline{IT}$ and TME bits in TCSR to 1.

When the WDT is used as an interval timer, an interval timer interrupt (WOVI) is generated each time the TCNT overflows. (The NMI interrupt is not generated.) Therefore, an interrupt can be generated at intervals.

### 14.3.10 IEBus Reception Master Address Register 1 (IEMA1)

IEMA1 indicates the lower four bits of the communications destination master unit address in slave/broadcast reception. This register is enabled when slave/broadcast reception starts, and the contents are changed at the timing of setting the RxS flag in IERSR.

If a broadcast receive error interrupt is selected by the DEE bit in IECTR and the receive buffer is not in the receive enabled state on control field reception, a receive error interrupt is generated and the lower 4 bits of the master address are stored in IEMA1. This register cannot be modified.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | IMA3 | 0 | R | Lower 4 Bits of IEBus Reception Master Address |
| 6 | IMA2 | 0 | R | Indicate the lower 4 bits of the communications destination master unit address in slave/broadcast reception. |
| 5 | IMA1 | 0 | R | |
| 4 | IMA0 | 0 | R | |
| 3 to 0 | — | All 0 | R | Reserved<br>These bits are always read as 0. |

### 14.3.11 IEBus Reception Master Address Register 2 (IEMA2)

IEMA2 indicates the upper 8 bits of the communications destination master unit address in slave/broadcast reception. This register is enabled when slave/broadcast reception starts, and the contents are changed at the timing of setting the RxS flag in IERSR.

If a broadcast receive error interrupt is selected with the DEE bit in IECTR and the receive buffer is not in the receive enabled state at control field reception, a receive error interrupt is generated and the upper 8 bits of the master address are stored in IEMA2. This register cannot be modified by a write.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | IMA11 | 0 | R | Upper 8 Bits of IEBus Reception Master Address |
| 6 | IMA10 | 0 | R | Indicate the upper 8 bits of the communications destination master unit address in slave/broadcast reception. |
| 5 | IMA9 | 0 | R | |
| 4 | IMA8 | 0 | R | |
| 3 | IMA7 | 0 | R | |
| 2 | IMA6 | 0 | R | |
| 1 | IMA5 | 0 | R | |
| 0 | IMA4 | 0 | R | |

### 14.6.7 Notes on DTC Specification

When transmit or receive data is transferred by the DTC, bit 5 (for transmission) or bit 6 (for reception) in DTCERG must be set by the bit manipulation instruction (such as BSET or BCLR). In this case, other bits (bits 7 and 4 to 0) in DTCERG must not be set to 1.

### 14.6.8 Error Handling in Transmission

Figure 14.15 shows the operation when a timing error occurs.

When a timing error occurs in data transmission (1), there is a possibility that the next data is already transferred to the transmit buffer by the DTC and the TxRDY flag that is the DTC initiation source is already cleared to 0 (2).

In this case, if retransfer is performed, data remained in the transmit buffer (previous frame data) is transmitted as the first byte data of the data field (3).

To avoid this error, in master transmission, the first byte data in the data field should be written to the transmit buffer by software instead of using the DTC. After that, data can be transferred by the DTC. In this case, the SAR (transfer source address) and CRA (transfer counter) should be specified as follows.

- An address of the on-chip memory that stores the second byte data → SAR
- The number of bytes specified by message length –1 → CRA

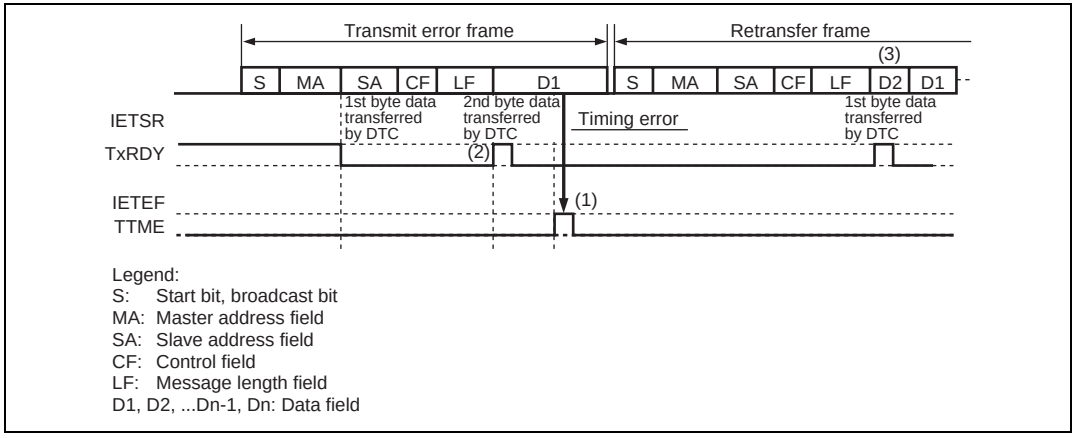
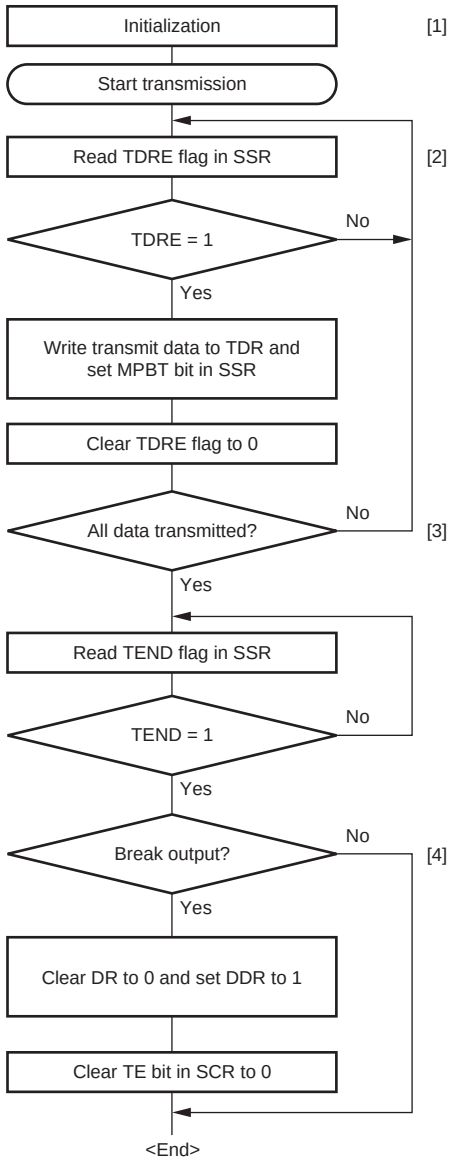



**Figure 14.15 Error Processing in Transfer**

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 3 | PER | 0 | R/(W)*1 | Parity Error<br>Indicates that a parity error occurred during reception using parity addition in asynchronous mode, causing abnormal termination.<br>[Setting condition]<br>When a parity error is detected during reception<br>If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Also, subsequent serial reception cannot be continued while the PER flag is set to 1. In clocked synchronous mode, serial transmission cannot be continued, either.<br>[Clearing condition]<br>When 0 is written to PER after reading PER = 1<br>The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0. |




[1] SCI initialization:
The TxD pin is automatically designated as the transmit data output pin.
After the TE bit is set to 1, a frame of 1s is output, and transmission is enabled.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR. Set the MPBT bit in SSR to 0 or 1. Finally, clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:
To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and then clear the TDRE flag to 0. Checking and clearing of the TDRE flag is automatic when the DMAC*1 or the DTC*2 is activated by a transmit-data-empty interrupt (TXI) request, and data is written to TDR.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, set the port DR to 0, clear DDR to 1, then clear the TE bit in SCR to 0.

Notes: 1. Supported only by the H8S/2239 Group.
2. The case, in which the DTC automatically clears the TDRE flag, occurs only when DISEL in DTC is 0 with the transfer counter not being 0. Therefore, the TDRE flag should be cleared by CPU when DISEL is 1, or when DISEL is 0 with the transfer counter being 0.

**Figure 15.14 Sample Multiprocessor Serial Transmission Flowchart**

## 15.6 Operation in Clocked Synchronous Mode

Figure 15.17 shows the general format for clocked synchronous communication. In clocked synchronous mode, data is transmitted or received synchronous with clock pulses. In clocked synchronous serial communication, data on the transmission line is output from one falling edge of the serial clock to the next. In clocked synchronous mode, the SCI receives data in synchronous with the rising edge of the serial clock. After 8-bit data is output, the transmission line holds the MSB state. In clocked synchronous mode, no parity or multiprocessor bit is added. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication through the use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so data can be read or written during transmission or reception, enabling continuous data transfer.

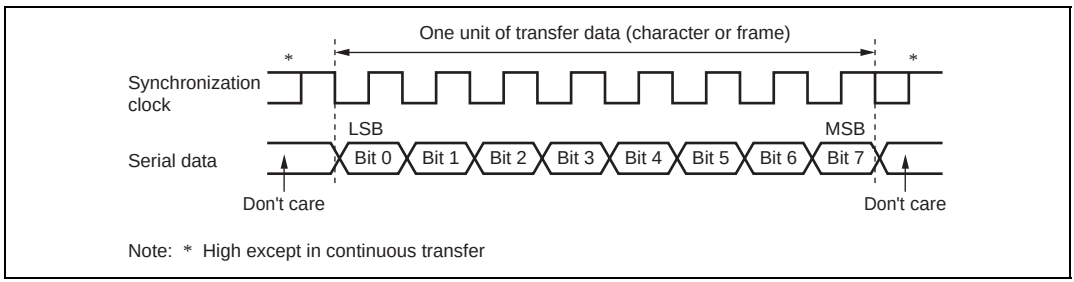



**Figure 15.17 Data Format in Synchronous Communication (For LSB-First)**

### 15.6.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK pin can be selected, according to the setting of CKE0 and CKE1 bits in SCR. When the SCI is operated on an internal clock, the serial clock is output from the SCK pin. Eight serial clock pulses are output in the transfer of one character, and when no transfer is performed the clock is fixed high.

### 15.6.2 SCI Initialization (Clocked Synchronous Mode)

Before transmitting and receiving data, the TE and RE bits in SCR should be cleared to 0, then the SCI should be initialized as described in a sample flowchart in figure 15.18. When the operating mode, or transfer format, is changed for example, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag is set to 1. Note that clearing the RE bit to 0 does not change the contents of the RDRF, PER, FER, and ORER flags, or the contents of RDR.

## 15.10 Usage Notes

### 15.10.1 Module Stop Mode Setting

SCI operation can be disabled or enabled using the module stop control register. The initial setting is for SCI operation to be halted. Register access is enabled by clearing module stop mode. For details, refer to section 24, Power-Down Modes.

### 15.10.2 Break Detection and Processing (Asynchronous Mode Only)

When framing error (FER) detection is performed, a break can be detected by reading the RxD pin value directly. In a break, the input from the RxD pin becomes all 0s, setting the FER flag, and possibly the PER flag. Note that as the SCI continues the receive operation after receiving a break, even if the FER flag is cleared to 0, it will be set to 1 again.

### 15.10.3 Mark State and Break Detection (Asynchronous Mode Only)

When TE is 0, the TxD pin is used as an I/O port whose direction (input or output) and level are determined by DDR. This can be used to set the TxD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both DDR and DR to 1. As TE is cleared to 0 at this point, the TxD pin becomes an I/O port, and 1 is output from the TxD pin. To send a break during serial transmission, first set PDR to 1 and DR to 0, and then clear TE to 0. When TE is cleared to 0, the transmitter is initialized regardless of the current transmission state, the TxD pin becomes an I/O port, and 0 is output from the TxD pin.

### 15.10.4 Receive Error Flags and Transmit Operations (Clocked Synchronous Mode Only)

Transmission cannot be started when a receive error flag (ORER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

**Table 16.7 I²C Bus Timing (SCL and SDA Output)**

| Item | Symbol | Output Timing | Unit | Notes |
|---|---|---|---|---|
| SCL output cycle time | $t_{SCLO}$ | 28 $t_{cyc}$ to 256 $t_{cyc}$ | ns | Figure 27.34 |
| SCL output high pulse width | $t_{SCLHO}$ | 0.5 $t_{SCLO}$ | ns | |
| SCL output low pulse width | $t_{SCLLO}$ | 0.5 $t_{SCLO}$ | ns | |
| SDA output bus free time | $t_{BUFO}$ | 0.5 $t_{SCLO}$ – 1 $t_{cyc}$ | ns | |
| Start condition output hold time | $t_{STAHO}$ | 0.5 $t_{SCLO}$ – 1 $t_{cyc}$ | ns | |
| Retransmission start condition output setup time | $t_{STASO}$ | 1 $t_{SCLO}$ | ns | |
| Stop condition output setup time | $t_{STOSO}$ | 0.5 $t_{SCLO}$ + 2 $t_{cyc}$ | ns | |
| Data output setup time (master) | $t_{SDASO}$ | 1 $t_{SCLLO}$ – 3 $t_{cyc}$ | ns | |
| Data output setup time (slave)*1 | | 1 $t_{SCLL}$ – 3 $t_{cyc}$ | ns | |
| Data output setup time (slave)*2 | | 1 $t_{SCLL}$ – (6 $t_{cyc}$ or 12 $t_{cyc}$)*3 | ns | |
| Data output hold time | $t_{SDAHO}$ | 3 $t_{cyc}$ | ns | |

Notes: 1. Not supported by the H8S/2258 Group.
2. Supported only by the H8S/2258 Group.
3. 6 $t_{cyc}$ when IICX is 0, 12 $t_{cyc}$ when IICX is 1.

4. SCL and SDA inputs are sampled in synchronization with the internal clock. The AC timing therefore depends on the system clock cycle $t_{cyc}$, as shown in table 27.22 (H8S/2239 Group) and table 27.34 (H8S/2238B and H8S/2236B). Note that the I²C bus interface AC timing specifications will not be met with a system clock frequency of less than 5 MHz.
5. The I²C bus interface specification for the SCL rise time $t_{sr}$ is under 1000 ns (300 ns for high-speed mode). In master mode, the I²C bus interface monitors the SCL line and synchronizes one bit at a time during communication. If $t_{sr}$ (the time for SCL to go from low to $V_{IH}$) exceeds the time determined by the input clock of the I²C bus interface, the high period of SCL is extended. The SCL rise time is determined by the pull-up resistance and load capacitance of the SCL line. To insure proper operation at the set transfer rate, adjust the pull-up resistance and load capacitance so that the SCL rise time does not exceed the values given in the table in table 16.8.

## 17.5 Operation

The A/D converter operates by successive approximation with 10-bit resolution. It has two operating modes; single mode and scan mode. When changing the operating mode or analog input channel, in order to prevent incorrect operation, first clear the bit ADST to 0 in ADCSR. The ADST bit can be set at the same time as the operating mode or analog input channel is changed.

### 17.5.1 Single Mode

In single mode, A/D conversion is to be performed only once on the specified single channel. The operations are as follows.

1. A/D conversion is started when the ADST bit is set to 1, according to software, timer conversion start trigger, or external trigger input.
2. When A/D conversion is completed, the result is transferred to the corresponding A/D data register to the channel.
3. On completion of conversion, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt request is generated.
4. The ADST bit remains set to 1 during A/D conversion. When A/D conversion ends, the ADST bit is automatically cleared to 0 and the A/D converter enters the wait state.

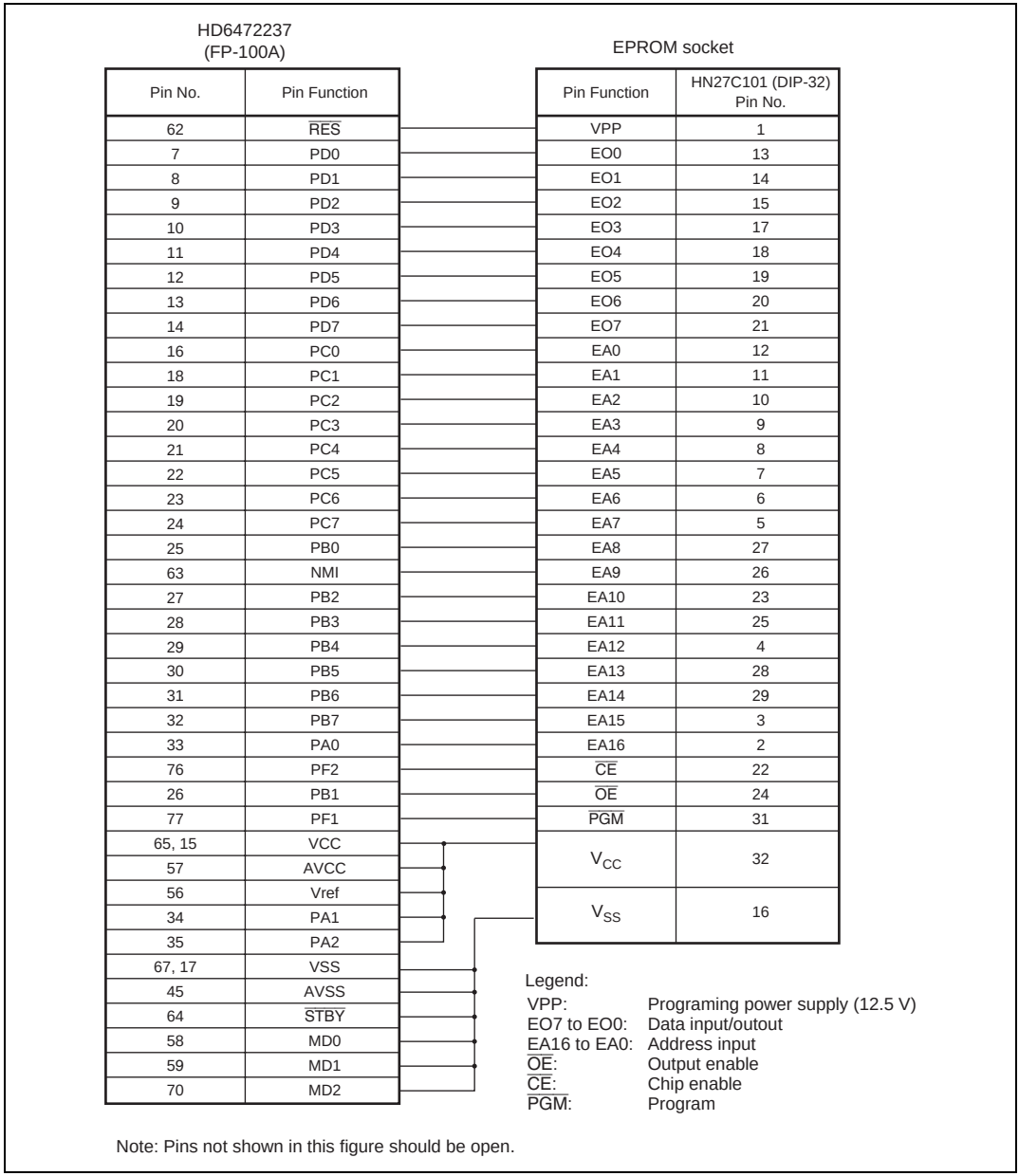



**Figure 22.2 HD6472237 Socket Adapter Pin Correspondence Diagram (FP-100A)**

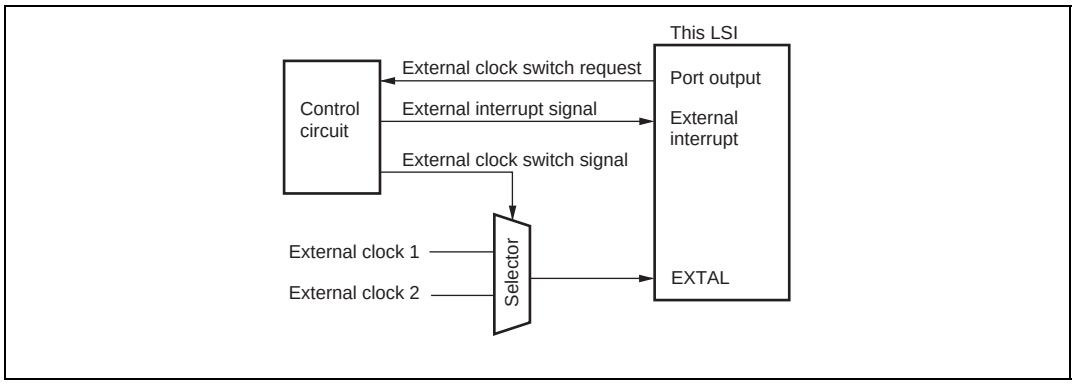
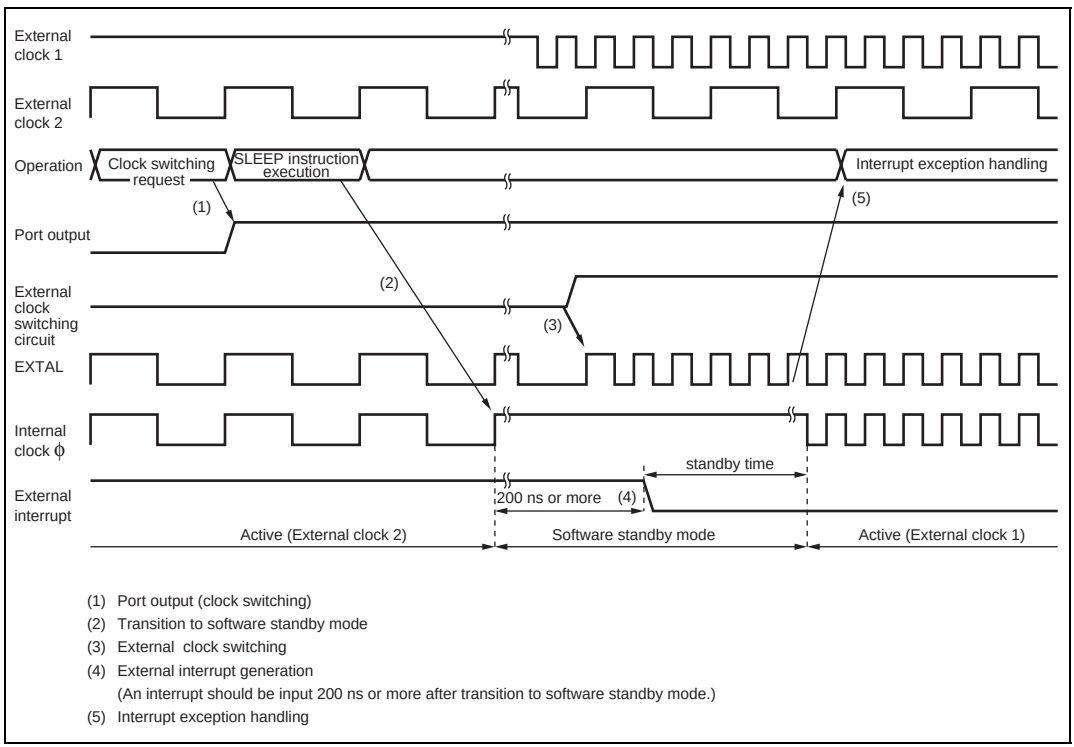



**Figure 23.6 External Clock Switching Circuit (Example)**




(1) Port output (clock switching)
(2) Transition to software standby mode
(3) External clock switching
(4) External interrupt generation
(An interrupt should be input 200 ns or more after transition to software standby mode.)
(5) Interrupt exception handling

**Figure 23.7 External Clock Switching Timing (Example)**

### 27.2.4 A/D Conversion Characteristics

Table 27.10 lists the A/D conversion characteristics.

**Table 27.10 A/D Conversion Characteristics**

Condition A: $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$ = 3.0 V to 3.6 V, $V_{ref}$ = 3.0 V to $AV_{CC}$, $V_{SS}$ = $AV_{SS}$ = 0 V, $\phi$ = 10 to 13.5 MHz, $T_a$ = –20°C to +75°C (regular specifications), $T_a$ = –40°C to +85°C (wide-range specifications)

| | Condition A | | | |
|---|---|---|---|---|
| **Item** | **Min** | **Typ** | **Max** | **Unit** |
| Resolution | 10 | 10 | 10 | bits |
| Conversion time | 9.6 | — | — | µs |
| Analog input capacitance | — | — | 20 | pF |
| Permissible signal-source impedance | — | — | 5 | kΩ |
| Non-linearity error | — | — | ±6.0 | LSB |
| Offset error | — | — | ±4.0 | LSB |
| Full-scale error | — | — | ±4.0 | LSB |
| Quantization error | — | — | ±0.5 | LSB |
| Absolute accuracy | — | — | ±8.0 | LSB |

### 27.2.5 D/A Conversion Characteristics

Table 27.11 lists the D/A conversion characteristics.

**Table 27.11 D/A Conversion Characteristics**

Condition A: $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$ = 4.0 V to 5.5 V, $V_{ref}$ = 4.0 V to $AV_{CC}$, $V_{SS}$ = $AV_{SS}$ = 0 V, $\phi$ = 10 to 13.5 MHz, $T_a$ = –20°C to +75°C (regular specifications), $T_a$ = –40°C to +85°C (wide-range specifications)

| | Condition A | | | | |
|---|---|---|---|---|---|
| **Item** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| Resolution | 8 | 8 | 8 | bits | |
| Conversion time | — | — | 10 | µs | Load capacitance: 20 pF |
| Absolute accuracy | — | ±2.0 | ±3.0 | LSB | Load resistance: 2 MΩ |
| | — | — | ±2.0 | LSB | Load resistance: 4 MΩ |