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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2258fa13iv

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions may occur due to the false recognition of the pin state as an input signal. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

Section 12 8-Bit Timers

Section 13 Watchdog Timer (WDT)

Type	Symbol	Pin No. TFP-100B TFP-100BV TFP-100G TFP-100GV FP-100B FP-100BV	Pin No. FP-100A*3 FP-100AV*3	Pin No. BP-112*1 BP-112V*1 TBP-112A*4 TBP-112AV*4	I/O	Function
8-bit timer	TMO3 to TMO0	88 to 85	91 to 88	A7, A6, B7, C6	Output	Compare-match output pins.
	TMCI23	89	92	B6	Input	Pins for external clock input to the counter.
	TMCI01	90	93	D6		
	TMRI23	89	92	B6	Input	Counter reset input pins.
	TMRI01	90	93	D6		
Watchdog timer (WDT)	BUZZ	74	77	B11	Output	This pin outputs the pulse that is divided by watchdog timer.
Serial communi-cation interface (SCI)/ smart card interface	TxD3	83	86	D7	Output	Data output pins.
	TxD2	31	34	J4		
	TxD1	79	82	A9		
	TxD0	76	79	A10		
	RxD3	84	87	C7	Input	Data input pins.
	RxD2	32	35	K4		
	RxD1	80	83	C8		
	RxD0	77	80	D8		
	SCK3	85	88	A7	Input/ Output	Clock input/output pins. SCK1 outputs NMOS push/pull.
	SCK2	33	36	L4		
	SCK1	81	84	B8		
	SCK0	78	81	B9		
I^2C bus interface (IIC) (optional)	SCL1	79	82	A9	Input/ Output	I^2C clock input/output pins. These pins drive bus. The output of SCL0 is NMOS open drain.
	SCL0	81	84	B8		
	SDA1	78	81	B9	Input/ Output	I^2C data input/output pins. These pins drive bus. The output of SDA0 is NMOS open drain.
	SDA0	80	83	C8		
A/D converter	AN7 to AN0	52 to 45	55 to 48	L10, L9, K11, K10, K9, K8, J8, H7	Input	Analog input pins for the A/D converter.
	$\overline{\text{ADTRG}}$	72	75	D9	Input	Pin for input of an external trigger to start A/D conversion.

2.2 CPU Operating Modes

The H8S/2000 CPU has two operating modes: normal and advanced. Normal mode supports a maximum 64-kbyte address space. Advanced mode supports a maximum 16-Mbyte total address space. The mode is selected by the mode pins.

2.2.1 Normal Mode

In normal mode, the exception vector table and stack have the same structure as the H8/300 CPU.

- Address Space

  Linear access is provided to a maximum address space of 64 kbytes.
- Extended Registers (En)

  The extended registers (E0 to E7) can be used as 16-bit registers, or as the upper 16-bit segments of 32-bit registers. When En is used as a 16-bit register it can contain any value, even when the corresponding general register (Rn) is used as an address register. If the general register is referenced in the register indirect addressing mode with pre-decrement (@–Rn) or post-increment (@Rn+) and a carry or borrow occurs, however, the value in the corresponding extended register (En) will be affected.
- Instruction Set

  All instructions and addressing modes can be used. Only the lower 16 bits of effective addresses (EA) are valid.
- Exception Vector Table and Memory Indirect Branch Addresses

  In normal mode the top area starting at H'0000 is allocated to the exception vector table. One branch address is stored per 16 bits. Figure 2.1 shows the structure of the exception vector table in normal mode. For details of the exception vector table, see section 4, Exception Handling.

  The memory indirect addressing mode (@@aa:8) employed in the JMP and JSR instructions uses an 8-bit absolute address included in the instruction code to specify a memory operand that contains a branch address. In normal mode the operand is a 16-bit word operand, providing a 16-bit branch address. Branch addresses can be stored in the top area from H'0000 to H'00FF. Note that this area is also used for the exception vector table.
- Stack Structure

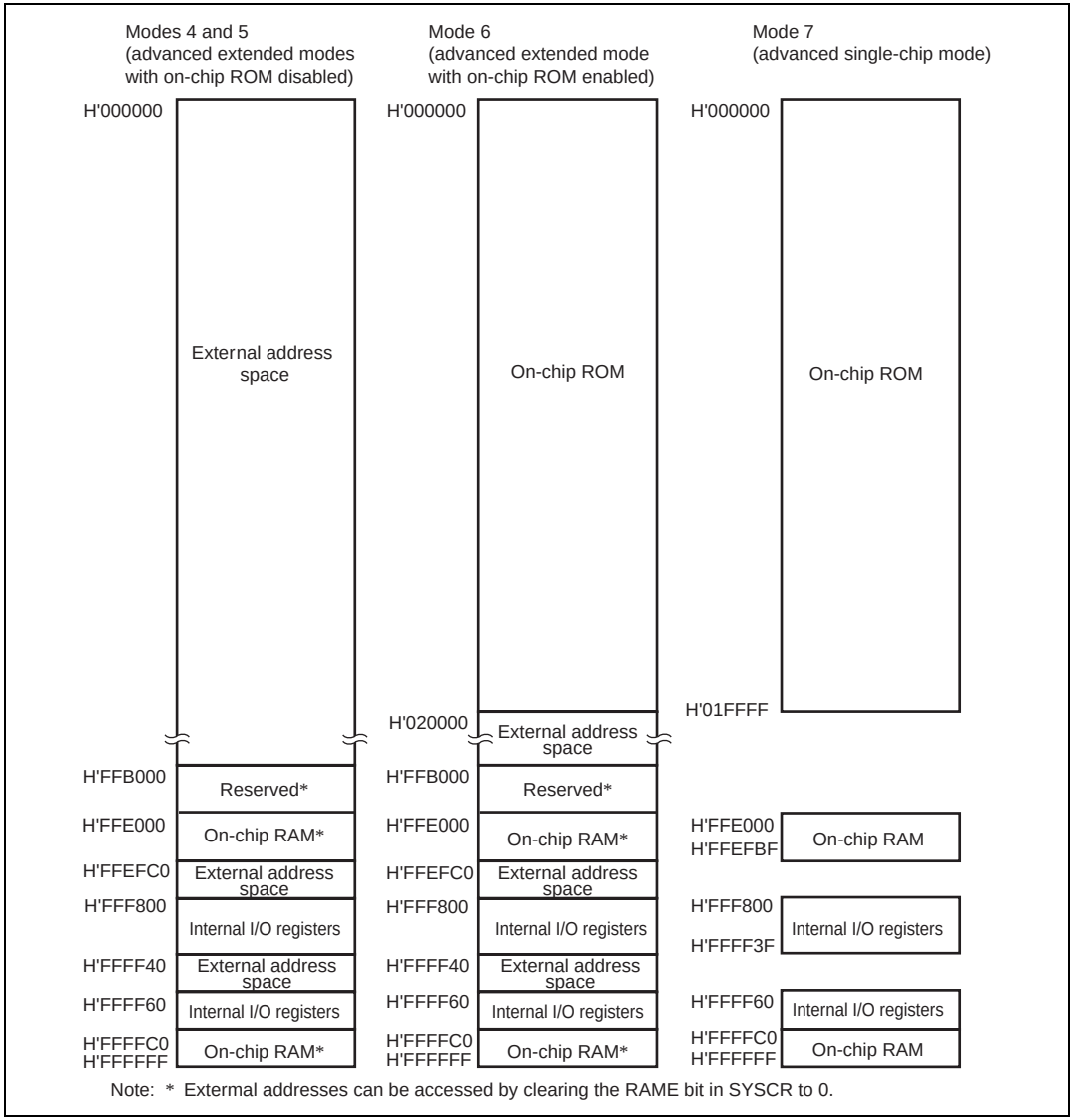
  In normal mode, when the program counter (PC) is pushed onto the stack in a subroutine call, and the PC, condition-code register (CCR) and extended control register (EXR) are pushed onto the stack in exception handling, they are stored as shown in figure 2.2. EXR is not pushed onto the stack in interrupt control mode 0. For details, see section 4, Exception Handling.

Note: Normal mode is not available in this LSI.

Table 2.3 Data Transfer Instructions

Instruction	Size*1	Function
MOV	B/W/L	(EAs) → Rd, Rs → (EAd) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register.
MOVFPE	B	Cannot be used in this LSI.
MOVTPE	B	Cannot be used in this LSI.
POP	W/L	@SP+ → Rn Pops a general register from the stack. POP.W Rn is identical to MOV.W @SP+, Rn. POP.L ERn is identical to MOV.L @SP+, ERn.
PUSH	W/L	Rn → @–SP Pushes a general register onto the stack. PUSH.W Rn is identical to MOV.W Rn, @–SP. PUSH.L ERn is identical to MOV.L ERn, @–SP.
LDM*2	L	@SP+ → Rn (register list) Pops two or more general registers from the stack.
STM*2	L	Rn (register list) → @–SP Pushes two or more general registers onto the stack.

Notes: 1. Refers to the operand size.
B: Byte
W: Word
L: Longword
2. Only register ER0 to ER6 should be used when using the STM/LDM instruction.



Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 3.7 H8S/2235 and H8S/2225 Memory Map in Each Operating Mode

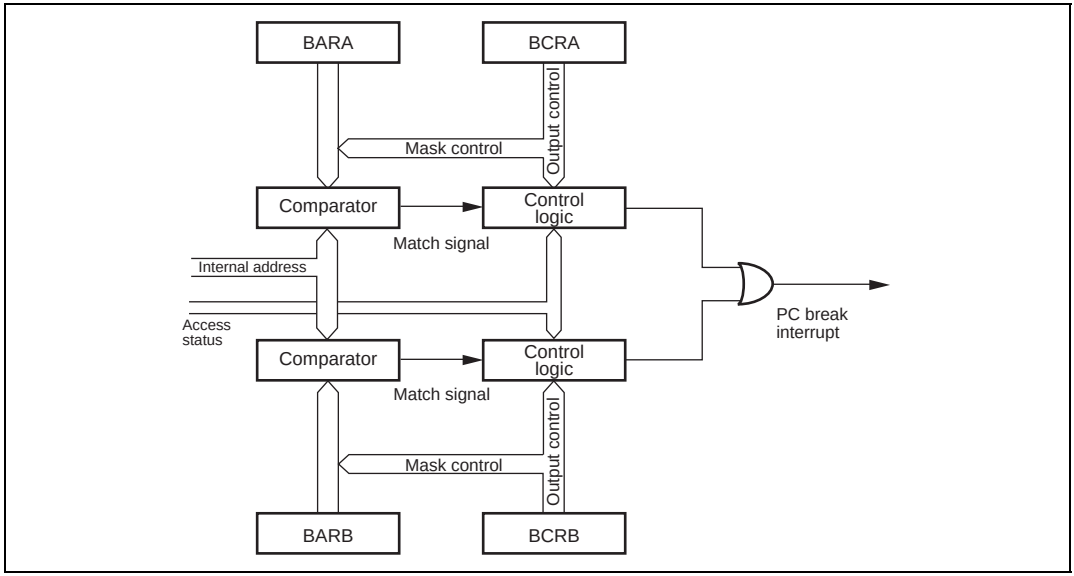


Figure 6.1 Block Diagram of PC Break Controller

6.2 Register Descriptions

The PC break controller has the following registers.

- Break address register A (BARA)
- Break address register B (BARB)
- Break control register A (BCRA)
- Break control register B (BCRB)

6.2.1 Break Address Register A (BARA)

BARA is a 32-bit readable/writable register that specifies the channel A break address.

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	Undefined	—	Reserved These bits are read as an undefined value and cannot be modified.
23 to 0	BAA23 to BAA0	All 0	R/W	Break Address 23 to 0 These bits set the channel A PC break address.

7.2 Input/Output Pins

Table 7.1 summarizes the pins of the bus controller.

Table 7.1 Pin Configuration

Name	Symbol	I/O	Function
Address strove	$\overline{AS}$	Output	Strobe signal indicating that address output on address bus is enabled.
Read	$\overline{RD}$	Output	Strobe signal indicating that external space is being read.
High write	$\overline{HWR}$	Output	Strobe signal indicating that external space is to be written, and upper half (D15 to D8) of data bus is enabled.
Low write	$\overline{LWR}$	Output	Strobe signal indicating that external space is to be written, and lower half (D7 to D0) of data bus is enabled.
Chip select 7 to 0	$\overline{CS7}$ to $\overline{CS0}$	Output	Strobe signal indicating that areas 7 to 0 are selected.
Wait	$\overline{WAIT}$	Input	Wait request signal when accessing external 3-state access space.
Bus request	$\overline{BREQ}$	Input	Request signal that releases bus to external device.
Bus request acknowledge	$\overline{BACK}$	Output	Acknowledge signal indicating that bus has been released.

7.3 Register Descriptions

The following shows the registers of the bus controller.

- Bus width control register (ABWCR)
- Access state control register (ASTCR)
- Wait control register H (WCRH)
- Wait control register L (WCRL)
- Bus control register H (BCRH)
- Bus control register L (BCRL)
- Pin function control register (PFCR)

ETCRB is decremented by 1 after every block transfer, and when the count reaches H'0000 the DTE bit in DMABCRL is cleared and transfer ends. If the DTIE bit in DMABCRL is set to 1 at this point, an interrupt request is sent to the CPU or DTC.

Figure 8.16 shows the operation flow in block transfer mode.

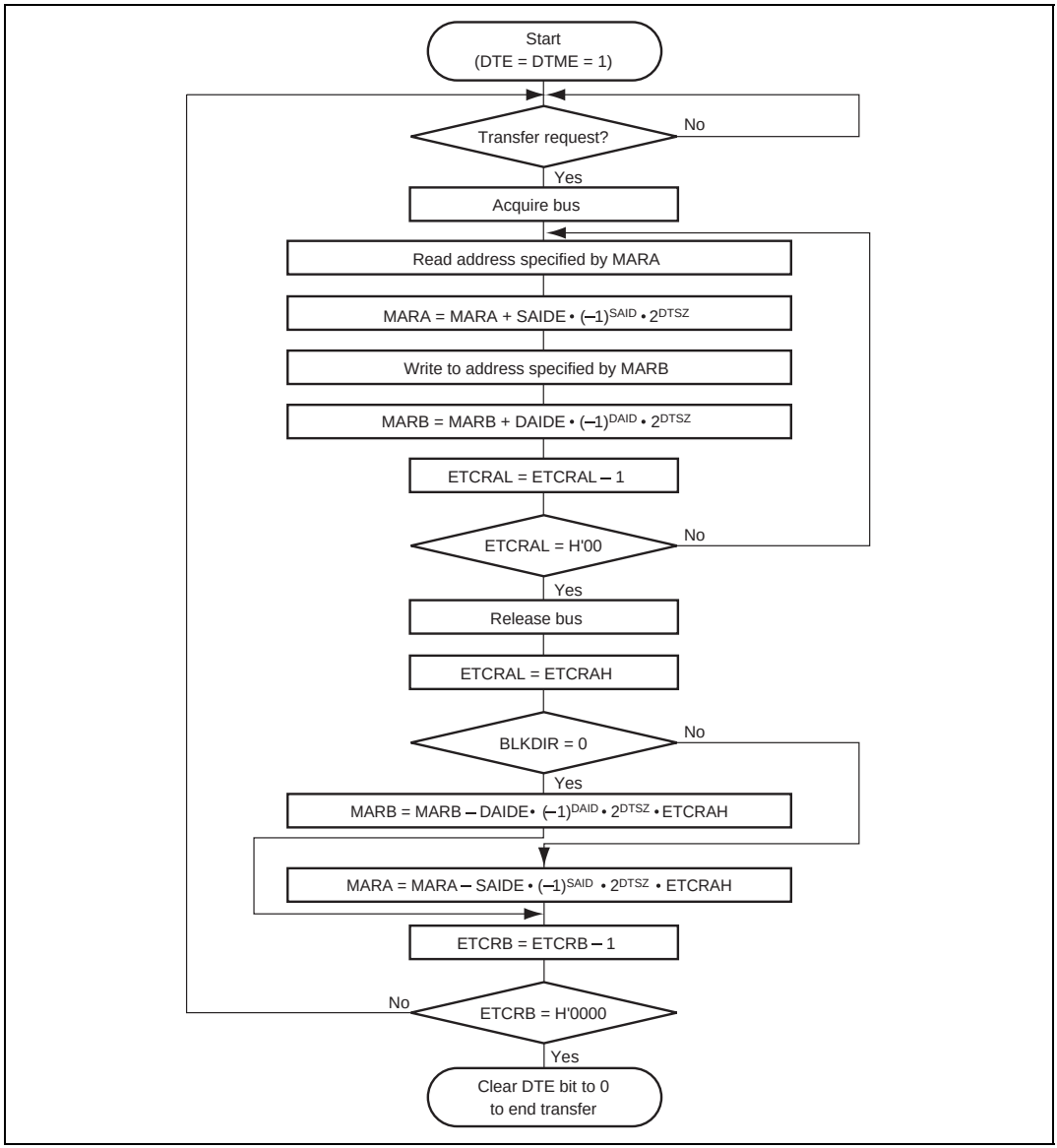


Figure 8.16 Operation Flow in Block Transfer Mode

8.5.10 DMA Transfer (Single Address Mode) Bus Cycles

Single Address Mode (Read): Figure 8.27 shows a transfer example in which $\overline{\text{TEND}}$ output is enabled and byte-size single address mode transfer (read) is performed from external 8-bit, 2-state access space to an external device.

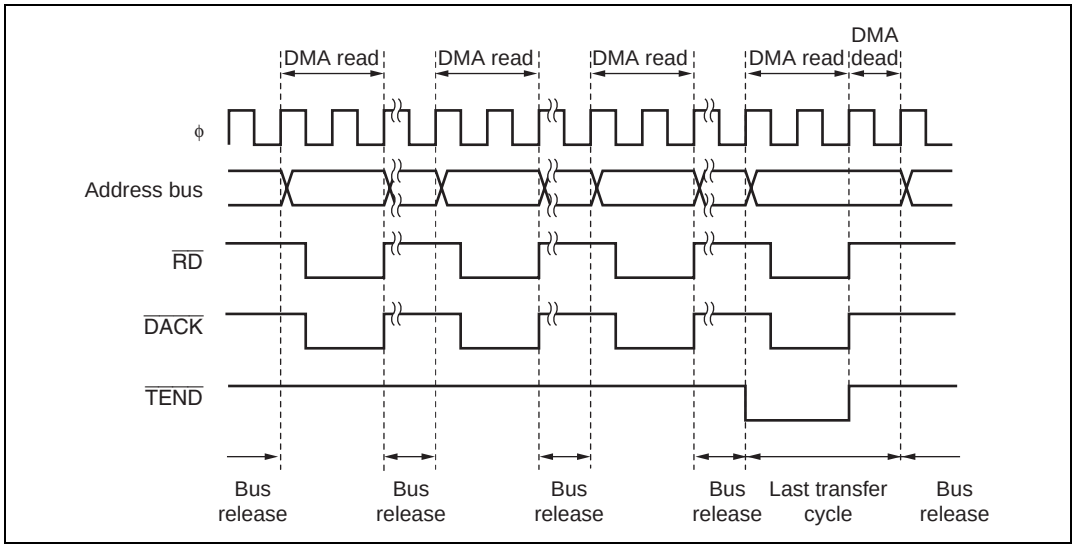


Figure 8.27 Example of Single Address Mode Transfer (Byte Read)

9.5 Operation

Register information is stored in on-chip RAM. When activated, the DTC reads register information in on-chip RAM and transfers data. After the data transfer, the DTC writes updated register information back to the memory.

The pre-storage of register information in memory makes it possible to transfer data over any required number of channels. The transfer mode can be specified as normal, repeat, and block transfer mode. Setting the CHNE bit in MRB to 1 makes it possible to perform a number of transfers with a single activation source (chain transfer).

The 24-bit SAR designates the DTC transfer source address, and the 24-bit DAR designates the transfer destination address. After each transfer, SAR and DAR are independently incremented, decremented, or left fixed depending on its register information.

Figure 9.5 shows the flowchart of DTC operation.

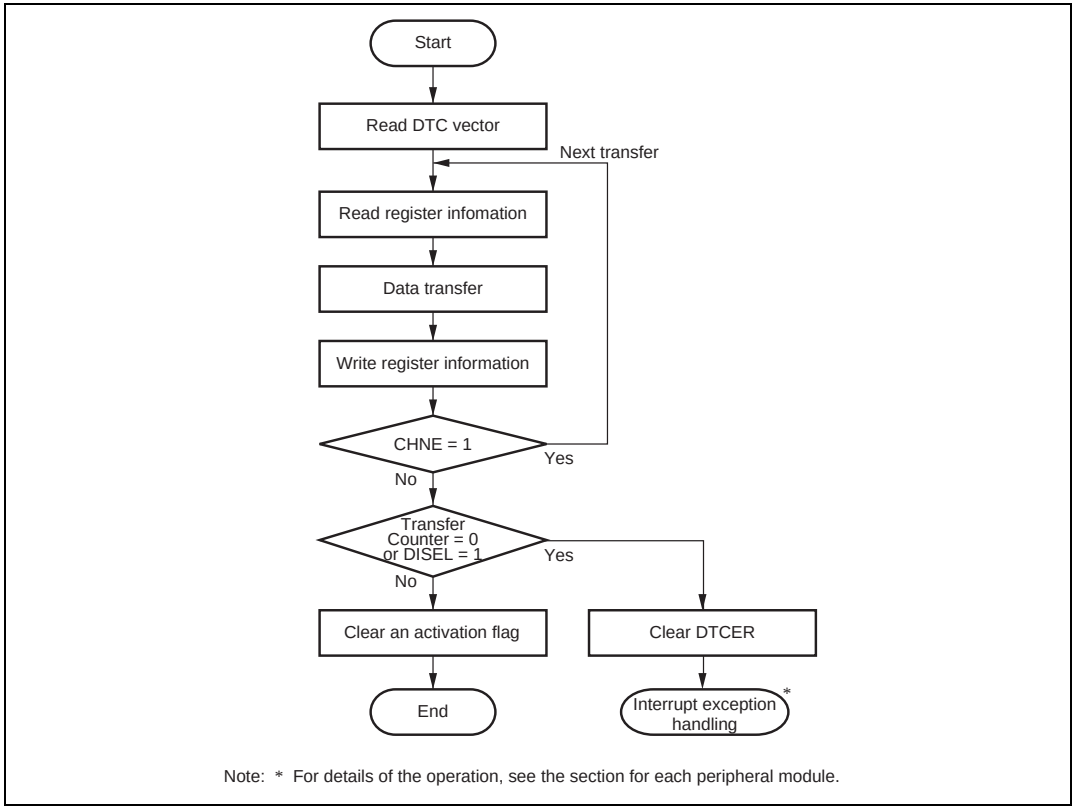


Figure 9.5 Flowchart of DTC Operation

Table 11.26 TIOR_4

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_4 Function***	**TIOCA4 Pin Function***
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCA4 pin Input capture at rising edge
			1		Capture input source is TIOCA4 pin Input capture at falling edge
		1	×		Capture input source is TIOCA4 pin Input capture at both edges
	1	×	×		Capture input source is TGRA_3 compare match/input capture Input capture at generation of TGRA_3 compare match/input capture

Legend: ×: Don't care

Note: * Not available in the H8S/2227 Group.

11.10.9 Contention between TGR Write and Input Capture

If the input capture signal is generated in the T_2 state of a TGR write cycle, the input capture operation takes precedence and the write to TGR is not performed.

Figure 11.51 shows the timing in this case.

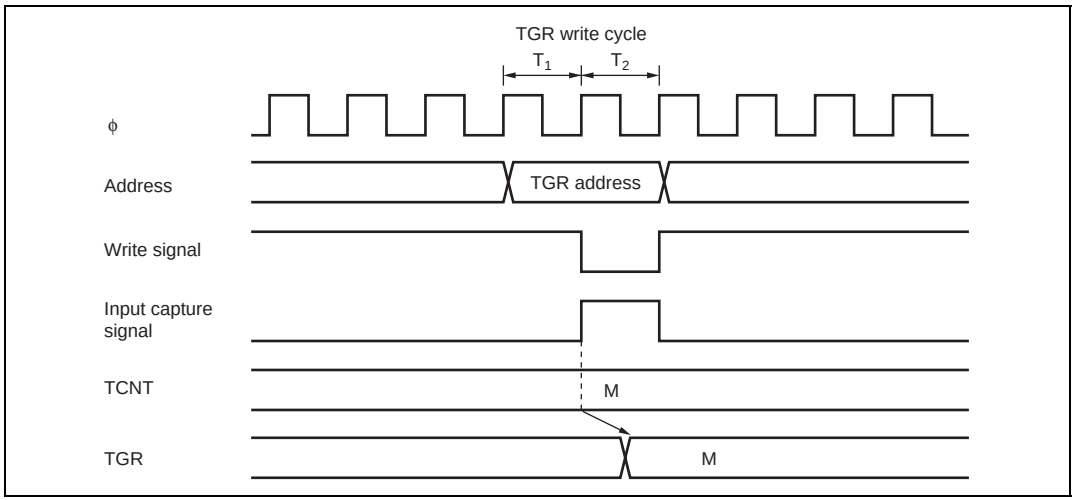


Figure 11.51 Contention between TGR Write and Input Capture

11.10.10 Contention between Buffer Register Write and Input Capture

If the input capture signal is generated in the T_2 state of a buffer register write cycle, the buffer operation takes precedence and the write to the buffer register is not performed.

Figure 11.52 shows the timing in this case.

- Programmer mode

  Flash memory can be programmed/erased in programmer mode using a PROM programmer, as well as in on-board programming mode.
- Emulation function for flash memory in RAM

  The real-time emulation for programming of flash memory is possible by overlapping the flash memory to a part of RAM.

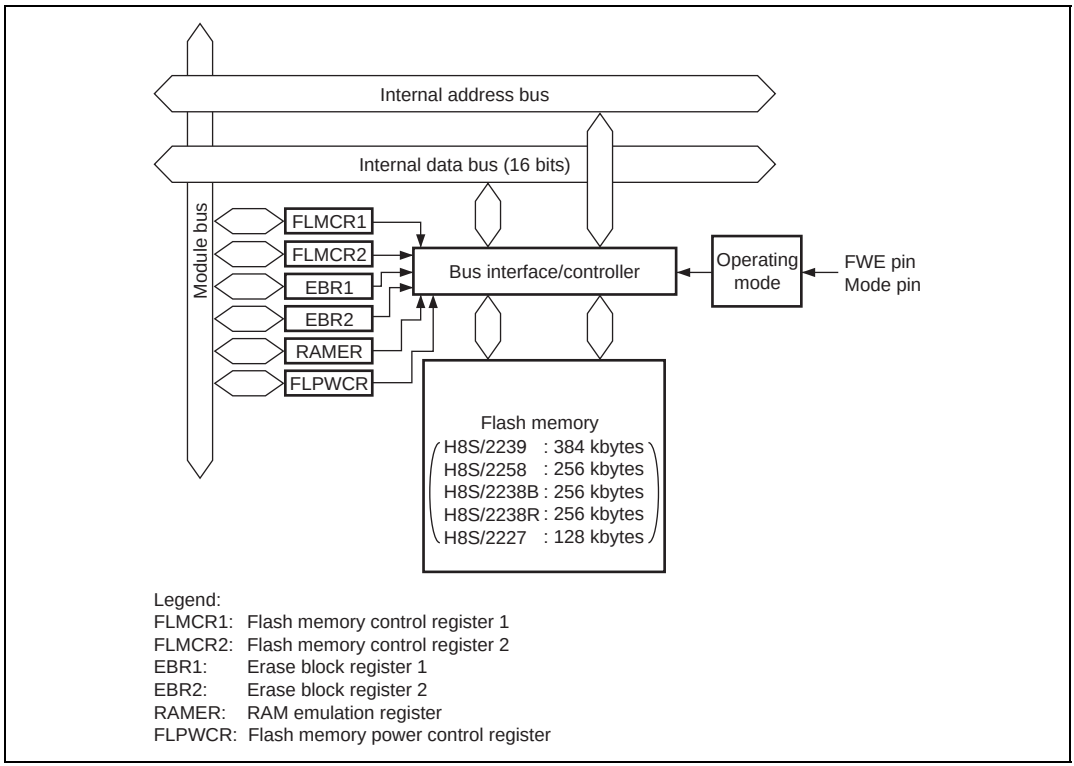


Figure 20.1 Block Diagram of Flash Memory

20.2 Mode Transitions

When the mode pins and the FWE pin are set in the reset state and a reset-start is executed, this LSI enters an operating mode as shown in figure 20.2. In user mode, flash memory can be read but not programmed or erased.

The boot, user program and programmer modes are provided as modes to write and erase the flash memory.

20.5.6 Flash Memory Power Control Register (FLPWCR)

FLPWCR enables/disables transition to power-down modes for the flash memory when this LSI enters sub-active mode.

Bit	Bit Name	Initial Value	R/W	Description
7	PDWND	0	R/W	Power Down Disable Enables/disables transition to power-down modes for the flash memory when this LSI enters sub-active mode. 0: Transition to power-down modes for the flash memory enabled. 1: Transition to power-down modes for the flash memory disabled.
6 to 0	—	All 0	R	Reserved These bits are always read as 0.

20.5.7 Serial Control Register X (SCRX)

SCRX performs register access control.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved Only 0 should be written to this bit.
6	IICX1	0	R/W	I^2C Transfer Select 1, 0
5	IICX0	0	R/W	For details, see section 16.3.5, Serial Control Register X (SCRX).
4	IICE	0	R/W	I^2C Master Enable For details, see section 16.3.5, Serial Control Register X (SCRX).

20.8.2 Erase/Erase-Verify

When erasing flash memory, the erase/erase-verify flowchart shown in figure 20.12 should be followed.

1. Prewriting (setting erase block data to all 0) is not necessary.
2. Erasing is performed in block units. Make only a single-bit specification in the erase block register 1 and 2 (EBR1 and EBR2). To erase multiple blocks, each block must be erased in turn.
3. The time during which the E1 bit is set to 1 is the flash memory erase time.
4. The watchdog timer (WDT) is set to prevent overprogramming due to program runaway, etc. Set a value greater than ($t_{sesu} + t_{se} + t_{ce} + t_{cesu}$) ms as the WDT overflow period.
5. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower 1 bit are B'0. Verify data can be read in words from the address to which a dummy write was performed.
5. If the read data is not erased successfully, set erase mode again, and repeat the erase/erase-verify sequence as before. The maximum number of repetitions of the erase/erase-verify sequence is (N).

Table 27.22 I²C Bus Timing

Conditions: V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0 V, ϕ = 5 MHz to maximum operating frequency, T_a = –20°C to +75°C

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
SCL input cycle time	t_{SCL}	12 t_{cyc}	—	—	ns	Figure 27.34
SCL input high pulse width	t_{SCLH}	3 t_{cyc}	—	—	ns	
SCL input low pulse width	t_{SCLL}	5 t_{cyc}	—	—	ns	
SCL, SDA input rise time	t_{Sr}	—	—	7.5 t_{cyc}*	ns	
SCL, SDA input fall time	t_{Sf}	—	—	300	ns	
SCL, SDA input spike pulse delete time	t_{SP}	—	—	1 t_{cyc}	ns	
SDA input bus free time	t_{BUF}	5 t_{cyc}	—	—	ns	
Operating condition input hold time	t_{STAH}	3 t_{cyc}	—	—	ns	
Retransmitting operating condition input setup time	t_{STAS}	3 t_{cyc}	—	—	ns	
Stop condition input setup time	t_{STOS}	3 t_{cyc}	—	—	ns	
Data input setup time	t_{SDAS}	0.5 t_{cyc}	—	—	ns	
Data input hold time	t_{SDAH}	0	—	—	ns	
SCL, SDA capacitor load	C_b	—	—	400	pF	

Note: * Maximum SCL and SDA input rise time 7.5 t_{cyc} or 17.5 t_{cyc} can be selected depending on the clock that is used in the I²C module. For detail, see section 16.6, Usage Notes.

(4) Timing of On-Chip Peripheral Modules

Table 27.45 lists the timing of on-chip peripheral modules. Table 27.46 lists the I^2C bus timing.

Table 27.45 Timing of On-Chip Peripheral Modules

Condition A (F-ZTAT version and masked ROM version):
V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V,
V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ϕ = 32.768 kHz, 2 to 13.5 MHz,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Condition B (F-ZTAT version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V,
V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ϕ = 32.768 kHz, 2 to 6.25 MHz,
T_a = –20°C to +75°C (regular specifications)

Condition C (Masked ROM version): V_{CC} = 2.2 V to 3.6 V, AV_{CC} = 2.2 V to 3.6 V,
V_{ref} = 2.2 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V,
ϕ = 32.768 kHz, 2 to 6.25 MHz,
T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

				Condition A		Conditions B, C			Test
Item			**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
I/O port*	Output data delay time		t_{PWD}	—	100	—	150	ns	Figure 27.24
	Input data setup time		t_{PRS}	50	—	80	—		
	Input data hold time		t_{PRH}	50	—	80	—		
TPU	Timer output delay time		t_{TOCD}	—	100	—	150	ns	Figure 27.25
	Timer input setup time		t_{TICS}	40	—	60	—		
	Timer clock input setup time		t_{TCKS}	40	—	60	—	ns	Figure 27.26
	Timer clock pulse width	Single edge	t_{TCKWH}	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{TCKWL}	2.5	—	2.5	—		
TMR	Timer output delay time		t_{TMOD}	—	100	—	150	ns	Figure 27.27
	Timer reset input setup time		t_{TMRS}	50	—	80	—	ns	Figure 27.29
	Timer clock input setup time		t_{TMCS}	50	—	80	—	ns	Figure 27.28

Item	Symbol	Condition A		Condition B		Condition C		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	1000	—	µs	Figure 27.11
Subclock oscillation stabilization time	t_{OSC3}	—	2	—	2	—	3	s	
Subclock oscillator frequency	f_{SUB}	32.768	32.768	32.768	32.768	32.768	32.768	kHz	
Subclock (ϕ_{SUB}) cycle time	t_{SUB}	30.5	30.5	30.5	30.5	30.5	30.5	µs	