Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2258fa13v

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

User's Manuals for Development Tools:

Document Title	Document No.
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimized Linkage Editor User's Manual	REJ10J2039
High-performance Embedded Workshop User's Manual	REJ10J2037

Application Notes:

Document Title	Document No.
H8S, H8/300 Series C/C++ Compiler Package Application Note	REJ05B0464

Section 12 8-Bit Timers

Section 13 Watchdog Timer (WDT)

Pin No.		Pin Name				
TFP-100B TFP-100BV TFP-100G TFP-100GV FP-100B[*1] FP-100BV[*1]	FP-100A[*2] FP-100AV[*2]	Mode 4	Mode 5	Mode 6	Mode 7	Flash Memory Programmable Mode[*3]
43	46	P97	P97	P97	P97	NC
44	47	P96	P96	P96	P96	NC
45	48	P47/AN7	P47/AN7	P47/AN7	P47/AN7	NC
46	49	P46/AN6	P46/AN6	P46/AN6	P46/AN6	NC
47	50	P45/AN5	P45/AN5	P45/AN5	P45/AN5	NC
48	51	P44/AN4	P44/AN4	P44/AN4	P44/AN4	NC
49	52	P43/AN3	P43/AN3	P43/AN3	P43/AN3	NC
50	53	P42/AN2	P42/AN2	P42/AN2	P42/AN2	NC
51	54	P41/AN1	P41/AN1	P41/AN1	P41/AN1	NC
52	55	P40/AN0	P40/AN0	P40/AN0	P40/AN0	NC
53	56	Vref	Vref	Vref	Vref	VCC
54	57	AVCC	AVCC	AVCC	AVCC	VCC
55	58	MD0	MD0	MD0	MD0	VSS
56	59	MD1	MD1	MD1	MD1	VSS
57	60	OSC2	OSC2	OSC2	OSC2	NC
58	61	OSC1	OSC1	OSC1	OSC1	VSS
59	62	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
60	63	NMI	NMI	NMI	NMI	VCC
61	64	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	VCC
62	65	VCC	VCC	VCC	VCC	VCC
63	66	XTAL	XTAL	XTAL	XTAL	XTAL
64	67	VSS	VSS	VSS	VSS	VSS
65	68	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL
66	69	FWE	FWE	FWE	FWE	FWE
67	70	MD2	MD2	MD2	MD2	VSS
68	71	PF7/ϕ	PF7/ϕ	PF7/ϕ	PF7/ϕ	NC
69	72	$\overline{\text{AS}}$	$\overline{\text{AS}}$	$\overline{\text{AS}}$	PF6	NC
70	73	$\overline{\text{RD}}$	$\overline{\text{RD}}$	$\overline{\text{RD}}$	PF5	NC

		Pin No.				
		TFP-100B TFP-100BV TFP-100G TFP-100GV FP-100B	FP-100A*3	BP-112*1 BP-112V*1 TBP-112A*4		
Type	Symbol	FP-100BV	FP-100AV*3	TBP-112AV*4	I/O	Function
Address bus	A23 to A0	37 to 15, 13	40 to 18, 16	L5, L4, L3, L2, K5, K4, K3, K2, K1, J5, J4, J3, J2, J1, H5, H4, H3, H2, H1, G4, G3, G2, G1, F1	Output	Outputs Address.
Data bus	D15 to D0	100 to 96, 11 to 1	100, 99, 14 to 1	E4, E3, E1, D4, D3, D2, D1, C4, C2, C1, B4, B3, B2, B1, A3, A2	Input/ output	Used as the bidirectional data bus.
Bus control	$\overline{CS7}$	87	90	C6	Output	Select signals for areas 7 to 0.
	$\overline{CS6}$	88	91	A6		
	$\overline{CS5}$	89	92	B6		
	$\overline{CS4}$	90	93	D6		
	$\overline{CS3}$	92	95	B5		
	$\overline{CS2}$	93	96	C5		
	$\overline{CS1}$	94	97	A4		
	$\overline{CS0}$	95	98	D5		
	$\overline{AS}$	69	72	E8	Output	When this pin is low, it indicates valid address output on the address bus.
	$\overline{RD}$	70	73	D10	Output	When this pin is low, it indicates that the external address space is being read.
	$\overline{HWR}$	71	74	C11	Output	Strobe signal: Writes to the external address bus to indicate valid data on the upper data bus (D15 to D8).
	$\overline{LWR}$	72	75	D9	Output	Strobe signal: Writes to the external bus to indicate valid data on the lower data bus (D7 to D0).
	$\overline{WAIT}$	73	76	C10	Input	Requests insertion of wait states in bus cycle when accesses to the external three-state address.

7.3.4 Bus Control Register H (BCRH)

BCRH selects enabling or disabling of idle cycle insertion, and the memory interface for area 0.

Bit	Bit Name	Initial Value	R/W	Description
7	ICIS1	1	R/W	Idle Cycle Insert 1 Selects whether or not one idle cycle state is to be inserted between bus cycles when successive external read cycles are performed in different areas. 0: Idle cycle not inserted in case of successive external read cycles in different areas 1: Idle cycle inserted in case of successive external read cycles in different areas
6	ICIS0	1	R/W	Idle Cycle Insert 0 Selects whether or not one idle cycle state is to be inserted between bus cycles when successive external read and write cycles are performed. 0: Idle cycle not inserted in case of successive external read and write cycles 1: Idle cycle inserted in case of successive external read and write cycles
5	BRSTRM	0	R/W	Burst ROM enable Selects whether area 0 is used as a burst ROM interface. 0: Area 0 is basic bus interface 1: Area 0 is burst ROM interface
4	BRSTS1	1	R/W	Burst Cycle Select 1 Selects the number of burst cycles for the burst ROM interface. 0: Burst cycle comprises 1 state 1: Burst cycle comprises 2 states
3	BRSTS0	0	R/W	Burst Cycle Select 0 Selects the number of words that can be accessed in a burst ROM interface burst access. 0: Max. 4 words in burst access 1: Max. 8 words in burst access
2 to 0	—	All 0	R/W	Reserved The write value should always be 0.

Single Address Mode (Write): Figure 8.29 shows a transfer example in which $\overline{\text{TEND}}$ output is enabled and byte-size single address mode transfer (write) is performed from an external device to external 8-bit, 2-state access space.

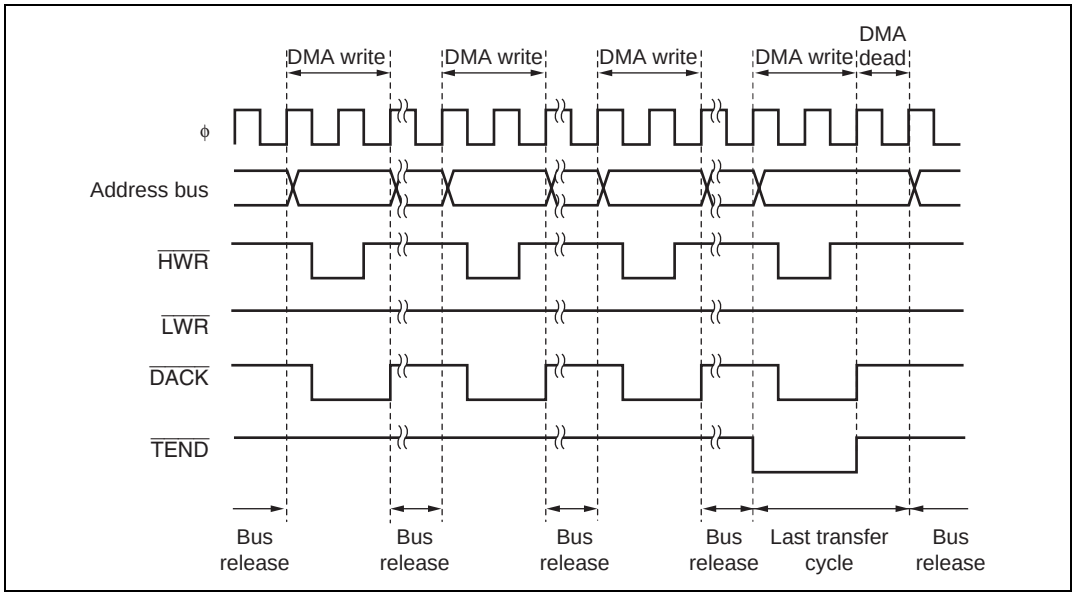


Figure 8.29 Example of Single Address Mode Transfer (Byte Write)

9.2.8 DTC Vector Register (DTVECR)

DTVECR is an 8-bit readable/writable register that enables or disables DTC activation by software, and sets a vector number for the software activation interrupt.

Bit	Bit Name	Initial Value	R/W	Description
7	SWDTE	0	R/W	DTC Software Activation Enable Enables or disables the DTC software activation. 0: Disables the DTC software activation. 1: Enables the DTC software activation. [Clearing conditions] • When the DISEL bit is 0 and the specified number of transfers have not ended • When 0 is written to the DISEL bit after a software-activated data transfer end interrupt (SWDTEND) request has been sent to the CPU. [Retaining conditions] • When the DISEL bit is 1 and data transfer has ended • When the specified number of transfers have ended • When the software-activated data transfer is in process
6	DTVEC6	0	R/W	DTC Software Activation Vectors 0 to 6 These bits specify a vector number for DTC software activation. The vector address is expressed as H'0400 + (vector number × 2). For example, when DTVEC6 to DTVEC0 = H'10, the vector address is H'0420. These bits are writable when SWDTE = 0.
5	DTVEC5	0	R/W	
4	DTVEC4	0	R/W	
3	DTVEC3	0	R/W	
2	DTVEC2	0	R/W	
1	DTVEC1	0	R/W	
0	DTVEC0	0	R/W	

10.1.2 Port 1 Data Register (P1DR)

P1DR stores output data for port 1 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P17DR	0	R/W	Output data for a pin is stored when the pin is specified as a general purpose output port.
6	P16DR	0	R/W	
5	P15DR	0	R/W	
4	P14DR	0	R/W	
3	P13DR	0	R/W	
2	P12DR	0	R/W	
1	P11DR	0	R/W	
0	P10DR	0	R/W	

10.1.3 Port 1 Register (PORT1)

PORT1 shows the pin states. This register cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	P17	—*	R	If a port 1 read is performed while P1DDR bits are set to 1, the P1DR values are read. If a port 1 read is performed while P1DDR bits are cleared to 0, the pin states are read.
6	P16	—*	R	
5	P15	—*	R	
4	P14	—*	R	
3	P13	—*	R	
2	P12	—*	R	
1	P11	—*	R	
0	P10	—*	R	

Note: * Determined by the states of pins P17 to P10.

10.2.4 Port 3 Open Drain Control Register (P3ODR)

P3ODR controls on/off state of the PMOS for port 3 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	—	Undefined	—	Reserved These bits are always read as undefined value.
6	P36ODR	0	R/W	When each of P36ODR and P33ODR to P30ODR bits is set to 1, the corresponding pins P36 and P33 to P30 function as NMOS open drain outputs. When cleared to 0, the corresponding pins function as CMOS outputs. When each of P35ODR and P34ODR bits is set to 1, the corresponding pins P35 and P34 function as open drain outputs. When they are cleared to 0, the corresponding pins function as NMOS push pull outputs.*
5	P35ODR	0	R/W	
4	P34ODR	0	R/W	
3	P33ODR	0	R/W	
2	P32ODR	0	R/W	
1	P31ODR	0	R/W	
0	P30ODR	0	R/W	

Note: * When they are cleared to 0, the corresponding pins function as CMOS outputs in the H8S/2237 Group and H8S/2227 Group.

10.2.5 Pin Functions

The port 3 pins also function as SCI I/O input pins, I2C bus interface* I/O pins, and as external interrupt input pins.

As shown in figure 10.1, when the pins P35, P34, SCK1, SCL0, or SDA0 type open drain output is used, a bus line is not affected even if the power supply for this LSI fails. Use (a) type open drain output when using a bus line having a state in which the power is not supplied to this LSI.

Note: * The I^2C bus interface is not available in the H8S/2237 Group and H8S/2227 Group.

Table 11.12 TIORH_0

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_0 Function**	**TIOCB0 Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCB0 pin Input capture at rising edge
			1		Capture input source is TIOCB0 pin Input capture at falling edge
		1	×		Capture input source is TIOCB0 pin Input capture at both edges
	1	×	×		Capture input source is channel 1/count clock Input capture at TCNT_1 count- up/count-down*1*2

Legend: ×: Don't care

Notes: 1. When bits TPSC2 to TPSC0 in TCR_1 are set to B'000 and φ/1 is used as the TCNT_1 count clock, this setting is invalid and input capture is not generated.

2. Not available in the H8S/2227 Group.

For details on PWM modes, see section 11.4.5, PWM Modes.

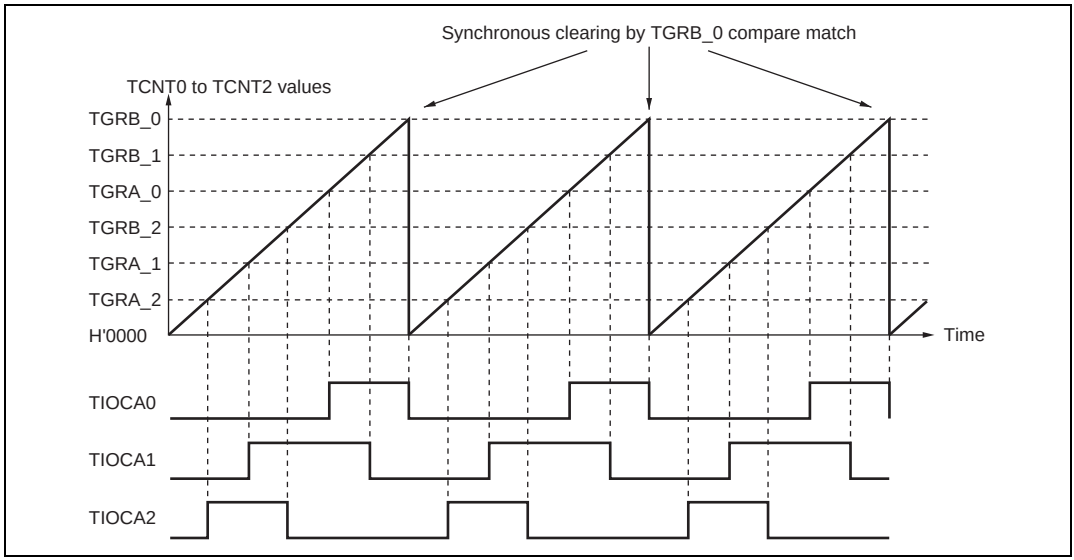


Figure 11.12 Example of Synchronous Operation

11.4.3 Buffer Operation

Buffer operation, provided for channels 0 and 3, enables TGRC and TGRD to be used as buffer registers.

Buffer operation differs depending on whether TGR has been designated as an input capture register or a compare match register.

Table 11.28 shows the register combinations used in buffer operation.

Table 11.28 Register Combinations in Buffer Operation

Channel	Timer General Register	Buffer Register
0	TGRA_0	TGRC_0
	TGRB_0	TGRD_0
3*	TGRA_3	TGRC_3
	TGRB_3	TGRD_3

Note: * Not available in the H8S/2227 Group.

11.10.9 Contention between TGR Write and Input Capture

If the input capture signal is generated in the T_2 state of a TGR write cycle, the input capture operation takes precedence and the write to TGR is not performed.

Figure 11.51 shows the timing in this case.

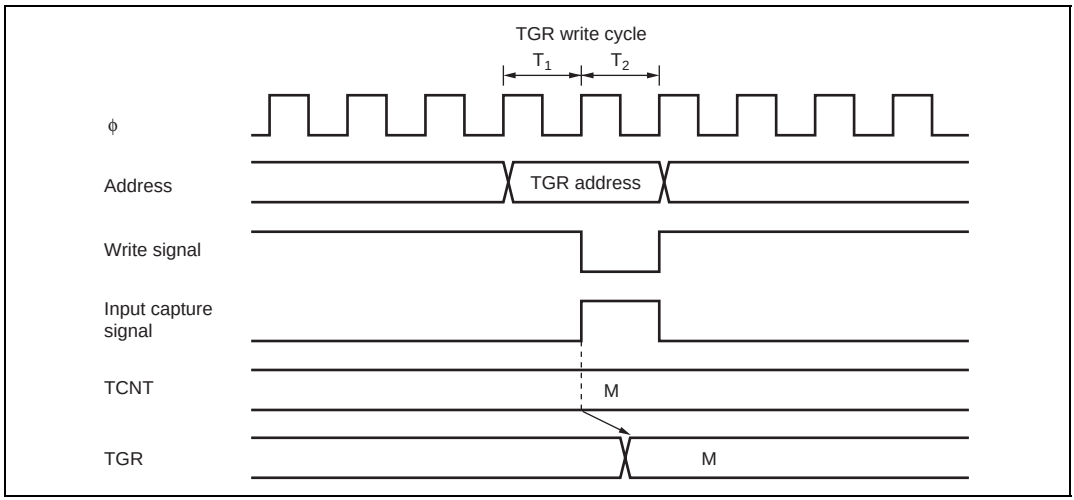


Figure 11.51 Contention between TGR Write and Input Capture

11.10.10 Contention between Buffer Register Write and Input Capture

If the input capture signal is generated in the T_2 state of a buffer register write cycle, the buffer operation takes precedence and the write to the buffer register is not performed.

Figure 11.52 shows the timing in this case.

15.5 Multiprocessor Communication Function

Use of the multiprocessor communication function enables data transfer between a number of processors sharing communication lines by asynchronous serial communication using the multiprocessor format, in which a multiprocessor bit is added to the transfer data. When multiprocessor communication is performed, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles; an ID transmission cycle that specifies the receiving station, and a data transmission cycle. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. If the multiprocessor bit is 1, the cycle is an ID transmission cycle; if the multiprocessor bit is 0, the cycle is a data transmission cycle. Figure 15.13 shows an example of inter-processor communication using the multiprocessor format. The transmitting station first sends the ID code of the receiving station with which it wants to perform serial communication as data with a 1 multiprocessor bit added. It then sends transmit data as data with a 0 multiprocessor bit added. When data with a 1 multiprocessor bit is received, the receiving station compares that data with its own ID. The station whose ID matches then receives the data sent next. Stations whose IDs do not match continue to skip data until data with a 1 multiprocessor bit is again received.

The SCI uses the MPIE bit in SCR to implement this function. When the MPIE bit is set to 1, transfer of receive data from RSR to RDR, error flag detection, and setting the SSR status flags, RDRF, FER, and ORER to 1, are inhibited until data with a 1 multiprocessor bit is received. On reception of a receive character with a 1 multiprocessor bit, the MPB bit in SSR is set to 1 and the MPIE bit is automatically cleared, thus normal reception is resumed. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt is generated.

When the multiprocessor format is selected, the parity bit setting is rendered invalid. All other bit settings are the same as those in normal asynchronous mode. The clock used for multiprocessor communication is the same as that in normal asynchronous mode.

15.10.7 Switching from SCK Pin Function to Port Pin Function

- Problem in Operation

  When switching the SCK pin function to the output port function (high-level output) by making the following settings while DDR = 1, DR = 1, C/$\overline{A}$ = 1, CKE1 = 0, CKE0 = 0, and TE = 1 (synchronous mode), low-level output occurs for one half-cycle.

  1. End of serial data transmission
  2. TE bit = 0
  3. C/$\overline{A}$ bit = 0… Switchover to port output
  4. Occurrence of low-level output

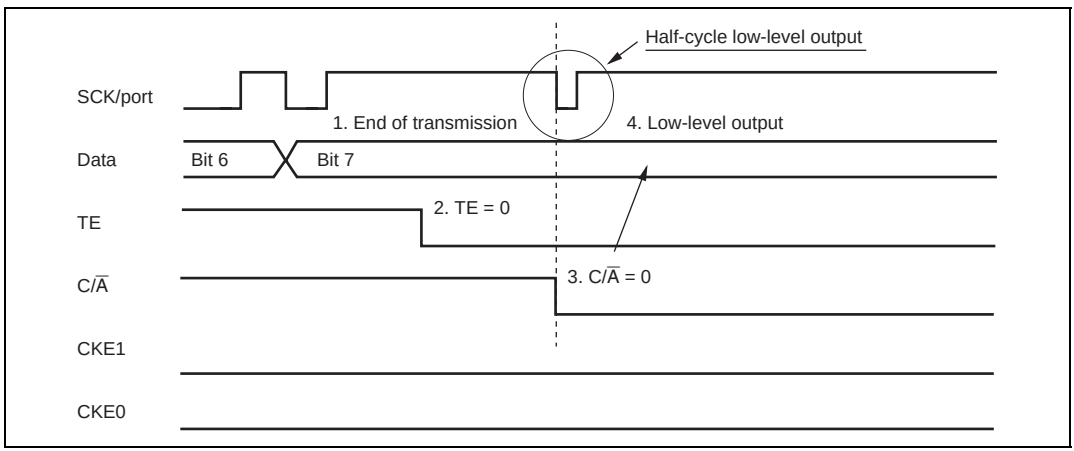


Figure 15.43 Operation when Switching from SCK Pin Function to Port Pin Function

- Sample Procedure for Avoiding Low-Level Output

  As this sample procedure temporarily places the SCK pin in the input state, the SCK/port pin should be pulled up beforehand with an external circuit.

  With DDR = 1, DR = 1, C/$\overline{A}$ = 1, CKE1 = 0, CKE0 = 0, and TE = 1, make the following settings in the order shown.

  1. End of serial data transmission
  2. TE bit = 0
  3. CKE1 bit = 1
  4. C/$\overline{A}$ bit = 0… Switchover to port output
  5. CKE1 bit = 0

Bit	Bit Name	Initial Value	R/W	Description
1	STC1	0	R/W	Multiplication factor setting
0	STC0	0	R/W	Specifies multiplication factor of the PLL circuit built in the evaluation chip. The specified multiplication factor becomes valid software standby mode, watch mode, or subactive mode is entered. These bits should be set to 11 in this LSI. Since the value becomes STC1 = STC0 = 0 after a reset, set STC1 = STC0 = 1. 00: × 1 01: × 2 (setting prohibited) 10: × 4 (setting prohibited) 11: PLL is bypass

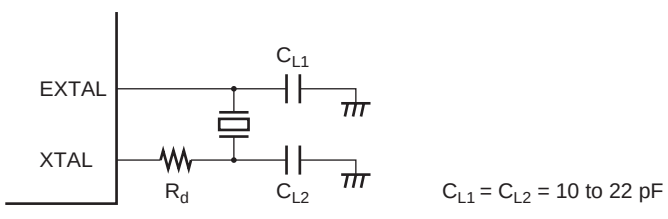
Note: * When watch mode or subactive mode is entered, set high-speed mode.

23.2 System Clock Oscillator

System clock pulses can be supplied by connecting a crystal resonator, or by input of an external clock.

23.2.1 Connecting a Crystal Resonator

A crystal resonator can be connected as shown in the example in figure 23.2. Select the damping resistance R_d according to table 23.1. An AT-cut parallel-resonance crystal should be used.



Note: C_{L1} and C_{L2} are reference values including the floating capacitance of the board.

Figure 23.2 Connection of Crystal Resonator (Example)

Table 23.1 Damping Resistance Value

Frequency (MHz)	2[*1]	4[*1]	6[*1]	8[*1]	10	12	16[*2]	20[*2]
R_d (Ω)	1 k	500	300	200	100	0	0	0

Notes: 1. The H8S/2258 Group is out of operation.
2. Supported only by the H8S/2239 Group.

Figure 23.3 shows the equivalent circuit of the crystal resonator. Use a crystal resonator that has the characteristics shown in table 23.2.

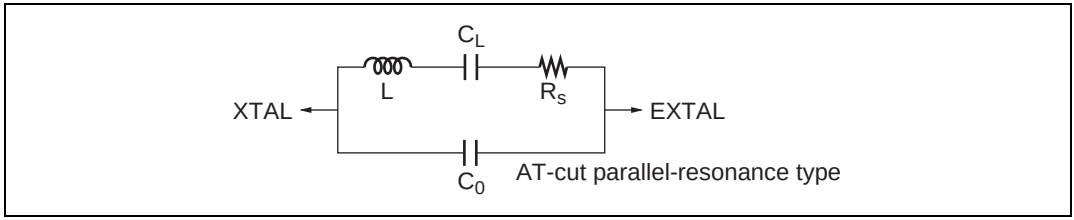


Figure 23.3 Crystal Resonator Equivalent Circuit

Table 23.2 Crystal Resonator Characteristics

Frequency (MHz)	2[*1]	4[*1]	6[*1]	8[*1]	10	12	16[*2]	20[*2]
R_S max (Ω)	500	120	100	80	60	60	50	40
C_0 max (pF)	7	7	7	7	7	7	7	7

Notes: 1. The H8S/2258 Group is out of operation.
2. Supported only by the H8S/2239 Group.

23.2.2 External Clock Input

An external clock signal can be input as shown in the examples in figure 23.4. If the XTAL pin is left open, ensure that stray capacitance does not exceed 10 pF. When complementary clock is input to the XTAL pin, the external clock input should be fixed high in standby mode, subactive mode, subsleep mode, or watch mode.

Table 23.4 External Clock Input Conditions (Duty Adjustment Circuit Unused) (3) (H8S/2238R, H8S/2236R)

		F-ZTAT		F-ZTAT and Masked ROM			
		V_{cc} = 2.7 V to 3.6 V		V_{cc} = 2.2 V to 3.6 V			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
External clock input low pulse width	t_{EXL}	37	—	80	—	ns	Figure 23.5
External clock input high pulse width	t_{EXH}	37	—	80	—	ns	
External clock rise time	t_{EXr}		7	—	15	ns	
External clock fall time	t_{EXf}	—	7	—	15	ns	

Note: If the duty adjustment circuit is not used, the maximum operating frequency will be lower to match the input waveform.

(Example: If $t_{EXL} = t_{EXH}$ = 37 ns and $t_{EXr} = t_{EXf}$ = 7 ns, the clock cycle = 88 ns and the maximum operating frequency = 11.3 MHz)

Table 23.4 External Clock Input Conditions (Duty Adjustment Circuit Unused) (4) (H8S/2237 Group, H8S/2227 Group)

		F-ZTAT and Masked ROM		Masked ROM		ZTAT			
		V_{cc} = 2.7 V to 3.6 V		V_{cc} = 2.2 V to 3.6 V		V_{cc} = 2.7 V to 3.6 V			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
External clock input low pulse width	t_{EXL}	37	—	80	—	50	—	ns	Figure 23.5
External clock input high pulse width	t_{EXH}	37	—	80	—	50	—	ns	
External clock rise time	t_{EXr}	—	7	—	15	—	10	ns	
External clock fall time	t_{EXf}	—	7	—	15	—	10	ns	

Note: If the duty adjustment circuit is not used, the maximum operating frequency will be lower to match the input waveform.

(Example: If $t_{EXL} = t_{EXH}$ = 37 ns and $t_{EXr} = t_{EXf}$ = 7 ns, the clock cycle = 88 ns and the maximum operating frequency = 11.3 MHz)

24.3.2 Exiting Sleep Mode

Sleep mode is exited by any interrupt, or signals at the $\overline{\text{RES}}$ pin, $\overline{\text{MRES}}$ pin, or $\overline{\text{STBY}}$ pin.

- Exiting Sleep Mode by Interrupts

  When an interrupt occurs, sleep mode is exited and interrupt exception processing starts. Sleep mode is not exited if the interrupt is disabled, or interrupts other than NMI are masked by the CPU.
- Exiting Sleep Mode by $\overline{\text{RES}}$ Pin or $\overline{\text{MRES}}$ Pin

  Setting the $\overline{\text{RES}}$ pin or $\overline{\text{MRES}}$ pin level low selects the reset state. After the stipulated reset input duration, driving the $\overline{\text{RES}}$ pin or $\overline{\text{MRES}}$ pin high starts the CPU performing reset exception processing.
- Exiting Sleep Mode by $\overline{\text{STBY}}$ Pin

  When the $\overline{\text{STBY}}$ pin level is driven low, a transition is made to hardware standby mode.

24.4 Software Standby Mode

24.4.1 Transition to Software Standby Mode

A transition is made to software standby mode when the SLEEP instruction is executed while the SSBY bit in SBYCR = 1 and the LSON bit in LPWRCR = 0, and the PSS bit in TCSR_1 (WDT_1) = 0. In this mode, the CPU, on-chip peripheral modules, and system clock oscillator all stop. However, the contents of the CPU's internal registers, RAM data, and the states of on-chip peripheral modules other than SCI and the A/D converter, and the states of I/O ports are retained. In this mode the oscillator stops, and therefore power dissipation is significantly reduced.

24.4.2 Clearing Software Standby Mode

Software standby mode is cleared by an external interrupt (NMI pin, or pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$), or by means of the $\overline{\text{MRES}}$ pin or $\overline{\text{STBY}}$ pin.

- Clearing with an Interrupt

  When an NMI, or IRQ7 to IRQ0 interrupt request signal is input, clock oscillation starts, and after the elapse of the time set in bits STS2 to STS0 in SYSCR, stable clocks are supplied to the entire this LSI chip, software standby mode is cleared, and interrupt exception handling is started.

  When clearing software standby mode with an IRQ7 to IRQ0 interrupt, set the corresponding enable bit/pin function switching bit to 1 and ensure that no interrupt with a higher priority