What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	4MHz
Connectivity	SIO, UART/USART
Peripherals	LCD, POR, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QIPE (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87f7932buef-2h

■Operating Temperature Range
- -40°C to +85°C

■Ports
- Normal withstand voltage I/O ports
  Ports whose input/output can be programmed in 1-bit units: 21 (P0n, P1n, P30, P70 to P73)
  Multiplexed functions
  Input ports (for debugger): 3 (DBGP0 (P05) to DBGP2 (P07))
  LCD ports (segment output): 8 (P1n)
- LCD ports/general purpose I/O ports
  Segment output: 32 (S00 to S31)
  Common output: 4 (COM0 to COM3)
  Bias power supply for LCD driving 5 (V1 to V3, CUP1, CUP2)
  Multiplexed functions
  Input/output ports: 36 (LPAn, LPBn, LPCn, LPL0 to LPL3, P1n)
- Oscillator pins: 4 (CF1, CF2, XT1, XT2)
- Reset pin: 1 ($\overline{\text{RES}}$)
- Power supply: 5 ($V_{SS}1$, $V_{SS}2$, $V_{DD}1$, $V_{DD}2$, V2)

■LCD Controller
(1) Seven display modes are available
(2) Duty: 1/3 duty, 1/4 duty
(3) Bias: 1/2 bias, 1/3 bias
(4) Segment/common output can be switched to general purpose I/O ports.
(5) LCD power range
    1) 1/3 bias   V1: 1.2V to 1.8V
                   V2: 2.4V to 3.6V
                   V3: 3.6V to 5.4V
                   An LCD panel that supports the V2 (=V_{DD}) × 1.5[V] must be used when 1/3 bias is selected.
                   If the supply voltage V_{DD} is 3.0V, for example, use an LCD panel that supports 4.5V.

    2) 1/2 bias   V1: 1.2V to 1.8V
                   V2: 2.4V to 3.6V
                   V3: 2.4V to 3.6V
                   (Connect V2 and V3 externally.)
                   An LCD panel that supports the V2 (=V_{DD})[V] must be used when 1/2 bias is selected.
                   If the supply voltage V_{DD} is 3.0V, for example, use an LCD panel that supports 3.0V.

■Timers
- Timer 0: 16 bit timer/counter with a capture register
        Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
        Mode 1: 8 bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter
               (with an 8-bit capture register)
        Mode 2: 16 bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
        Mode 3: 16 bit counter (with a 16 bit capture register)
- Timer 1: 16 bit timer/counter that supports PWM/toggle output
        Mode 0: 8-bit timer with an 8-bit prescaler (with toggle output) + 8-bit timer/counter (with toggle output)
        Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
        Mode 2: 16 bit timer/counter with an 8-bit prescaler (with toggle output)
               (Toggle outputs also from the low-order 8 bits)
        Mode 3: 16 bit timer with an 8-bit prescaler (with toggle output)
               (The low-order 8 bits can be used as a PWM.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Base Timer
  (1) The clock can be selected from any of the following:
      Subclock (32.768kHz crystal oscillator/low-speed RC oscillator), system clock, and timer 0 prescaler output.
  (2) Interrupts can be generated at five specified time intervals.

■High-speed Clock Counter
  (1) Capable of counting a clock with a maximum clock rate of 8MHz (at a main clock of 4MHz).
  (2) Real-time output

■Serial Interface
  • SIO0: 8-bit synchronous serial interface
    (1) Synchronous 8-bit serial I/O (2- or 3-wire configuration, 4/3 to 512/3 tCYC transfer clock rate)
    (2) Continuous data transfer (variable length data transfer in bit units from 1 to 256 bits, 4/3 to 512/3 tCYC transfer clock rate)
    (3) Bi-phase modulation
       Manchester/Bi-phase-Space data transfer
    (4) LSB first/MSB first selectable
    (5) SPI function: HOLD/X'tal HOLD mode release function upon receipt of a 1-byte (8-bit clock).

  • SIO1: 8-bit asynchronous/synchronous serial interface
       Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clock rate)
       Mode 1: Asynchronous serial I/O (half duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrate)
       Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clock rate)
       Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

■UART
  • Full duplex
  • Data length: 7/8/9 bits selectable
  • 1 stop bit (2 bits in continuous data transmission)
  • Built-in baudrate generator
  • Operating mode: Programmable transfer mode, fixed-rate transfer mode
  • Transfer data conversion: Normal (NRZ), Manchester encoding

■AD Converter: 12 bits/8 bits × 7 channels
  • 12-/8-bit AD converter resolution selectable

■Remote Control Receiver Circuit (multiplexed with the P73/INT3/T0IN pin)
  • Noise rejection function (Noise filter time constant selectable from 1/32/128 tCYC)

■Watchdog Timer
  • Generation of interrupt or system reset selectable
  • Two types of watchdog timer
    (1) Watchdog timer using an external RC circuit
    (2) Watchdog timer using the microcontroller's base timer
  • Detection intervals (1/2/4/8 seconds) can be selected for the watchdog timer that uses the base timer by configuring options.

■Buzzer Output
  • Generates buzzer output from P17 using the base timer.

■Real Time Clock (RTC)
  (1) Uses the base timer to count the calendar years, months, days, hours, minutes, and seconds.
  (2) Calendar counts up to December 31, 2799 and calculates leap years automatically
  (3) The RTC uses the Gregorian calendar, which maintains GMT (Greenwich Mean Time).

■Internal Reset Function
  • Power-on-reset (POR) function
    (1) The POR causes a system reset only when power is turned on.

∎Interrupts:
- 21 sources, 10 vectors

(1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.

(2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the lowest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L
4	0001BH	H or L	INT3/base timer/RTC
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1-receive
8	0003BH	H or L	SIO1/UART-send
9	00043H	H or L	ADC/T6/T7/SPI
10	0004BH	H or L	Port 0/T4/T5

- Priority level: $X > H > L$
- For equal priority levels, the interrupt with the lowest vector address is given priority.

∎Subroutine Stack Levels:
- Up to 1024 levels max. (Stack is allocated in RAM.)

∎High-speed Multiplication/Division Instructions
- 16 bits × 8 bits   (5 tCYC execution time)
- 24 bits × 16 bits   (12 tCYC execution time)
- 16 bits ÷ 8 bits   (8 tCYC execution time)
- 24 bits ÷ 16 bits   (12 tCYC execution time)

∎Oscillator Circuits
- On-chip high-speed RC oscillator: For system clock (500kHz typ)
- On-chip low-speed RC oscillator: For system clock (50kHz typ)
- CF oscillator: For system clock, Rf built in, Rd external
- Crystal oscillator: For low-speed system clock, Rf built in
- On-chip variable modulation frequency RC oscillator (VMRC): For system clock
  (1) Adjustable in ±4% (typ) step from a selected center frequency
  (2) Can measure the frequency of the source oscillator clock using an input signal from the XT1 pin as a reference.

∎System Clock Divider
- Low consumption current operation possible
- The minimum instruction cycle can be selected from among 750ns, 1.5μs, 3.0μs, 6.0μs, 12μs, 24μs, 48μs, 96μs, and 192μs (at a main clock rate of 4MHz).

∎System Clock Output
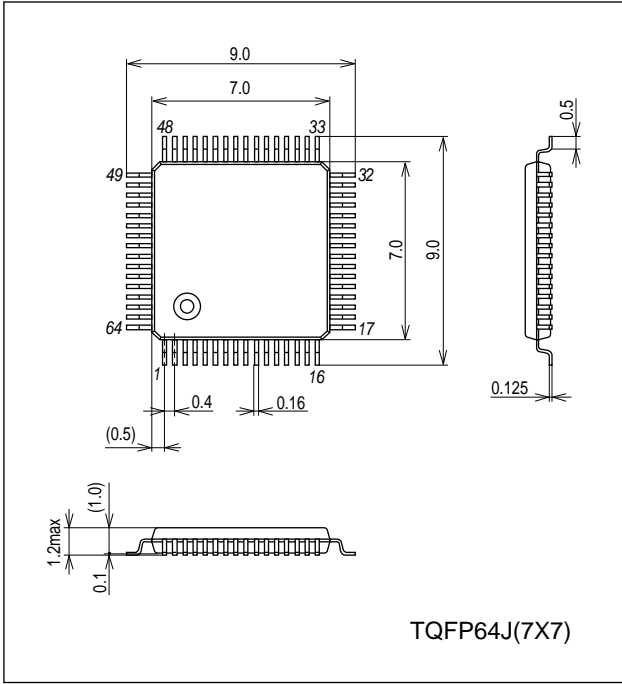- The system clock can be output from the P04 pin.
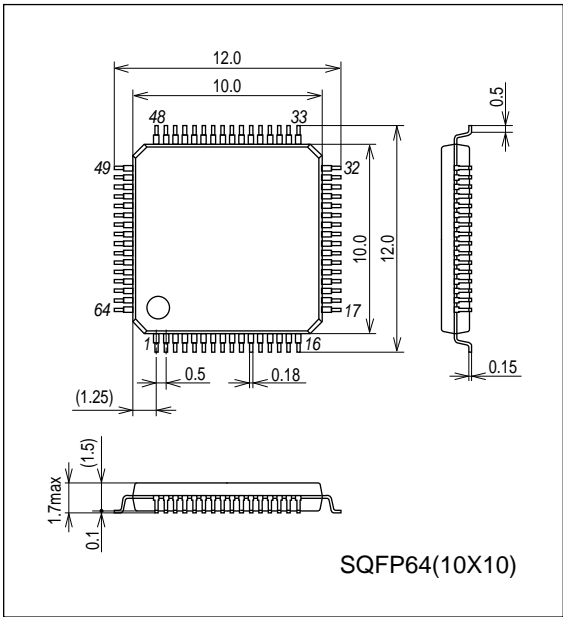
Package Dimensions

unit : mm (typ)
3159A
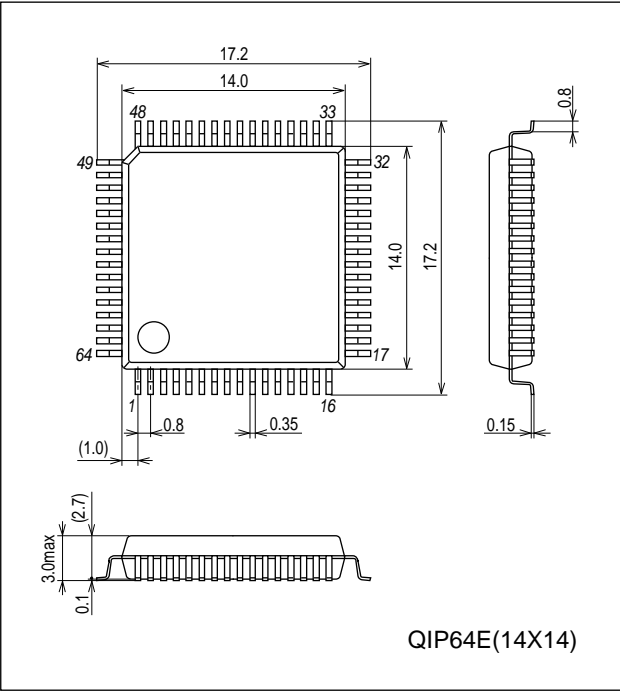
QIP64E(14X14)

Package Dimensions

unit : mm (typ)
3289

TQFP64J(7X7)

Package Dimensions

unit : mm (typ)
3190A

SQFP64(10X10)

Pin Assignment

Top labels (left to right, pins 48–33):
S23/LPC7, S22/LPC6, S21/LPC5, S20/LPC4, S19/LPC3, S18/LPC2, S17/LPC1, S16/LPC0, S15/LPB7, S14/LPB6, S13/LPB5, S12/LPB4, S11/LPB3, S10/LPB2, S09/LPB1, S08/LPB0

Left side (pins 49–64):

Pin	Signal
49	$\overline{\text{RES}}$
50	XT1
51	XT2
52	V$_{SS}$1
53	CF1
54	CF2
55	V$_{DD}$1
56	P00/UTX1/AN0
57	P01/RTX1/AN1
58	P02/AN2
59	P03/AN3
60	P04/CKO/AN4
61	P05/DBGP0
62	P06/T6O/DBGP1
63	P07/T7O/DBGP2
64	P30

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Right side (pins 32–17):

Pin	Signal
32	S07/LPA7
31	S06/LPA6
30	S05/LPA5
29	S04/LPA4
28	S03/LPA3
27	S02/LPA2
26	S01/LPA1
25	S00/LPA0
24	COM3/LPL3
23	COM2/LPL2
22	COM1/LPL1
21	COM0/LPL0
20	V3
19	V2
18	V1
17	VDC

Bottom labels (pins 1–16):
P70/INT0/T0LCP/AN5, P71/INT1/T0HCP/AN6, P72/INT2/T0IN/NKIN, P73/INT3/T0IN, VDD2, VSS2, P10/SO0/S24, P11/SI0/SB0/S25, P12/SCK0/S26, P13/SO1/S27, P14/SI1/SB1/S28, P15/SCK1/S29, P16/T1PWML/S30, P17/T1PWMH/BUZ/S31, CUP1, CUP2
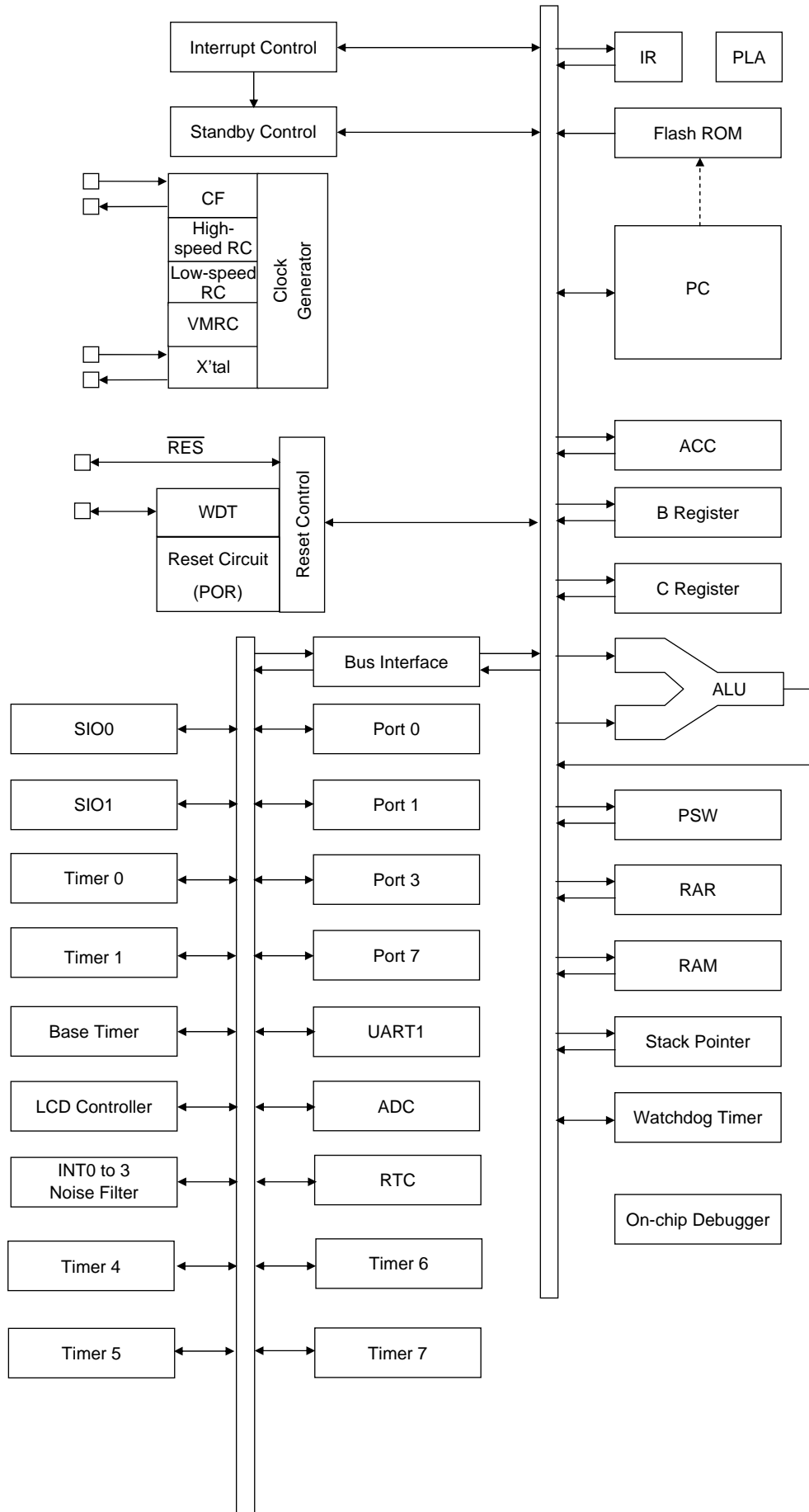
Top view

QIP64E (14×14) "Lead-and-halogen-free product"
TQFP64J (7×7) "Lead-and-halogen-free product"
SQFP64 (10×10) "Lead-and-halogen-free product"

System Block Diagram

```
                          ┌──────────────────┐                          ┌──────┐   ┌──────┐
                          │ Interrupt Control│◄────────────────────────►│  IR  │   │ PLA  │
                          └──────────────────┘                          └──────┘   └──────┘
                                   │
                                   ▼
                          ┌──────────────────┐                          ┌──────────────┐
                          │  Standby Control │◄────────────────────────►│  Flash ROM   │
                          └──────────────────┘                          └──────────────┘
                  ┌───┐   ┌──────┬───────────┐                                  ▲
                  └───┘──►│  CF  │           │                          ┌──────────────┐
                  ┌───┐   ├──────┤           │                          │              │
                  └───┘◄──│High- │           │                          │              │
                          │speed │  Clock    │                          │      PC      │
                          │ RC   │ Generator │◄────────────────────────►│              │
                          ├──────┤           │                          │              │
                          │Low-  │           │                          └──────────────┘
                          │speed │           │
                          │ RC   │           │
                          ├──────┤           │
                          │ VMRC │           │
                  ┌───┐   ├──────┤           │
                  └───┘──►│      │           │
                  ┌───┐   │X'tal │           │
                  └───┘◄──│      │           │
                          └──────┴───────────┘
                  ┌───┐   RES    ┌───────────┐                          ┌──────────────┐
                  └───┘◄────────►│           │◄────────────────────────►│     ACC      │
                          ┌──────┤  Reset    │                          └──────────────┘
                  ┌───┐   │ WDT  │  Control  │                          ┌──────────────┐
                  └───┘◄─►│      │           │◄────────────────────────►│  B Register  │
                          ├──────┤           │                          └──────────────┘
                          │Reset │           │                          ┌──────────────┐
                          │Circuit│          │                          │  C Register  │
                          │(POR) │           │                          └──────────────┘
                          └──────┴───────────┘
         ┌──────────┐           ┌──────────────┐                        ┌──────────────┐
         │  SIO0    │◄─►    ◄──►│ Bus Interface│◄──────────────────────►│     ALU      │
         └──────────┘           └──────────────┘                        └──────────────┘
         ┌──────────┐           ┌──────────────┐
         │  SIO1    │◄─►    ◄──►│    Port 0    │
         └──────────┘           └──────────────┘                        ┌──────────────┐
         ┌──────────┐           ┌──────────────┐                        │     PSW      │
         │ Timer 0  │◄─►    ◄──►│    Port 1    │                        └──────────────┘
         └──────────┘           └──────────────┘                        ┌──────────────┐
         ┌──────────┐           ┌──────────────┐                        │     RAR      │
         │ Timer 1  │◄─►    ◄──►│    Port 3    │                        └──────────────┘
         └──────────┘           └──────────────┘                        ┌──────────────┐
         ┌──────────┐           ┌──────────────┐                        │     RAM      │
         │Base Timer│◄─►    ◄──►│    Port 7    │                        └──────────────┘
         └──────────┘           └──────────────┘                        ┌──────────────┐
         ┌──────────┐           ┌──────────────┐                        │Stack Pointer │
         │LCD       │◄─►    ◄──►│    UART1     │                        └──────────────┘
         │Controller│           └──────────────┘                        ┌──────────────┐
         └──────────┘           ┌──────────────┐                        │Watchdog Timer│
         ┌──────────┐           │     ADC      │                        └──────────────┘
         │INT0 to 3 │◄─►    ◄──►└──────────────┘
         │Noise     │           ┌──────────────┐                        ┌──────────────┐
         │Filter    │           │     RTC      │                        │On-chip       │
         └──────────┘           └──────────────┘                        │Debugger      │
         ┌──────────┐           ┌──────────────┐                        └──────────────┘
         │ Timer 4  │◄─►    ◄──►│   Timer 6    │
         └──────────┘           └──────────────┘
         ┌──────────┐           ┌──────────────┐
         │ Timer 5  │◄─►    ◄──►│   Timer 7    │
         └──────────┘           └──────────────┘
```

User Option Table

Option Name	Option to be Applied on	Mask Version *1	Flash-ROM Version	Option Selected in Units of	Option Selection
Port output type	P00 to P07		○	1 bit	CMOS
					N-channel open drain
	P10 to P17		○	1 bit	CMOS
					N-channel open drain
	P30		○	1 bit	CMOS
					N-channel open drain
Base timer watchdog timer	Watchdog timer detection period		○	-	1 second
					2 seconds
					4 seconds
					8 seconds
Program start address	-	*2	○	-	00000h
					07E00h

*1: Mask option selection. No change possible after mask is completed.

*2: Program start address of the mask version is 00000h.

*Note 1: Connect the IC as shown below to minimize noise on the $V_{DD}1$.

Be sure to electrically short the $V_{SS}1$ and $V_{SS}2$.

*Note 2: The power to retain the internal memory is supplied via the V2 pin. $V_{DD}1$, $V_{DD}2$ and V2 are used as power supply for ports. If $V_{DD}1$ and $V_{DD}2$ are not backed up, the output does not go high even if a high level is applied to the port latch. Therefore, if $V_{DD}1$ and $V_{DD}2$ are not backed up, the high level output becomes unstable in HOLD mode, and the backup time becomes shorter because a through-current flows from V_{DD} to GND in the input buffer.

If $V_{DD}1$ and $V_{DD}2$ are not backed up, configure the program or set up the external circuit so that the output is held at a low level in HOLD mode to prevent an unnecessary through-current from flowing.
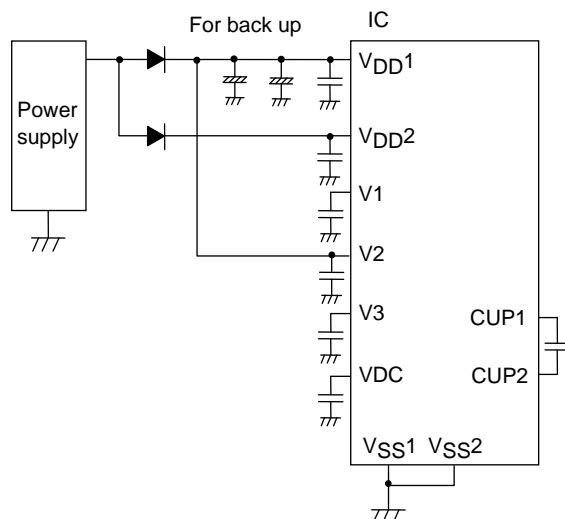
Circuit Example

(1)1/3 bias, 1/4 duty

LCD panel 24SEG×4COM

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I/O — P00, P01, P02, P03, P04, P05, P06, P07

I/O — P10, P11, P12, P13, P14, P15, P16, P17

I/O — P70, P71, P72, P73

I/O — P30

COM0 ---- COM3   S00 ----- S23

CUP1, CUP2 — C1

VDC — C2
V1 — C3
V2 — C4
V3 — C5

2.4V to 3.6V

VDD1, VDD2

R_{RES} C_{DEN}

$\overline{RES}$

C_{RES}

VSS1, VSS2

CF2 CF1   XT2 XT1

CF / C_{DC} / C_{GC} *2   X'tal / C_{DX} / C_{GX} *1

*1: Crystal oscillator
*2: Ceramic oscillator

X'tal	Crystal resonator	Refer to Page 26 (Characteristics of a sample clock oscillator circuit)
C_{GX}	Trimmer capacitor	
C_{DX}	Capacitor for crystal oscillator	
CF	Ceramic resonator	Refer to Page 26 (Characteristics of a sample clock oscillator circuit)
C_{GC}	Capacitor for ceramic oscillator	
C_{DC}	Capacitor for ceramic oscillator	
C1 to C5	Capacitors	0.1μF (recommended)
C_{DEN}	Electrolytic capacitor	For back up
C_{RES}	Capacitor for $\overline{RES}$	Refer to User's manual "Reset Function"
R_{RES}	Resistor for $\overline{RES}$	

(2)1/2 bias, 1/3 duty

X'tal	Crystal resonator	Refer to Page 26 (Characteristics of a sample clock oscillator circuit)
C_{GX}	Trimmer capacitor	
C_{DX}	Capacitor for crystal oscillator	
CF	Ceramic resonator	Refer to Page 26 (Characteristics of a sample clock oscillator circuit)
C_{GC}	Capacitor for ceramic oscillator	
C_{DC}	Capacitor for ceramic oscillator	
C1 to C4	Capacitors	0.1μF (recommended)
C_{DEN}	Electrolytic capacitor	For back up
C_{RES}	Capacitor for $\overline{RES}$	Refer to User's manual "Reset Function"
R_{RES}	Resistor for $\overline{RES}$	

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Allowable Operating Conditions at Ta=-40°C to +85°C, $V_{SS}1=V_{SS}2=0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V2$	$0.75\mu s{\leq}tCYC{\leq}200\mu s$ Normal mode		2.4		3.6	
Memory sustaining supply voltage	VHD	$V_{DD}1=V_{DD}2=V2$	RAM and register contents sustained in HOLD mode.		2.2		3.6	
High level input voltage	$V_{IH}(1)$	Ports 0, 3 LPA, LPB, LPC, LPL	Output disabled	2.4 to 3.6	$0.3V_{DD}$ +0.7		V_{DD}	V
	$V_{IH}(2)$	Port 1 P71 to 73 P70 port input / interrupt side	• Output disabled • When INT1VTSL=0 (P71 only)	2.4 to 3.6	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	P71 interrupt side	• Output disabled • When INT1VTSL=1	2.4 to 3.6	$0.85V_{DD}$		V_{DD}	
	$V_{IH}(4)$	P70 watchdog timer side	Output disabled	2.4 to 3.6	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(5)$	XT1, XT2, CF1, $\overline{RES}$		2.4 to 3.6	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 0, 3 LPA, LPB, LPC, LPL	Output disabled	2.4 to 3.6	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Port 1 P71 to 73 P70 port input / interrupt side	• Output disabled • When INT1VTSL=0 (P71 only)	2.4 to 3.6	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	P71 interrupt side	• Output disabled • When INT1VTSL=1	2.4 to 3.6	V_{SS}		$0.45V_{DD}$	
	$V_{IL}(4)$	P70 watchdog timer side	Output disabled	2.4 to 3.6	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(5)$	XT1, XT2, CF1, $\overline{RES}$		2.4 to 3.6	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC			2.4 to 3.6			200	μs
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ratio = 1/1 • External system clock duty = 50±5%	2.4 to 3.6	0.1		4	MHz
			• CF2 pin open • System clock frequency division ratio = 1/2	2.4 to 3.6	0.2		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	• 4MHz ceramic oscillation • See Fig. 1.	2.4 to 3.6		4		MHz
	FmRC(1)		Internal high-speed RC oscillation	2.4 to 3.6	250	500	750	
	FsRC(1)		Internal low-speed RC oscillation	2.4 to 3.6	25	50	75	kHz
	FsX'tal	XT1, XT2	• 32.768kHz crystal oscillation • See Fig. 2.	2.4 to 3.6		32.768		
VMRC oscillation usable range	OpVMRC(1)		When VMSL4M=0	3.0 to 3.6	8	10	12	MHz
	OpVMRC(2)		When VMSL4M=1	2.4 to 3.6	3.5	4	4.5	
VMRC oscillation adjustment range	VmADJ(1)		Each step of VMRAJn (Wide range)	2.4 to 3.6	8	24	64	%
	VmADJ(2)		Each step of VMFAJn (Small range)	2.4 to 3.6	1	4	8	

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

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Electrical Characteristics at Ta=-40°C to +85°C, $V_{SS}1=V_{SS}2=0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 3, 7 LPA, LPB, LPC LPL	• Output disabled • Pull-up resistor off • $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	2.4 to 3.6			1	μA
	$I_{IH}(2)$	$\overline{RES}$	$V_{IN}=V_{DD}$	2.4 to 3.6			1	
	$I_{IH}(3)$	XT1, XT2	• Input port specification • $V_{IN}=V_{DD}$	2.4 to 3.6			1	
	$I_{IH}(4)$	CF1	$V_{IN}=V_{DD}$	2.4 to 3.6			15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 3, 7 LPA, LPB, LPC LPL	• Output disabled • Pull-up resistor off • $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	2.4 to 3.6	-1			
	$I_{IL}(2)$	$\overline{RES}$	$V_{IN}=V_{SS}$	2.4 to 3.6	-1			
	$I_{IL}(3)$	XT1, XT2	• Input port specification • $V_{IN}=V_{SS}$	2.4 to 3.6	-1			
	$I_{IL}(4)$	CF1	$V_{IN}=V_{SS}$	2.4 to 3.6	-15			
High level output voltage	$V_{OH}(1)$	CMOS output ports 0, 1	$I_{OH}=-0.4mA$	3.0 to 3.6	V_{DD}-0.4			
	$V_{OH}(2)$		$I_{OH}=-0.2mA$	2.4 to 3.6	V_{DD}-0.4			
	$V_{OH}(3)$	CMOS output port 3	$I_{OH}=-1.6mA$	3.0 to 3.6	V_{DD}-0.4			
	$V_{OH}(4)$		$I_{OH}=-1mA$	2.4 to 3.6	V_{DD}-0.4			
	$V_{OH}(5)$	P71 to 73	$I_{OH}=-0.4mA$	3.0 to 3.6	V_{DD}-0.4			
	$V_{OH}(6)$		$I_{OH}=-0.2mA$	2.4 to 3.6	V_{DD}-0.4			
	$V_{OH}(7)$	LPA, LPB, LPC LPL	$I_{OH}=-0.1mA$	2.4 to 3.6	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1	$I_{OL}=1.6mA$	3.0 to 3.6			0.4	
	$V_{OL}(2)$		$I_{OL}=1mA$	2.4 to 3.6			0.4	
	$V_{OL}(3)$	Port 3	$I_{OL}=5mA$	3.0 to 3.6			0.4	V
	$V_{OL}(4)$		$I_{OL}=2.5mA$	2.4 to 3.6			0.4	
	$V_{OL}(5)$	Port 7	$I_{OL}=1.6mA$	3.0 to 3.6			0.4	
	$V_{OL}(6)$	XT2	$I_{OL}=1mA$	2.4 to 3.6			0.4	
	$V_{OL}(7)$	LPA, LPB, LPC LPL	$I_{OL}=0.1mA$	2.4 to 3.6			0.4	
LCD output voltage deviation	VODLS	S00 to S31	• $I_O=0mA$ • V1, V2, V3 LCD level output • See Fig. 8.	2.4 to 3.6	0		±0.2	
	VODLC	COM0 to COM3	• $I_O=0mA$ • V1, V2, V3 LCD level output • See Fig. 8.	2.4 to 3.6	0		±0.2	
Pull-up resistance	Rpu(1)	Ports 0, 1, 3, 7	$V_{OH}=0.9V_{DD}$	2.4 to 3.6	18	50	150	kΩ
Hysterisis voltage	VHYS(1)	Ports 1, 7 $\overline{RES}$		2.4 to 3.6		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	• For pins other than that under test: $V_{IN}=V_{SS}$ • f=1MHz • Ta=25°C	2.4 to 3.6		10		pF

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.4 to 3.6	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.4 to 3.6	2			tSCK
		Low level pulse width	tSCKL(4)					1/2		
		High level pulse width	tSCKH(4)					1/2		
Serial input		Data setup time	tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to the rising edge of SIOCLK. • See Fig. 6.	2.4 to 3.6	0.03			µs
		Data hold time	thDI(2)				0.03			
Serial output		Output delay time	tdDO(4)	SO1(P13), SB1(P14)	• Must be specified with respect to the falling edge of SIOCLK. • Must be specified as the time up to the beginning of output state change in open drain output mode. • See Fig. 6.	2.4 to 3.6			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Be sure to add margin depending on its use.

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72)	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.4 to 3.6	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.4 to 3.6	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.4 to 3.6	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.4 to 3.6	256			
	tPIL(5)	$\overline{RES}$	Resetting is enabled.	2.4 to 3.6	200			µs

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Current consumption in normal operating mode (Note 7-1)	IDDOP(1)	$V_{DD}1=V_{DD}2$ =V2	• FmCF=4MHz ceramic oscillation • FsX'tal=32.768kHz crystal oscillation • System clock set to 4MHz side • Internal RC oscillation stopped • VMRC oscillation stopped • 1/1 frequency division ratio	2.4 to 3.6		2.0	4.2	mA
	IDDOP(2)		• FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • System clock set to high-speed internal RC oscillation • VMRC oscillation stopped • 1/1 frequency division ratio	2.4 to 3.6		250	900	μA
	IDDOP(3)		• FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • System clock set to low-speed internal RC oscillation • VMRC oscillation stopped • 1/1 frequency division ratio	2.4 to 3.6		30	120	
	IDDOP(4)		• FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • Internal RC oscillation stopped • System clock set to 4MHz VMRC oscillation • 1/1 frequency division ratio	2.4 to 3.6		2.0	5.4	mA
	IDDOP(5)		• FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • Internal RC oscillation stopped • System clock set to 500kHz VMRC oscillation •1/1 frequency division ratio	2.4 to 3.6		250	900	μA
	IDDOP(6)		• FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • System clock set to 32.768kHz side • Internal RC oscillation stopped • VMRC oscillation stopped • 1/1 frequency division ratio • Normal XT amp mode	2.4 to 3.6		20	86	
	IDDOP(7)		• FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • System clock set to 32.768kHz side • Internal RC oscillation stopped • VMRC oscillation stopped •1/1 frequency division ratio • Low consumption XT amp mode	2.4 to 3.6		15	72	

Note 7-1: The consumption current value does not include current that flows into the output transistors and internal pull-up resistors.

Continued from preceding page.

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Current consumption in HALT mode (Note 7-1)	IDDHALT(1)	$V_{DD}1=V_{DD}2$ =V2	HALT mode • FmCF=4MHz ceramic oscillation • FsX'tal=32.768kHz crystal oscillation • System clock set to 4MHz side • Internal RC oscillation stopped • VMRC oscillation stopped • 1/1 frequency division ratio	2.4 to 3.6		0.55	1.55	mA
	IDDHALT(2)		HALT mode • FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • System clock set to high-speed internal RC oscillation • VMRC oscillation stopped • 1/1 frequency division ratio	2.4 to 3.6		68	280	
	IDDHALT(3)		HALT mode • FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • System clock set to low-speed internal RC oscillation • VMRC oscillation stopped • 1/1 frequency division ratio	2.4 to 3.6		7	85	
	IDDHALT(4)		HALT mode • FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • Internal RC oscillation stopped • System clock set to 4MHz VMRC oscillation • 1/1 frequency division ratio	2.4 to 3.6		650	1460	
	IDDHALT(5)		HALT mode • FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • Internal RC oscillation stopped • System clock set to VMRC oscillation (500kHz) • 1/1 frequency division ratio	2.4 to 3.6		68	280	μA
	IDDHALT(6)		HALT mode • FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • System clock set to 32.768kHz side • Internal RC oscillation stopped. • VMRC oscillation stopped •1/1 frequency division ratio • Normal XT amp mode	2.4 to 3.6		8	70	
	IDDHALT(7)		HALT mode • FmCF=0Hz (Oscillation stopped) • FsX'tal=32.768kHz crystal oscillation • System clock set to 32.768kHz side • Internal RC oscillation stopped. • VMRC oscillation stopped • 1/1 frequency division ratio • Low consumption XT amp mode	2.4 to 3.6		4	50	

Note 7-1: The consumption current value does not include current that flows into the output transistors and internal pull-up resistors.

Continued from preceding page.

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Current consumption in HOLD mode	IDDHOLD(1)	$V_{DD}1=V_{DD}2$ $=V2$	HOLD mode • CF1=V_{DD} or open (When using external clock)	2.4 to 3.6		0.05	30	μA
Current consumption in time-of-day clock HOLD mode	IDDHOLD(2)	$V_{DD}1=V_{DD}2$ $=V2$	Time-of-day clock HOLD mode • CF1=V_{DD} or open (When using external clock) • FsX'tal=32.768kHz crystal oscillation • 1/1 frequency division ratio • LCD display off • Normal XT amp mode	2.4 to 3.6		6.5	67	
	IDDHOLD(3)		Time-of-day clock HOLD mode • CF1=V_{DD} or open (When using external clock) • FsX'tal=32.768kHz crystal oscillation • 1/1 frequency division ratio • LCD display off • Low consumption XT amp mode	2.4 to 3.6		0.45	46	
	IDDHOLD(4)		Time-of-day clock HOLD mode • CF1=V_{DD} or open (When using external clock) • FsX'tal=low-speed RC oscillation • 1/1 frequency division ratio • LCD display off	2.4 to 3.6		1.5	70	

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Excluding power dissipation in the microcontroller block	3.0 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing operation	3.0 to 5.5		20	30	ms
	tFW(2)		• Programming operation			45	60	µs

UART (Full Duplex) Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR	UTX (P00), URX (P01)		2.4 to 3.6	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)
Stop bits: 1 bit (2 bits in continuous data transmission)
Parity bits: None

Example of 8-bit Data Transmission Mode Processing (Transmit Data=55H)
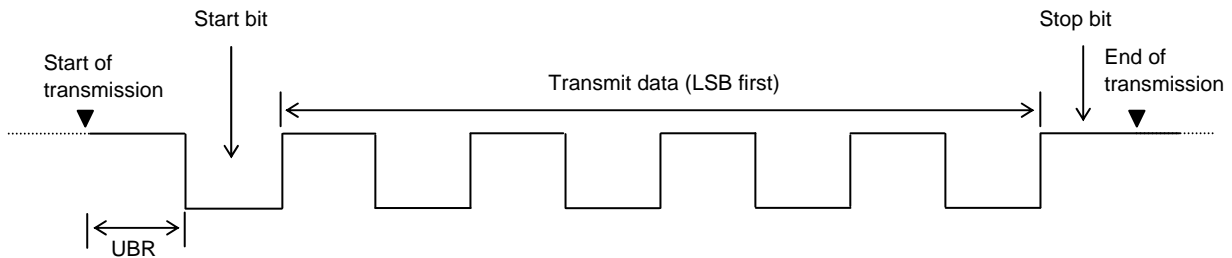
Example of 8-bit Data Reception Mode Processing (Receive Data=55H)
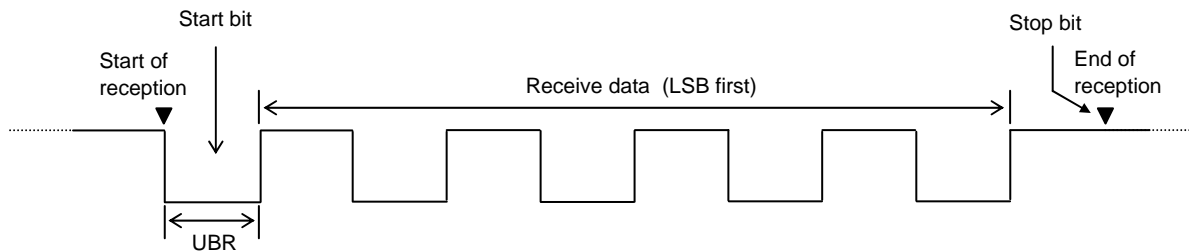
Characteristics of a Sample Main System Clock Oscillator Circuit

Given below are the characteristics of a sample main system clock oscillator circuit, which are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with normal and stable oscillation confirmed by the resonator vendor.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal Frequency	Vendor Name	Resonator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
4.00MHz	Murata	CSTCR4M00G53-R0	(15)	(15)	Open	1k	2.4 to 3.6	0.03	0.15	Internal C1, C2
		CSTLS4M00G53-B0	(15)	(15)	Open	1k	2.4 to 3.6	0.02	0.15	

The oscillation stabilization time is the period required for the resonator to stabilize in the following situations. (See Figure 4)

- After V_{DD} goes above the operating voltage lower limit until the oscillation is stabilized.
- After the instruction for starting the main clock oscillation circuit is executed until the oscillation is stabilized.
- After HOLD mode is released until the oscillation is stabilized.
- After HOLD mode is released and oscillation is started with CFSTOP (OCR register, bit0) set to 0 until the oscillation is stabilized.

Characteristics of a Sample Sub-system Clock Oscillator Circuit

Given below are the characteristics of a sample sub-system clock oscillator circuit, which are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with normal and stable oscillation confirmed by the resonator vendor. (Different evaluation boards are used for Tables 2 and 3.)

Table 2 Characteristics of a Sample Sub-system Clock Oscillator Circuit with a Crystal Resonator 1

Nominal Frequency	Vendor Name	Resonator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768KHz	Epson Toyocom	MC-306	9	9	Open	330k	2.4 to 3.6	1	3	CL=7.0pF Normal amp
			3	3	Open	0	2.4 to 3.6	2	6	CL=7.0pF Low consumption amp

Table 3 Characteristics of a Sample Sub-system Clock Oscillator Circuit with a Crystal Resonator 2 (*5)

Nominal Frequency	Vendor Name	Resonator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz (*1)	Seiko Instruments (*2)	SSP-T7-F	22	22	Open	820k	2.4 to 3.6	1.8	3	CL=12.5pF (*3) Normal amp
		VT-200-F								
		SSP-T7-FL	7	6	Open	0	2.4 to 3.6	0.9	3	CL=6.0pF (*4) Low consumption amp
		VT-200-FL								

(*1) Normal XT amplifier mode (*3) or low consumption amplifier mode (*4) should be selected for the sub-system clock oscillator circuit.

(*2) Contact Seiko Instruments, Inc., (http://www.sii-crystal.com) for further information about the use of the resonator.

(*3) When considering the use of normal XT amplifier mode, use an resonator that has a large load capacitance.

(*4) When considering the use of low consumption XT amplifier mode, use a resonator that has a small load capacitance. The applicable CL value of 6.0pF makes it possible to achieve a high time accuracy for the subclock oscillator as well as high-speed oscillation startup and low power dissipation. In addition to this value, 7.0pF and 9.0pF also fall within the applicable CL value range.
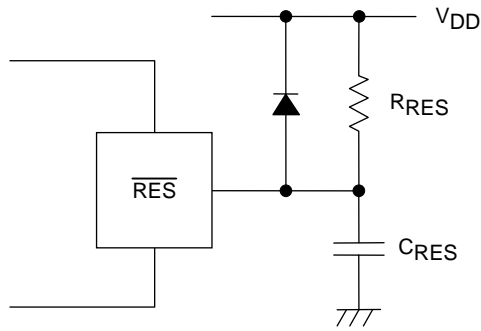
LC87F7932B
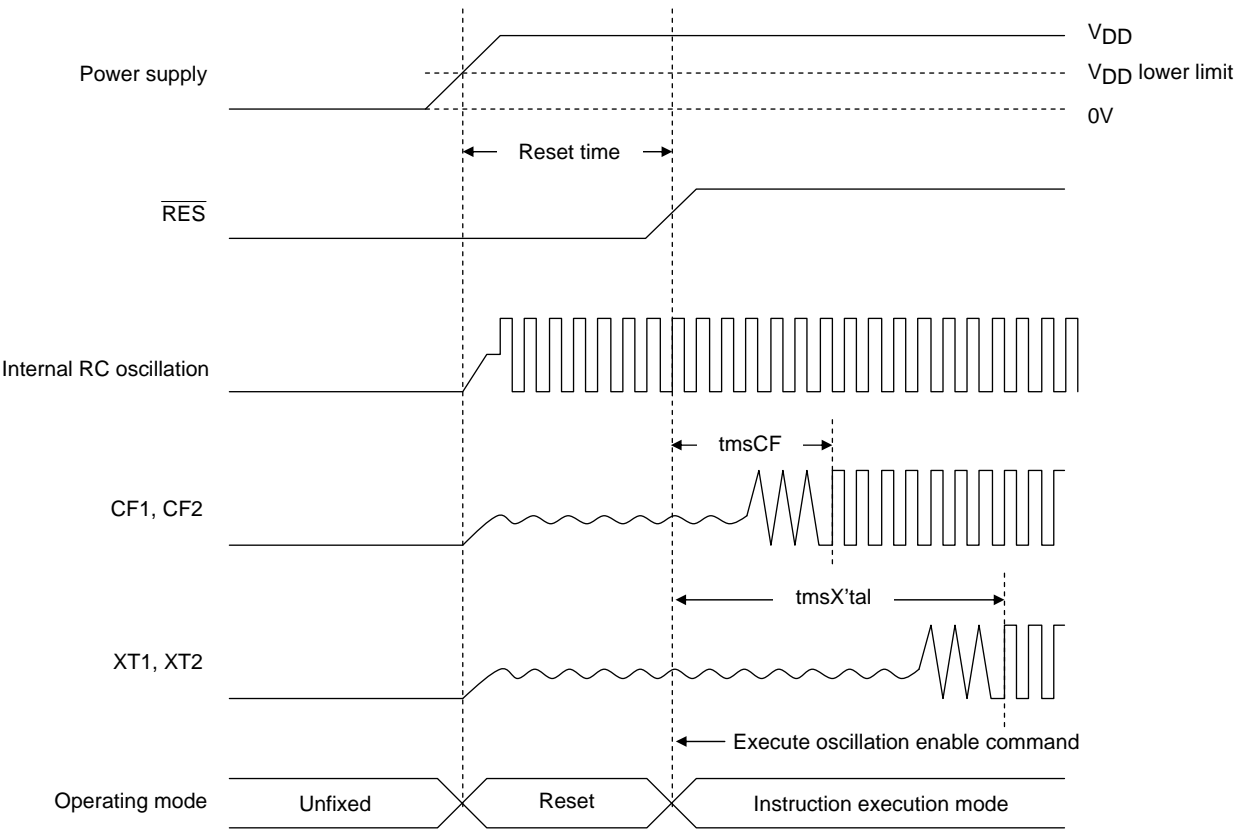
Reset Time and Oscillation Stabilization Time
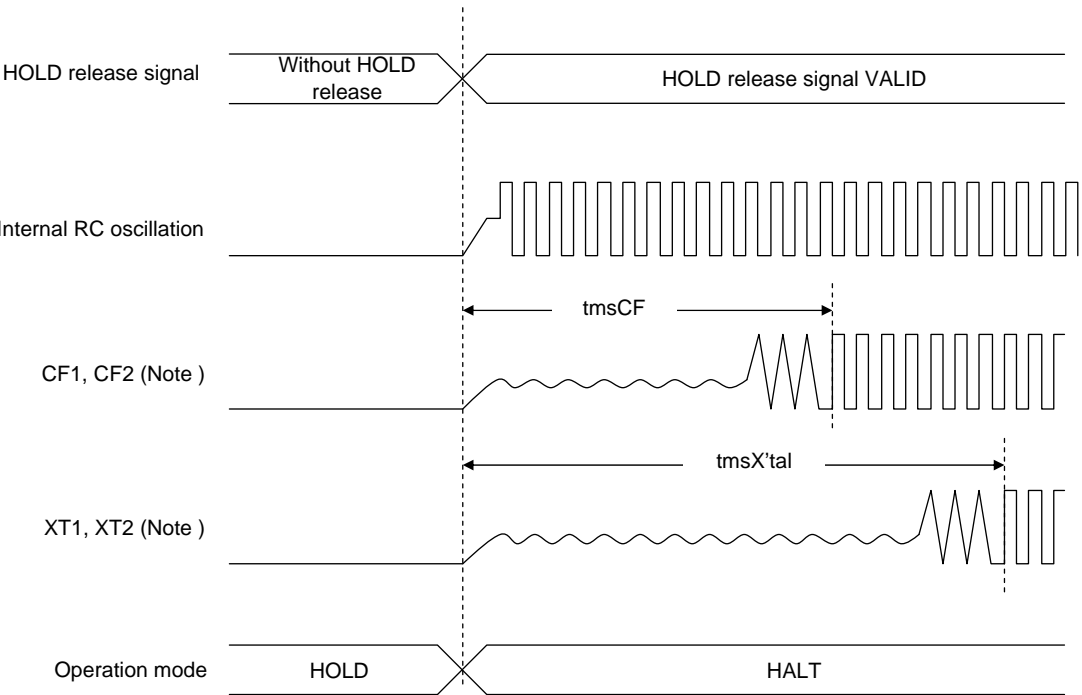
HOLD Release Signal and Oscillation Stabilization Time

Note: Oscillation is enabled before HOLD mode is entered.

Figure 4   Oscillation Stabilization Time

LC87F7932B

Note:
External circuits for reset may vary depending on the usage of POR. Please refer to the user's manual on reset function.
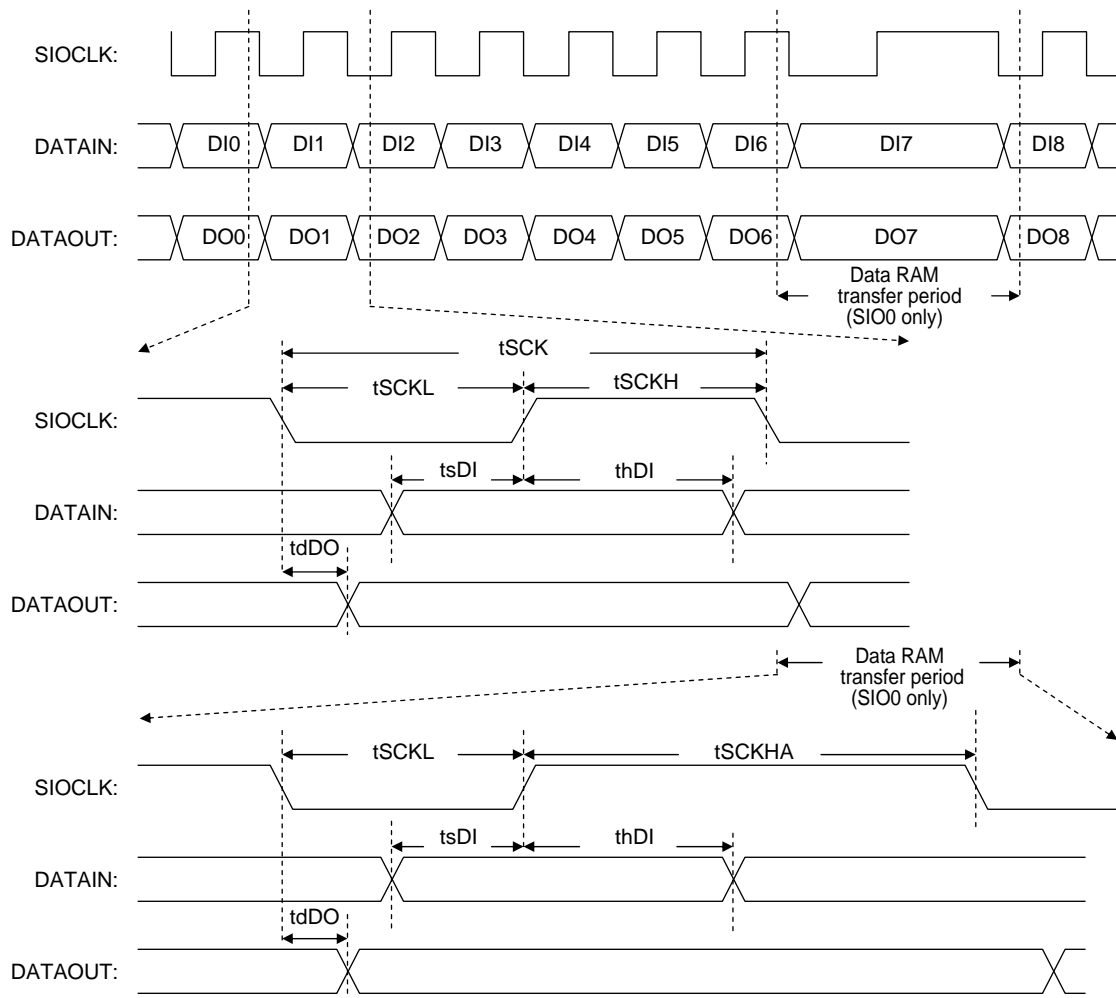
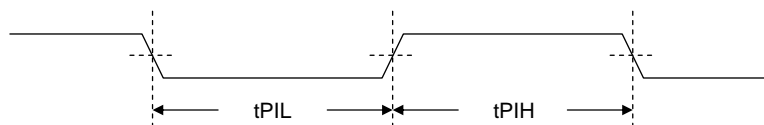Figure 5 Reset Circuit

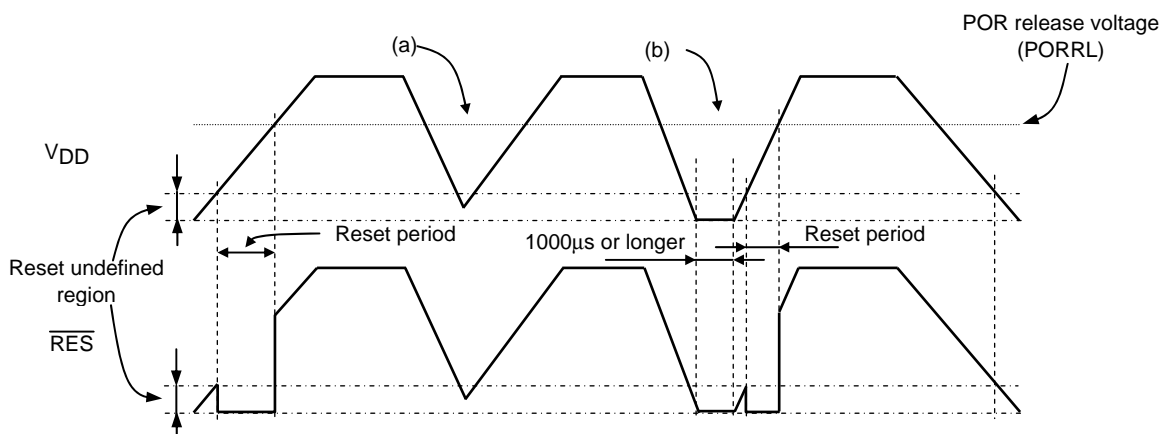Figure 6 Serial Input/Output Waveform

Figure 7 Pulse Input Timing Waveform

Figure 8   Sample Operating Waveforms when POR is Used
(Reset pin: Pull-up resistor R$_{RES}$ only)

- The POR function generates a reset only when power is turned on starting at the V$_{SS}$ level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V$_{SS}$ level as shown in (a).
- A reset is generated only when the power level goes down to the V$_{SS}$ level as shown in (b) and power is turned on again after this condition continues for 1000μs or longer.