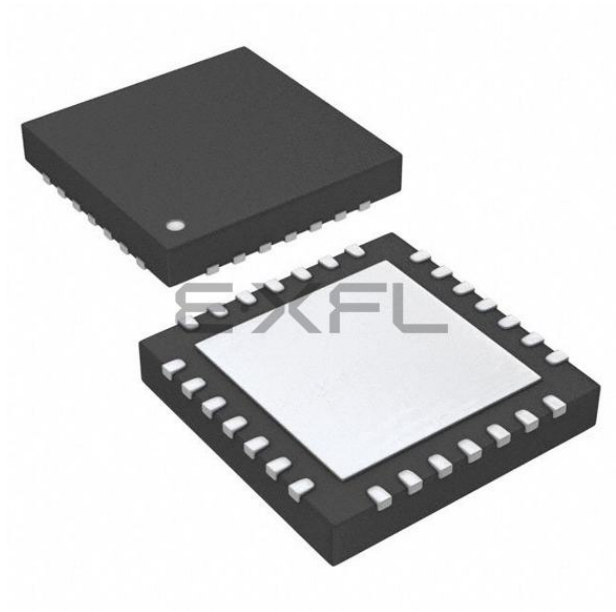

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1782-e-mv

1.0 DEVICE OVERVIEW

The PIC16(L)F1782/3 are described within this data sheet. The block diagram of these devices are shown in Figure 1-1. The available peripherals are shown in Table 1-1, and the pin out descriptions are shown in Table 1-2.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1782	PIC16(L)F1783	PIC16(L)F1784	PIC16(L)F1786	PIC16(L)F1787	PIC16(L)F1788	PIC16(L)F1789
Analog-to-Digital Converter (ADC)		•	•	•	•	•	•	•
Fixed Voltage Reference (FVR)		•	•	•	•	•	•	•
Reference Clock Module		•	•	•	•	•	•	•
Temperature Indicator		•	•	•	•	•	•	•
Capture/Compare/PWM (CCP/ECCP) Modules								
	CCP1	•	•	•	•	•	•	•
	CCP2	•	•	•	•	•	•	•
	CCP3			•	•	•	•	•
Comparators								
	C1	•	•	•	•	•	•	•
	C2	•	•	•	•	•	•	•
	C3	•	•	•	•	•	•	•
	C4			•	•	•	•	•
Digital-to-Analog Converter (DAC)								
	(8-bit DAC) D1	•	•	•	•	•	•	•
	(5-bit DAC) D2							•
	(5-bit DAC) D3							•
	(5-bit DAC) D4							•
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)								
	EUSART	•	•	•	•	•	•	•
Master Synchronous Serial Ports								
	MSSP	•	•	•	•	•	•	•
Op Amp								
	Op Amp 1	•	•	•	•	•	•	•
	Op Amp 2	•	•	•	•	•	•	•
	Op Amp 3			•		•		•
Programmable Switch Mode Controller (PSMC)								
	PSMC1	•	•	•	•	•	•	•
	PSMC2	•	•	•	•	•	•	•
	PSMC3			•	•	•	•	•
	PSMC4						•	•
Timers								
	Timer0	•	•	•	•	•	•	•
	Timer1	•	•	•	•	•	•	•
	Timer2	•	•	•	•	•	•	•

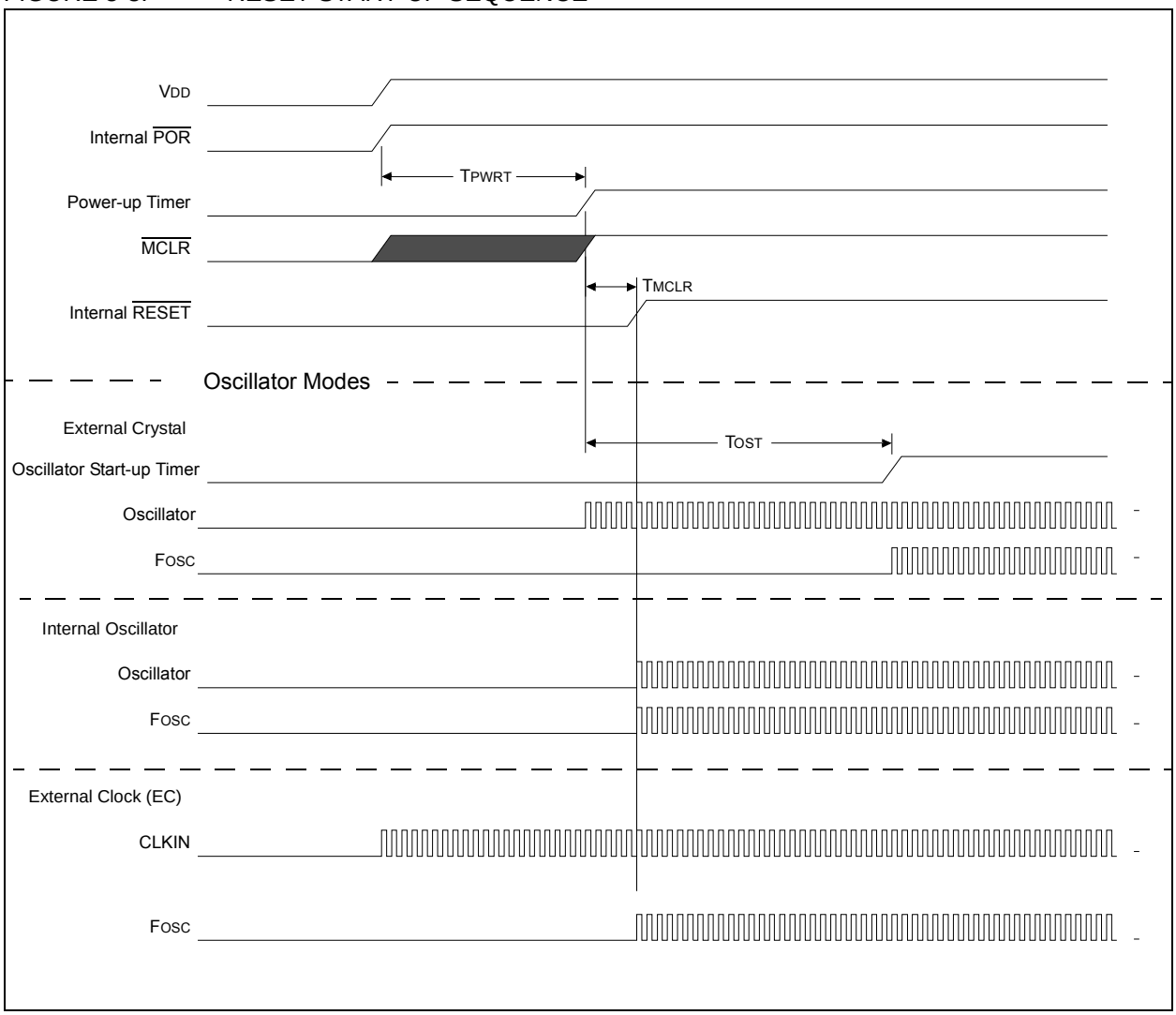
TABLE 1-2: PIC16(L)F1782/3 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB0/AN12/C2IN1+/PSMC1IN/ PSMC2IN/CCP1(1)/INT	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	A/D Channel 12 input.
	C2IN1+	AN	—	Comparator C2 positive input.
	PSMC1IN	ST	—	PSMC1 Event Trigger input.
	PSMC2IN	ST	—	PSMC2 Event Trigger input.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
	INT	ST	—	External interrupt.
RB1/AN10/C1IN3-/C2IN3-/ C3IN3-/OPA2OUT	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	A/D Channel 10 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	C3IN3-	AN	—	Comparator C3 negative input.
	OPA2OUT	—	AN	Operational Amplifier 2 output.
RB2/AN8/OPA2IN-/CLKR	RB2	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	A/D Channel 8 input.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
	CLKR	—	CMOS	Clock output.
RB3/AN9/C1IN2-/C2IN2-/ C3IN2-/OPA2IN+/CCP2(1)	RB3	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	A/D Channel 9 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	C3IN2-	AN	—	Comparator C3 negative input.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RB4/AN11/C3IN1+	RB4	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	A/D Channel 11 input.
	C3IN1+	AN	—	Comparator C3 positive input.
RB5/AN13/C3OUT/T1G/SDO(1)	RB5	TTL/ST	CMOS	General purpose I/O.
	AN13	AN	—	A/D Channel 13 input.
	C3OUT	—	CMOS	Comparator C3 output.
	T1G	ST	—	Timer1 gate input.
	SDO	—	CMOS	SPI data output.
RB6/TX(1)/CK(1)/SDI(1)/SDA(1)/ ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C™ data input/output.
	ICSPCLK	ST	—	Serial Programming Clock.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See Register 13-1 .
2: All pins have Interrupt-on-Change functionality.

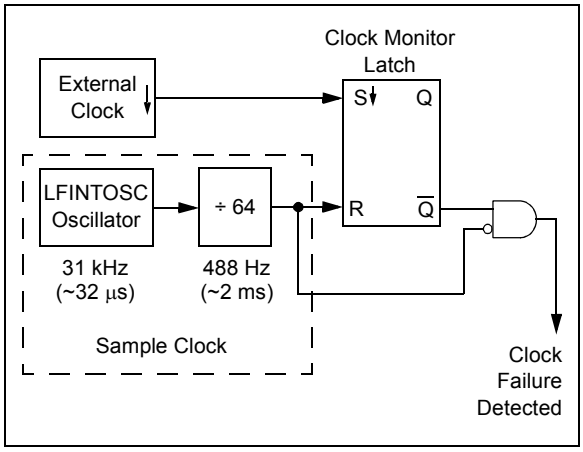
FIGURE 5-3: RESET START-UP SEQUENCE



6.5 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the Configuration Words. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, EC, Timer1 Oscillator and RC).

FIGURE 6-9: FSCM BLOCK DIAGRAM



6.5.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 6-9. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

6.5.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSFIF of the PIR2 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE2 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation.

The internal clock source chosen by the FSCM is determined by the IRCF<3:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

6.5.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a `SLEEP` instruction or changing the SCS bits of the OSCCON register. When the SCS bits are changed, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware.

6.5.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

Note:	Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the Status bits in the OSCSTAT register to verify the oscillator start-up and that the system clock switchover has successfully completed.

REGISTER 8-7: PIR4: PERIPHERAL INTERRUPT REQUEST REGISTER 4

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	PSMC2TIF	PSMC1TIF	—	—	PSMC2SIF	PSMC1SIF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 Unimplemented: Read as '0'

bit 5 PSMC2TIF: PSMC2 Time Base Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 PSMC1TIF: PSMC1 Time Base Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3-2 Unimplemented: Read as '0'

bit 1 PSMC2SIF: PSMC2 Auto-shutdown Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 PSMC1SIF: PSMC1 Auto-shutdown Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	79
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			174
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	80
PIE2	OSEIE	C2IE	C1IE	EEIE	BCL1IE	—	C3IE	CCP2IE	81
—	Unimplemented								—
PIE4	—	—	PSMC2TIE	PSMC1TIE	—	—	PSMC2SIE	PSMC1SIE	82
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	83
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	C3IF	CCP2IF	84
—	Unimplemented								—
PIR4	—	—	PSMC2TIF	PSMC1TIF	—	—	PSMC2SIF	PSMC1SIF	85

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupts.

REGISTER 13-7: ODCONA: PORTA OPEN DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODA7	ODA6	ODA5	ODA4	ODA3	ODA2	ODA1	ODA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 ODA<7:0>: PORTA Open Drain Enable bits
For RA<7:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 13-8: SLRCONA: PORT A SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRA7	SLRA6	SLRA5	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 SLRA<7:0>: PORTA Slew Rate Enable bits
For RA<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 13-9: INLVLA: PORTA INPUT LEVEL CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 INLVLA<7:0>: PORTA Input Level Select bits
For RA<7:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

14.0 INTERRUPT-ON-CHANGE

All pins on all ports can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual pin, or combination of pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 14-1 is a block diagram of the IOC module.

14.1 Enabling the Module

To allow individual pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

14.2 Individual Pin Configuration

For each pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting the associated bits in both of the IOCxP and IOCxN registers.

14.3 Interrupt Flags

The bits located in the IOCxF registers are status flags that correspond to the Interrupt-on-change pins of each port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCxF bits.

14.4 Clearing Interrupt Flags

The individual status flags, (IOCxF register bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 14-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW  0xff
XORWF  IOCAF, W
ANDWF  IOCAF, F
```

14.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the affected IOCxF register will be updated prior to the first instruction executed out of Sleep.

17.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note 1:	The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.
2:	The ADC operates during Sleep only when the FRC oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the GIE and PEIE bits of the INTCON register must be disabled. If the GIE and PEIE bits of the INTCON register are enabled, execution will switch to the Interrupt Service Routine.

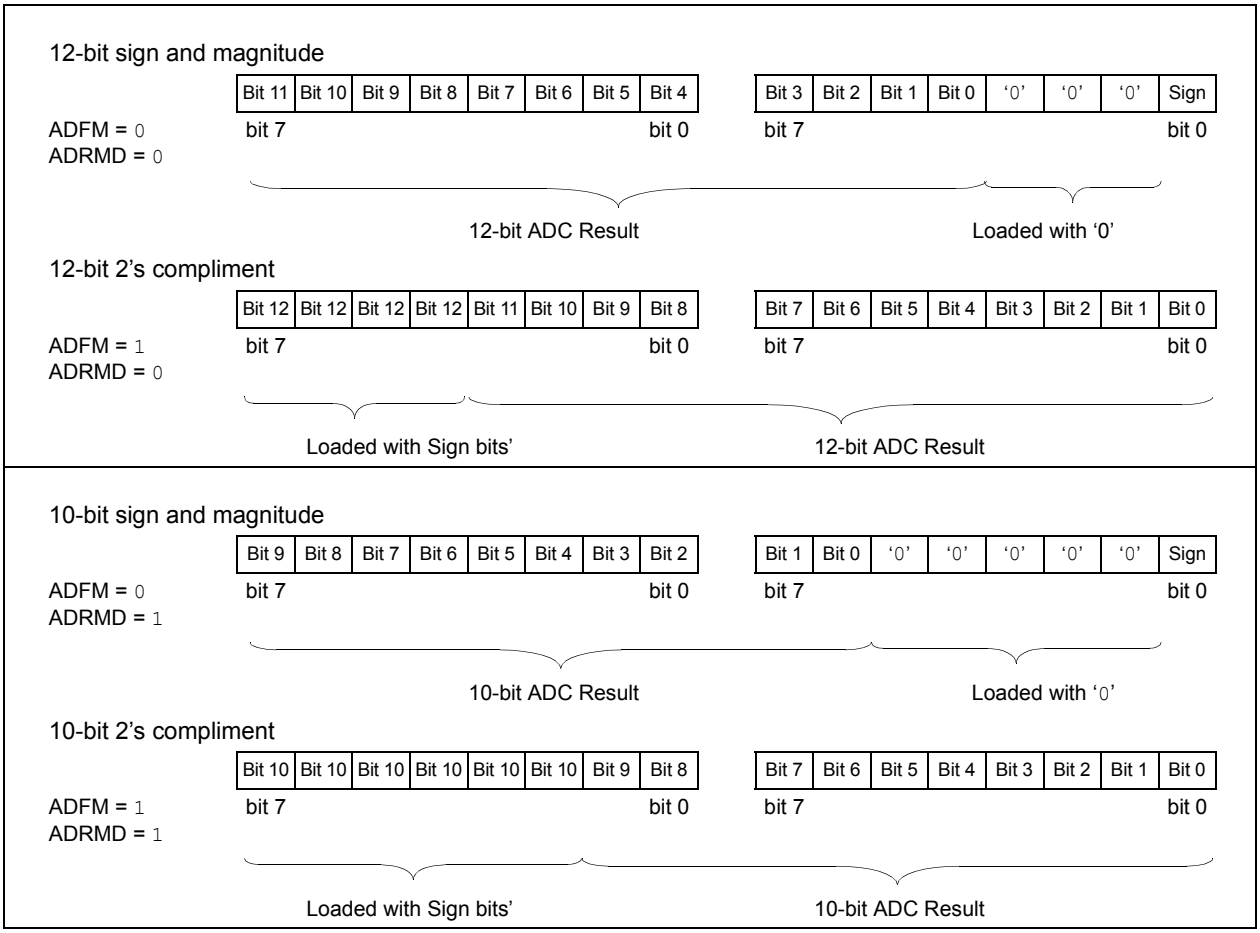
17.1.6 RESULT FORMATTING

The 10-bit and 12-bit ADC conversion results can be supplied in two formats: 2's complement or sign-magnitude. The ADFM bit of the ADCON1 register controls the output format. Sign magnitude is left justified with the sign bit in the LSb position. Negative numbers are indicated when the sign bit is '1'.

Two's complement is right justified with the sign extended into the most significant bits.

Figure 17-3 shows the two output formats. Table 17-2 shows conversion examples.

FIGURE 17-3: ADC CONVERSION RESULT FORMAT



REGISTER 17-6: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADSIGN				AD<11:8>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 ADSIGN: Extended AD Result Sign bit

bit 3-0 AD<11:8>: ADC Result Register bits
Most Significant 4 bits of 12-bit conversion result

REGISTER 17-7: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
AD<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 AD<7:0>: ADC Result Register bits
Least Significant 8 bits of 12-bit conversion result

19.6 Register Definitions: DAC Control

REGISTER 19-1: DACCON0: VOLTAGE RE FERENCE CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
DACEN	—	DACOE1	DACOE2	DACPSS<1:0>		—	DACNSS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 DACEN: DAC Enable bit
1 = DAC is enabled
0 = DAC is disabled

bit 6 Unimplemented: Read as ‘0’

bit 5 DACOE1: DAC Voltage Output 1 Enable bit
1 = DAC voltage level is also an output on the DACOUT1 pin
0 = DAC voltage level is disconnected from the DACOUT1 pin

bit 4 DACOE2: DAC Voltage Output 2 Enable bit
1 = DAC voltage level is also an output on the DACOUT2 pin
0 = DAC voltage level is disconnected from the DACOUT2 pin

bit 3-2 DACPSS<1:0>: DAC Positive Source Select bits
11 = Reserved, do not use
10 = FVR Buffer2 output
01 = V_{REF}+ pin
00 = V_{DD}

bit 1 Unimplemented: Read as ‘0’

bit 0 DACNSS: DAC Negative Source Select bits
1 = V_{REF}- pin
0 = V_{SS}

REGISTER 19-2: DACCON1: VOLTAGE RE FERENCE CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
DACR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 DACR<7:0>: DAC Voltage Output Select bits

20.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- Independent comparator control
- Programmable input selection
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Programmable Speed/Power optimization
- PWM shutdown
- Programmable and fixed voltage reference

20.1 Comparator Overview

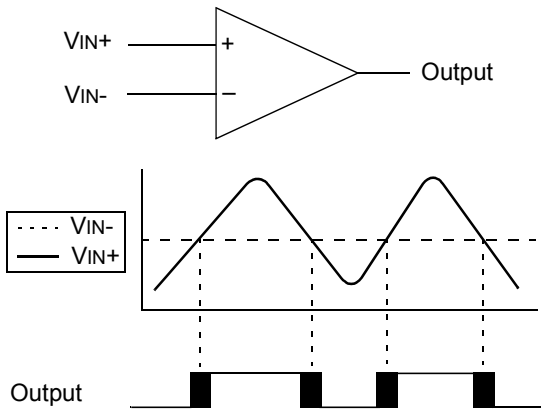
A single comparator is shown in Figure 20-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The comparators available for this device are located in Table 20-1.

TABLE 20-1: COMPARATOR AVAILABILITY PER DEVICE

Device	C1	C2	C3
PIC16(L)F1782	•	•	•
PIC16(L)F1783	•	•	•

FIGURE 20-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

REGISTER 24-9: PSMCxREBS: PSMC RI SING EDGE BLANKED SOURCE REGISTER

R/W-0/0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0
PxREBSIN	—	—	—	PxREBSC3	PxREBSC2	PxREBSC1	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 PxREBSIN: PSMCx Rising Edge Event Blanked from PSMCxIN pin
1 = PSMCxIN pin cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = PSMCxIN pin is not blanked

bit 6-4 Unimplemented: Read as ‘0’

bit 3 PxREBSC3: PSMCx Rising Edge Event Blanked from sync_C3OUT
1 = sync_C3OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C3OUT is not blanked

bit 2 PxREBSC2: PSMCx Rising Edge Event Blanked from sync_C2OUT
1 = sync_C2OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C2OUT is not blanked

bit 1 PxREBSC1: PSMCx Rising Edge Event Blanked from sync_C1OUT
1 = sync_C1OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C1OUT is not blanked

bit 0 Unimplemented: Read as ‘0’

REGISTER 24-10: PSMCxFEBS: PSMC FALLING EDGE BLANKED SOURCE REGISTER

R/W-0/0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0
PxFEBSIN	—	—	—	PxFEBSC3	PxFEBSC2	PxFEBSC1	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 PxFEBSIN: PSMCx Falling Edge Event Blanked from PSMCxIN pin
1 = PSMCxIN pin cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = PSMCxIN pin is not blanked

bit 6-4 Unimplemented: Read as ‘0’

bit 3 PxFEBSC3: PSMCx Falling Edge Event Blanked from sync_C3OUT
1 = sync_C3OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C3OUT is not blanked

bit 2 PxFEBSC2: PSMCx Falling Edge Event Blanked from sync_C2OUT
1 = sync_C2OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C2OUT is not blanked

bit 1 PxFEBSC1: PSMCx Falling Edge Event Blanked from sync_C1OUT
1 = sync_C1OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C1OUT is not blanked

bit 0 Unimplemented: Read as ‘0’

REGISTER 24-32: PSMCxINT: PSMC TIME BASE INTERRUPT CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PxTOVIE	PxTPHIE	PxTDCIE	PxTPRIE	PxTOVIF	PxTPHIF	PxTDCIF	PxTPRIF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 PxTOVIE: PSMC Time Base Counter Overflow Interrupt Enable bit
- 1 = Time base counter overflow interrupts are enabled
- 0 = Time base counter overflow interrupts are disabled

bit 6 PxTPHIE: PSMC Time Base Phase Interrupt Enable bit
- 1 = Time base phase match interrupts are enabled
- 0 = Time base phase match interrupts are disabled

bit 5 PxTDCIE: PSMC Time Base Duty Cycle Interrupt Enable bit
- 1 = Time base duty cycle match interrupts are enabled
- 0 = Time base duty cycle match interrupts are disabled

bit 4 PxTPRIE: PSMC Time Base Period Interrupt Enable bit
- 1 = Time base period match interrupts are enabled
- 0 = Time base period match Interrupts are disabled

bit 3 PxTOVIF: PSMC Time Base Counter Overflow Interrupt Flag bit
- 1 = The 16-bit PSMCxTMR has overflowed from FFFFh to 0000h
- 0 = The 16-bit PSMCxTMR counter has not overflowed

bit 2 PxTPHIF: PSMC Time Base Phase Interrupt Flag bit
- 1 = The 16-bit PSMCxTMR counter has matched PSMCxPH<15:0>
- 0 = The 16-bit PSMCxTMR counter has not matched PSMCxPH<15:0>

bit 1 PxTDCIF: PSMC Time Base Duty Cycle Interrupt Flag bit
- 1 = The 16-bit PSMCxTMR counter has matched PSMCxDC<15:0>
- 0 = The 16-bit PSMCxTMR counter has not matched PSMCxDC<15:0>

bit 0 PxTPRIF: PSMC Time Base Period Interrupt Flag bit
- 1 = The 16-bit PSMCxTMR counter has matched PSMCxPR<15:0>
- 0 = The 16-bit PSMCxTMR counter has not matched PSMCxPR<15:0>

26.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSPCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

26.5.6.1 Normal Clock Stretching

Following an $\overline{ACK}$ if the R/$\overline{W}$ bit of SSPSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPBUF with data to transfer to the master. If the SEN bit of SSPCON2 is set, the slave hardware will always stretch the clock after the $\overline{ACK}$ sequence. Once the slave is ready; CKP is set by software and communication resumes.

Note 1:	The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPBUF was read before the 9th falling edge of SCL.
2:	Previous versions of the module did not stretch the clock for a transmission if SSPBUF was loaded before the 9th falling edge of SCL. It is now always cleared for read requests.

26.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPADD.

Note:	Previous versions of the module did not stretch the clock if the second address byte did not match.

26.5.6.3 Byte NACKing

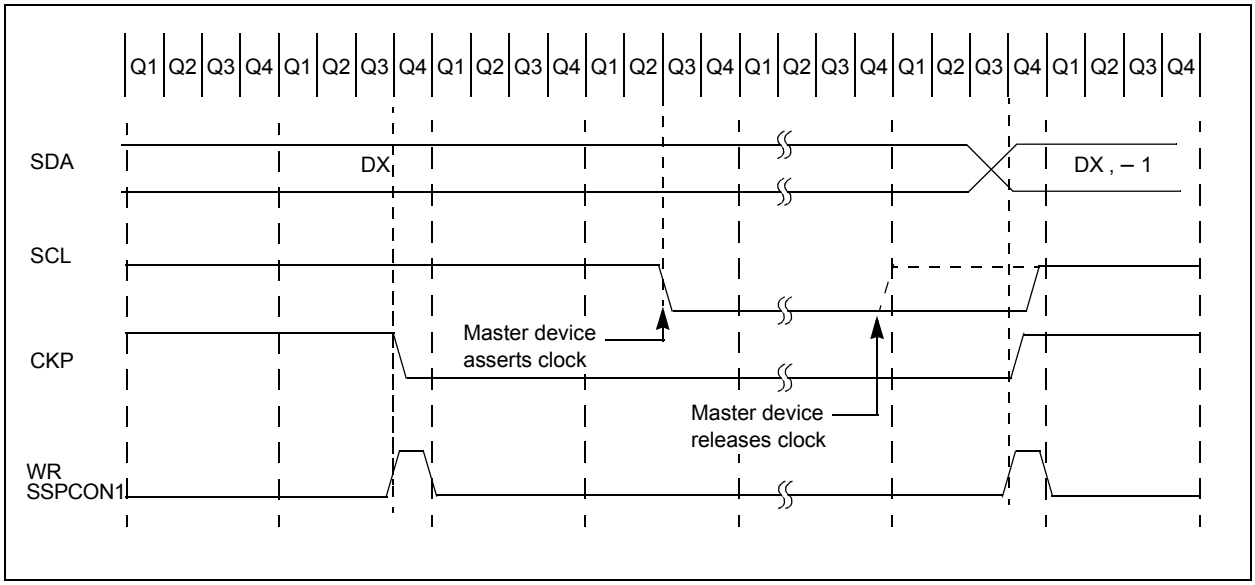
When AHEN bit of SSPCON3 is set; CKP is cleared by hardware after the 8th falling edge of SCL for a received matching address byte. When DHEN bit of SSPCON3 is set; CKP is cleared after the 8th falling edge of SCL for received data.

Stretching after the 8th falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

26.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I^2C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 26-22).

FIGURE 26-23: CLOCK SYNCHRONIZATION TIMING



26.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 26-29).

26.6.8.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

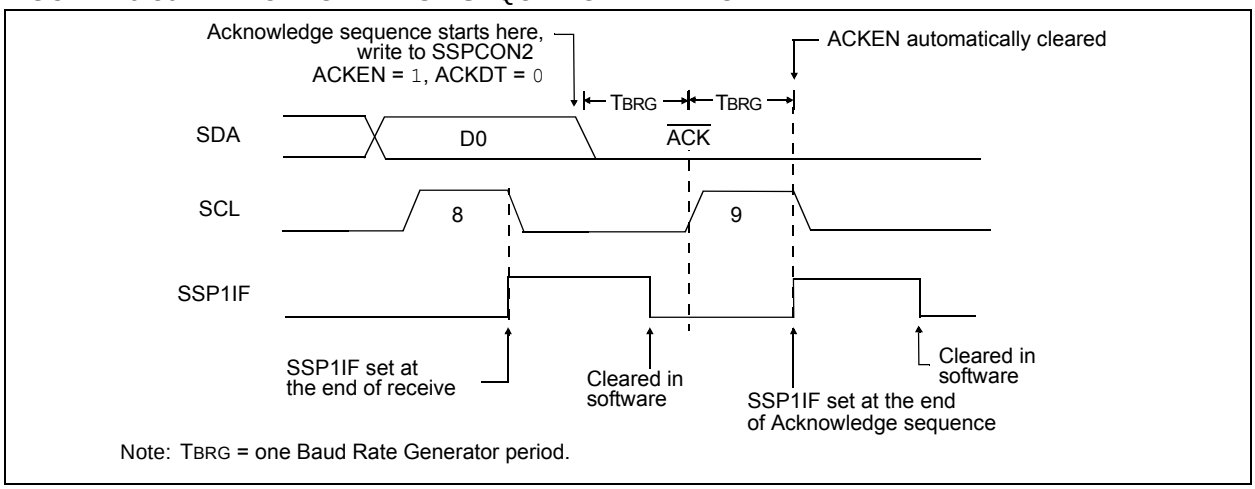
26.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPSTAT register is set. A TBRG later, the PEN bit is cleared and the SSP1IF bit is set (Figure 26-30).

26.6.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 26-30: ACKNOWLEDGE SEQUEN CE WAVEFORM



Note: TBRG = one Baud Rate Generator period.

REGISTER 26-3: SSPCON2: SSP CONTROL REGISTER 2

R/W-0/0	R-0/0	R/W-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/W/HS-0/0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Cleared by hardware S = User set

bit 7 GCEN: General Call Enable bit (in I^2C Slave mode only)
1 = Enable interrupt when a general call address (0x00 or 00h) is received in the SSPSR
0 = General call address disabled

bit 6 ACKSTAT: Acknowledge Status bit (in I^2C mode only)
1 = Acknowledge was not received
0 = Acknowledge was received

bit 5 ACKDT: Acknowledge Data bit (in I^2C mode only)
In Receive mode:
Value transmitted when the user initiates an Acknowledge sequence at the end of a receive
1 = Not Acknowledge
0 = Acknowledge

bit 4 ACKEN: Acknowledge Sequence Enable bit (in I^2C Master mode only)
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit. Automatically cleared by hardware.
0 = Acknowledge sequence idle

bit 3 RCEN: Receive Enable bit (in I^2C Master mode only)
1 = Enables Receive mode for I^2C
0 = Receive idle

bit 2 PEN: Stop Condition Enable bit (in I^2C Master mode only)
SCKMSSP Release Control:
1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Stop condition Idle

bit 1 RSEN: Repeated Start Condition Enable bit (in I^2C Master mode only)
1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated Start condition Idle

bit 0 SEN: Start Condition Enable/Stretch Enable bit
In Master mode:
1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Start condition Idle
In Slave mode:
1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)
0 = Clock stretching is disabled

Note 1: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I^2C module is not in the Idle mode, this bit may not be set (no spooling) and the SSPBUF may not be written (or writes to the SSPBUF are disabled).

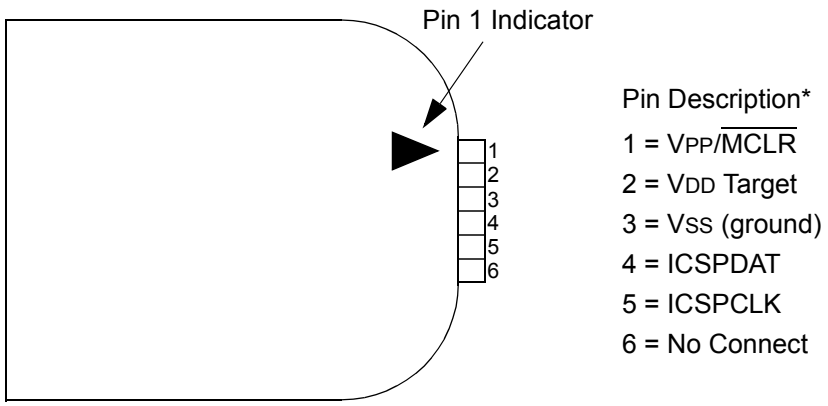
TABLE 27-2: SUMMARY OF REGISTERS ASSO CIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	111
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	322
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	79
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	80
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	83
RCREG	EUSART Receive Data Register								315*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	321
SPBRGL	BRG<7:0>								323
SPBRGH	BRG<15:8>								323
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	125
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	320

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for asynchronous reception.

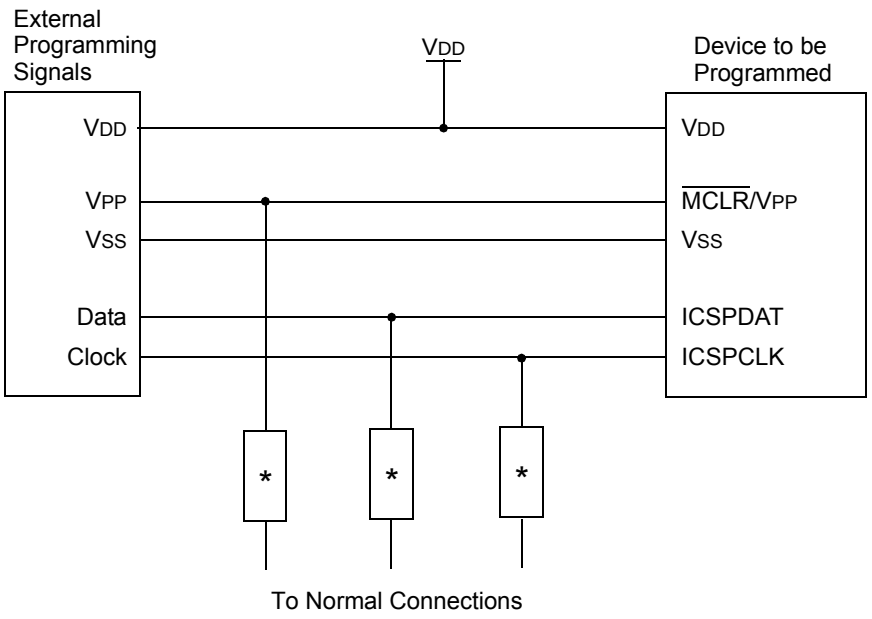
* Page provides register information.

FIGURE 28-2: PICkit PROGRAMME R STYLE CONNECTOR INTERFACE



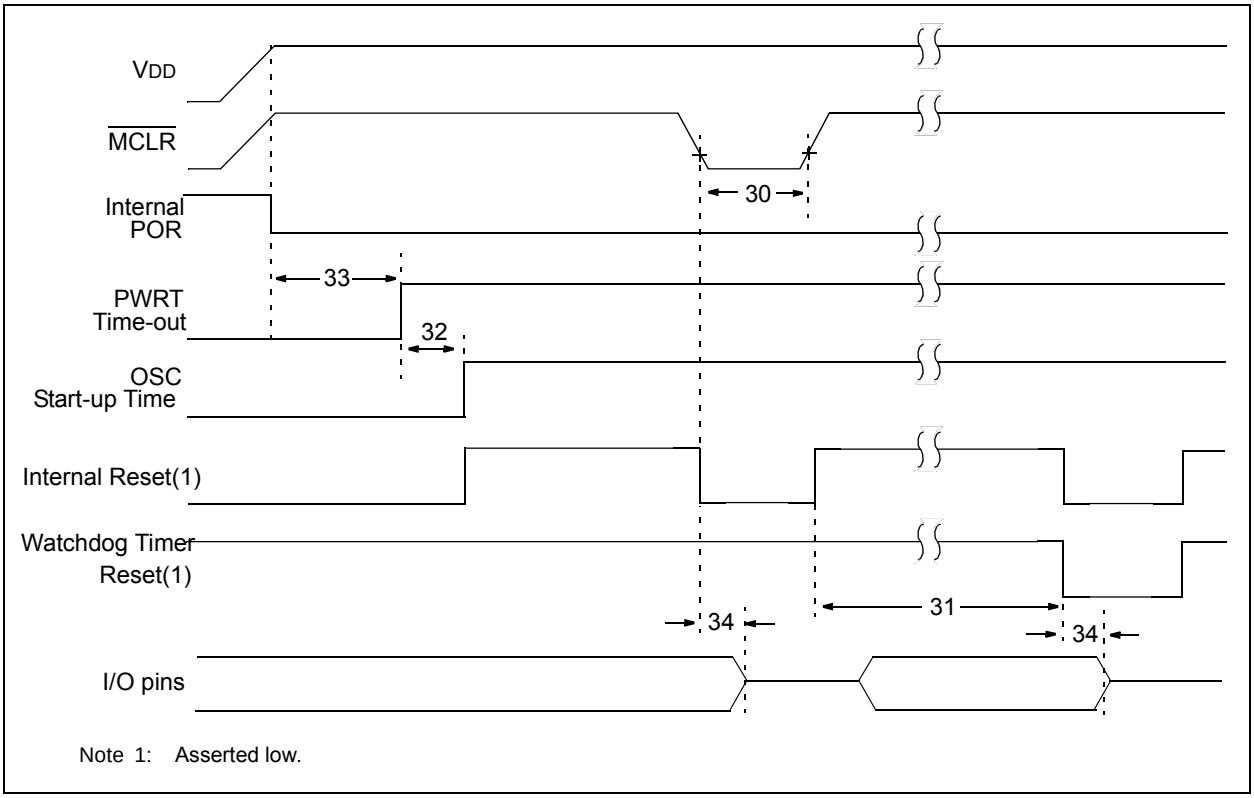
* The 6-pin header (0.100" spacing) accepts 0.025" square pins.

FIGURE 28-3: TYPICAL CONNECTION FOR ICSP PROGRAMMING



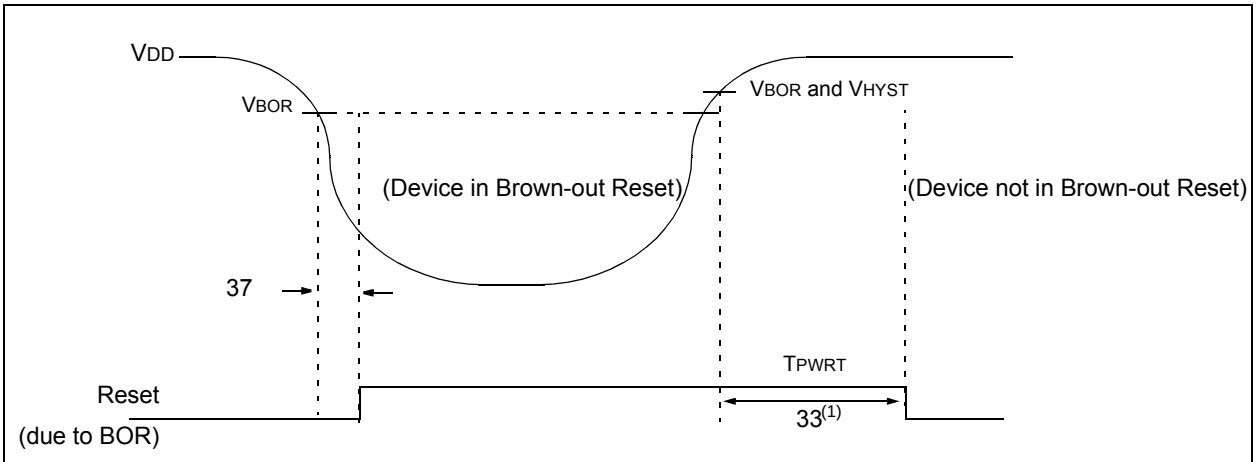
* Isolation devices (as required).

FIGURE 30-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note 1: Asserted low.

FIGURE 30-9: BROWN-OUT RESET TIMING AND CHARACTERISTICS



Note 1: The delay, (TPWRT) releasing Reset, only occurs when the Power-up Timer is enabled, ($\overline{PWRTE}$ = 0).