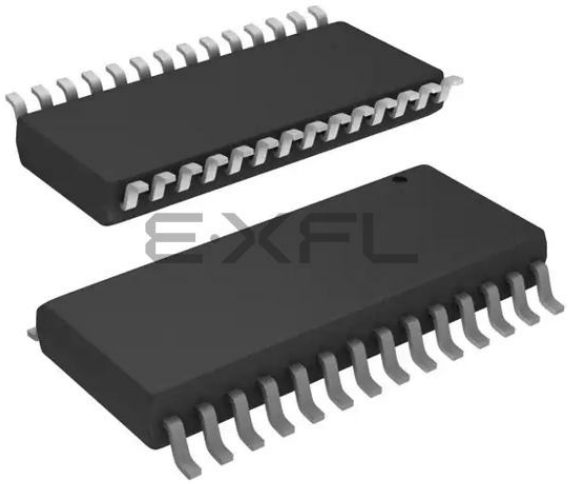
Microchip Technology - PIC16LF1782-I/SO Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1782-i-so

FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1782

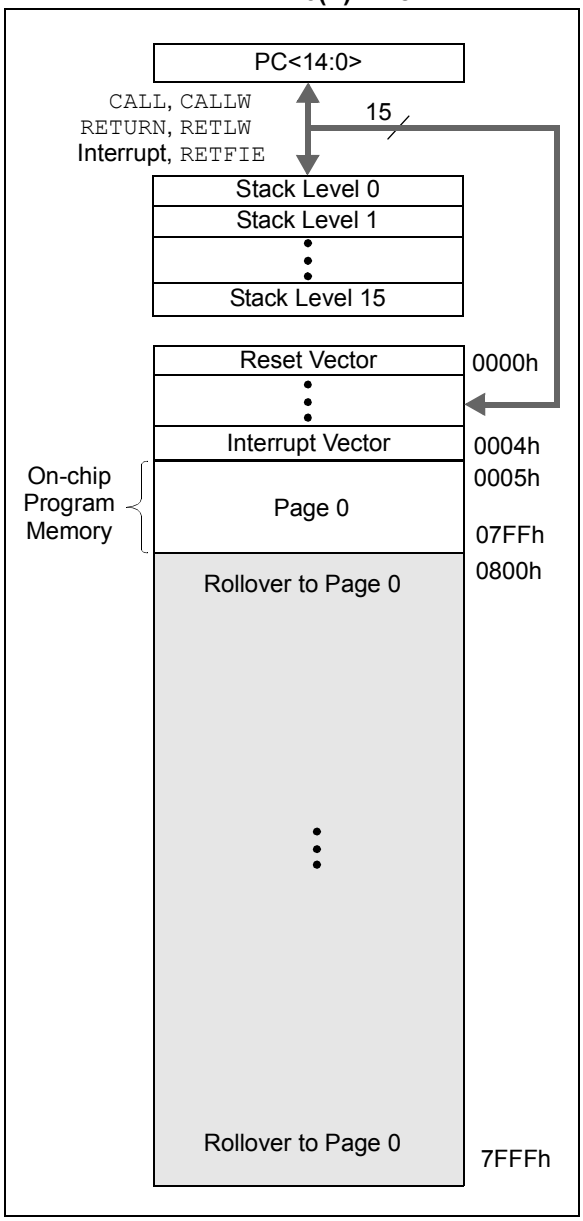
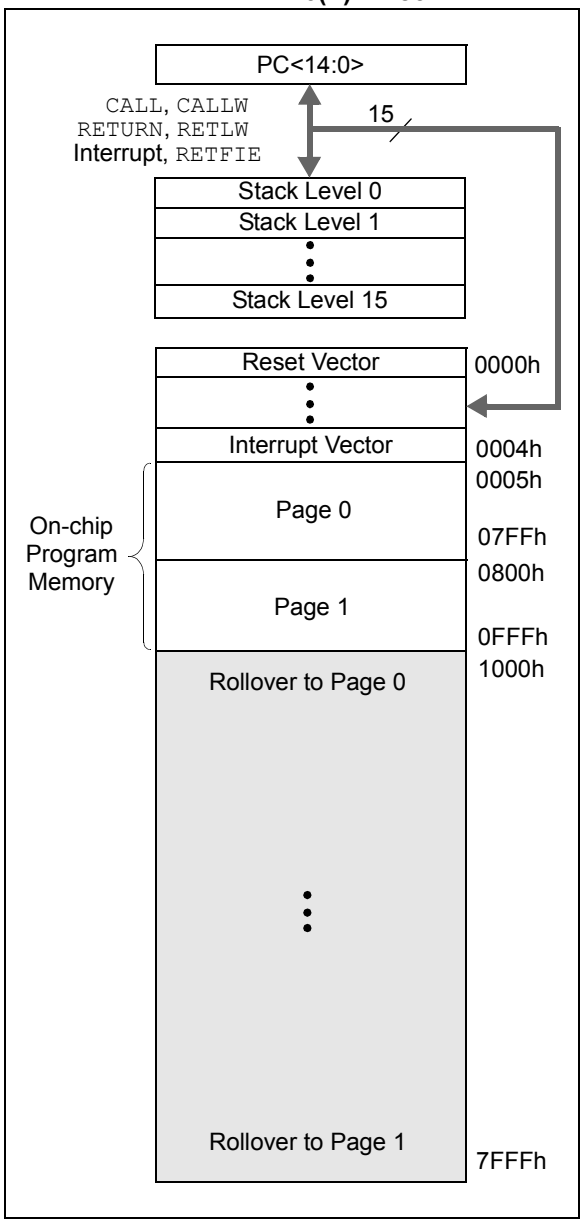


FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1783



3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):

- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 3.6 "Indirect Addressing"** for more information.

Data memory uses a 12-bit address. The upper 5 bits of the address define the Bank address and the lower 7 bits select the registers/RAM in that bank.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-7.

TABLE 3-2: CORE REGISTERS

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

6.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 16 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 6-3).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). One of multiple frequencies derived from the HFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 6.2.2.7 "Internal Oscillator Clock Switch Timing"** for more information.

The HFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'.

A fast startup oscillator allows internal circuits to power up and stabilize before switching to HFINTOSC.

The High Frequency Internal Oscillator Ready bit (HFIOFR) of the OSCSTAT register indicates when the HFINTOSC is running.

The High Frequency Internal Oscillator Status Locked bit (HFIOFL) of the OSCSTAT register indicates when the HFINTOSC is running within 2% of its final value.

The High Frequency Internal Oscillator Stable bit (HFIOFS) of the OSCSTAT register indicates when the HFINTOSC is running within 0.5% of its final value.

6.2.2.2 MFINTOSC

The Medium-Frequency Internal Oscillator (MFINTOSC) is a factory calibrated 500 kHz internal clock source. The frequency of the MFINTOSC can be altered via software using the OSCTUNE register (Register 6-3).

The output of the MFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). One of nine frequencies derived from the MFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 6.2.2.7 "Internal Oscillator Clock Switch Timing"** for more information.

The MFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

The Medium Frequency Internal Oscillator Ready bit (MFIOFR) of the OSCSTAT register indicates when the MFINTOSC is running.

6.2.2.3 Internal Oscillator Frequency Adjustment

The 500 kHz internal oscillator is factory calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 6-3). Since the HFINTOSC and MFINTOSC clock sources are derived from the 500 kHz internal oscillator a change in the OSCTUNE register value will apply to both.

The default value of the OSCTUNE register is '0'. The value is a 6-bit two's complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

6.2.2.4 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source.

The output of the LFINTOSC connects to a multiplexer (see Figure 6-1). Select 31 kHz, via software, using the IRCF<3:0> bits of the OSCCON register. See **Section 6.2.2.7 "Internal Oscillator Clock Switch Timing"** for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<3:0> bits of the OSCCON register = 000) as the system clock source (SCS bits of the OSCCON register = 1x), or when any of the following are enabled:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired LF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

Peripherals that use the LFINTOSC are:

- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The Low-Frequency Internal Oscillator Ready bit (LFIOFR) of the OSCSTAT register indicates when the LFINTOSC is running.

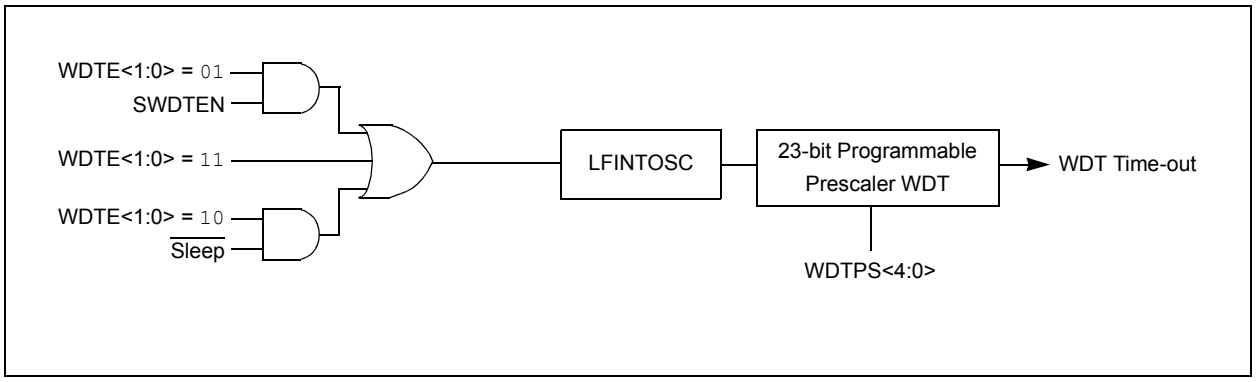
11.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- Independent clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Multiple Reset conditions
- Operation during Sleep

FIGURE 11-1: WATCHDOG TIMER BLOCK DIAGRAM



12.3.2 ERASING FLASH PROGRAM MEMORY

While executing code, program memory can only be erased by rows. To erase a row:

1. Load the EEADRH:EEADRL register pair with the address of new row to be erased.
2. Clear the CFGS bit of the EECON1 register.
3. Set the EEPGD, FREE, and WREN bits of the EECON1 register.
4. Write 55h, then AAh, to EECON2 (Flash programming unlock sequence).
5. Set control bit WR of the EECON1 register to begin the erase operation.
6. Poll the FREE bit in the EECON1 register to determine when the row erase has completed.

See Example 12-4.

After the "`BSF EECON1,WR`" instruction, the processor requires two cycles to set up the erase operation. The user must place two `NOP` instructions after the WR bit is set. The processor will halt internal operations for the typical 2 ms erase time. This is not Sleep mode as the clocks and peripherals will continue to run. After the erase cycle, the processor will resume operation with the third instruction after the EECON1 write instruction.

12.3.3 WRITING TO FLASH PROGRAM MEMORY

Program memory is programmed using the following steps:

1. Load the starting address of the word(s) to be programmed.
2. Load the write latches with data.
3. Initiate a programming operation.
4. Repeat steps 1 through 3 until all data is written.

Before writing to program memory, the word(s) to be written must be erased or previously unwritten. Program memory can only be erased one row at a time. No automatic erase occurs upon the initiation of the write.

Program memory can be written one or more words at a time. The maximum number of words written at one time is equal to the number of write latches. See Figure 12-2 (block writes to program memory with 32 write latches) for more details. The write latches are aligned to the address boundary defined by EEADRL as shown in Table 12-1. Write operations do not cross these boundaries. At the completion of a program memory write operation, the write latches are reset to contain 0x3FFF.

The following steps should be completed to load the write latches and program a block of program memory. These steps are divided into two parts. First, all write latches are loaded with data except for the last program memory location. Then, the last write latch is loaded and the programming sequence is initiated. A special unlock sequence is required to load a write latch with data or initiate a Flash programming operation. This unlock sequence should not be interrupted.

1. Set the EEPGD and WREN bits of the EECON1 register.
2. Clear the CFGS bit of the EECON1 register.
3. Set the LWLO bit of the EECON1 register. When the LWLO bit of the EECON1 register is '`1`', the write sequence will only load the write latches and will not initiate the write to Flash program memory.
4. Load the EEADRH:EEADRL register pair with the address of the location to be written.
5. Load the EEDATH:EEDATL register pair with the program memory data to be written.
6. Write 55h, then AAh, to EECON2, then set the WR bit of the EECON1 register (Flash programming unlock sequence). The write latch is now loaded.
7. Increment the EEADRH:EEADRL register pair to point to the next location.
8. Repeat steps 5 through 7 until all but the last write latch has been loaded.
9. Clear the LWLO bit of the EECON1 register. When the LWLO bit of the EECON1 register is '`0`', the write sequence will initiate the write to Flash program memory.
10. Load the EEDATH:EEDATL register pair with the program memory data to be written.
11. Write 55h, then AAh, to EECON2, then set the WR bit of the EECON1 register (Flash programming unlock sequence). The entire latch block is now written to Flash program memory.

It is not necessary to load the entire write latch block with user program data. However, the entire write latch block will be written to program memory.

An example of the complete write sequence for eight words is shown in Example 12-5. The initial address is loaded into the EEADRH:EEADRL register pair; the eight words of data are loaded using indirect addressing.

After the "`BSF EECON1,WR`" instruction, the processor requires two cycles to set up the write operation. The user must place two `NOP` instructions after the WR bit is set. The processor will halt internal operations for the typical 2 ms, only during the cycle in which the write takes place (i.e., the last word of the block write). This is not Sleep mode as the clocks and peripherals will continue to run. The processor does not stall when LWLO = `1`, loading the write latches. After the write cycle, the processor will resume operation with the third instruction after the EECON1 `WRITE` instruction.

13.9 PORTE Registers

RE3 is input only, and also functions as $\overline{MCLR}$. The $\overline{MCLR}$ feature can be disabled via a configuration fuse. RE3 also supplies the programming voltage. The TRIS bit for RE3 (TRISE3) always reads '1'.

13.9.1 INPUT THRESHOLD CONTROL

The INLVLE register (Register 13-28) controls the input voltage threshold for each of the available PORTE input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTE register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See **Section TABLE 30-1: "Supply Voltage"** for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

13.9.2 PORTE FUNCTIONS AND OUTPUT PRIORITIES

No output priorities. RE3 is an input-only pin.

REGISTER 13-27: WPUE: WEAK PULL-UP PORTE REGISTER

U-0	U-0	U-0	U-0	R/W-1/1	U-0	U-0	U-0
—	—	—	—	WPUE3	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **WPUE3:** Weak Pull-up Register bit
1 = Pull-up enabled
0 = Pull-up disabled

bit 2-0 **Unimplemented:** Read as '0'

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

REGISTER 13-28: INLVLE: PORTE INPUT LEVEL CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-1/1	U-0	U-0	U-0
—	—	—	—	INLVLE3	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **INLVLE3:** PORTE Input Level Select bit(1)
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

bit 2-0 **Unimplemented:** Read as '0'

TABLE 13-9: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	ADRMD	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	147
INLVLE	—	—	—	—	INLVLE3	—	—	—	130
PORTE	—	—	—	—	RE3	—	—	—	129
TRISE	—	—	—	—	—(1)	—	—	—	129
WPUE	—	—	—	—	WPUE3	—	—	—	130

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTE.
Note 1: Unimplemented, read as '1'.
2: PIC16(L)F1783 only

17.3 Register Definitions: ADC Control

REGISTER 17-1: ADCON0: ADC CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ADRMD	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ADRMD:** ADC Result Mode bit
1 = ADRESL and ADRESH provide data formatted for a 10-bit result
0 = ADRESL and ADRESH provide data formatted for a 12-bit result
See Figure 17-3 for details

bit 6-2 **CHS<4:0>:** Positive Differential Input Channel Select bits
11111 = FVR (Fixed Voltage Reference) Buffer 1 Output(3)
11110 = DAC_output(2)
11101 = Temperature Indicator(4)
11100 = Reserved. No channel connected.
•
•
•
01110 = Reserved. No channel connected.
01101 = AN13
01100 = AN12
01011 = AN11
01010 = AN10
01001 = AN9
01000 = AN8
00111 = Reserved. No channel connected.
00110 = Reserved. No channel connected.
00101 = Reserved. No channel connected.
00100 = AN4
00011 = AN3
00010 = AN2
00001 = AN1
00000 = AN0

bit 1 **GO/$\overline{\text{DONE}}$:** ADC Conversion Status bit
1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle.
This bit is automatically cleared by hardware when the ADC conversion has completed.
0 = ADC conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

Note 1: See **Section 19.0 "Digital-to-Analog Converter (DAC) Module"** for more information.
2: See **Section 15.0 "Fixed Voltage Reference (FVR)"** for more information.
3: See **Section 16.0 "Temperature Indicator Module"** for more information.

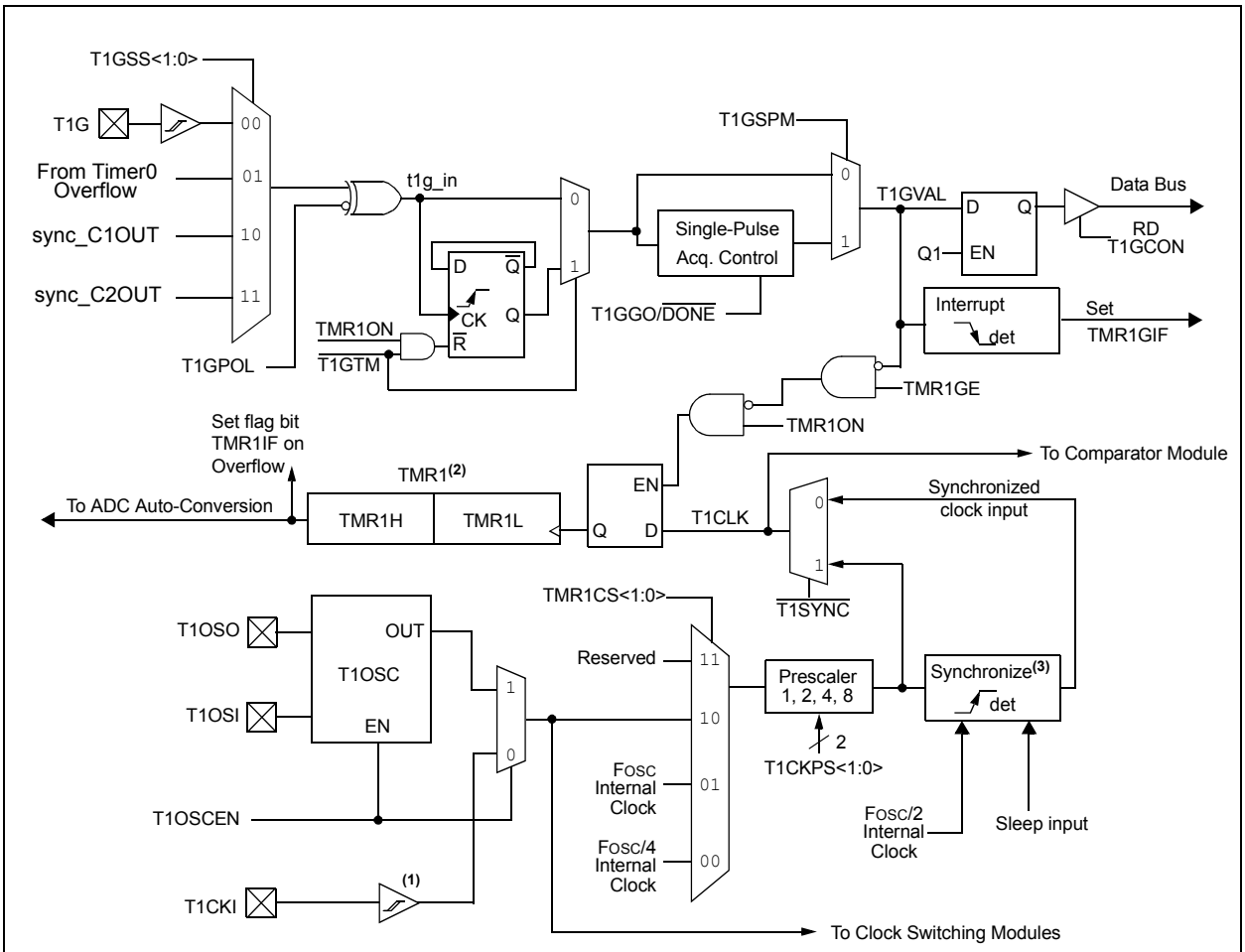
22.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 2-bit prescaler
- Dedicated 32 kHz oscillator circuit
- Optionally synchronized comparator out
- Multiple Timer1 gate (count enable) sources
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Auto-conversion Trigger (with CCP)
- Selectable Gate Source Polarity
- Gate Toggle mode
- Gate Single-pulse mode
- Gate Value Status
- Gate Event Interrupt

Figure 22-1 is a block diagram of the Timer1 module.

FIGURE 22-1: TIMER1 BLOCK DIAGRAM



Note 1: ST Buffer is high speed type when using T1CKI.
2: Timer1 register increments on rising edge.
3: Synchronize does not operate while in Sleep.

REGISTER 22-2: T1GCON: TIMER1 GATE CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W/HC-0/u	R-x/x	R/W-0/u	R/W-0/u
TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **TMR1GE:** Timer1 Gate Enable bit

If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 counting is controlled by the Timer1 gate function
0 = Timer1 counts regardless of Timer1 gate function

bit 6 **T1GPOL:** Timer1 Gate Polarity bit

1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 5 **T1GTM:** Timer1 Gate Toggle Mode bit

1 = Timer1 Gate Toggle mode is enabled
0 = Timer1 Gate Toggle mode is disabled and toggle flip-flop is cleared
Timer1 gate flip-flop toggles on every rising edge.

bit 4 **T1GSPM:** Timer1 Gate Single-Pulse Mode bit

1 = Timer1 Gate Single-Pulse mode is enabled and is controlling Timer1 gate
0 = Timer1 Gate Single-Pulse mode is disabled

bit 3 **T1GGO/$\overline{\text{DONE}}$:** Timer1 Gate Single-Pulse Acquisition Status bit

1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge
0 = Timer1 gate single-pulse acquisition has completed or has not been started

bit 2 **T1GVAL:** Timer1 Gate Current State bit

Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L.
Unaffected by Timer1 Gate Enable (TMR1GE).

bit 1-0 **T1GSS<1:0>:** Timer1 Gate Source Select bits

11 = Comparator 2 optionally synchronized output (sync_C2OUT)
10 = Comparator 1 optionally synchronized output (sync_C1OUT)
01 = Timer0 overflow output
00 = Timer1 gate pin

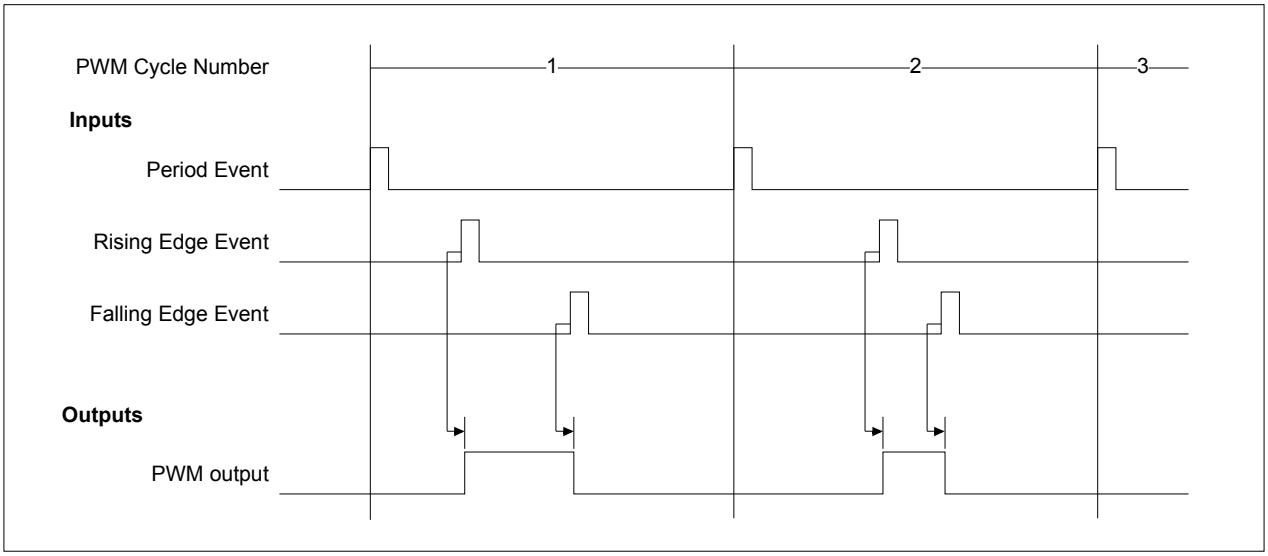
24.1 Fundamental Operation

PSMC operation is based on the sequence of three events:

- Period Event – Determines the frequency of the active signal.
- Rising Edge Event – Determines start of the active pulse. This is also referred to as the phase.
- Falling Edge Event – Determines the end of the active pulse. This is also referred to as the duty cycle.

The basic waveform generated from these events is shown in Figure 24-2.

FIGURE 24-2: BASIC PWM WAVEFORM GENERATION



Each of the three types of events is triggered by a user selectable combination of synchronous timed and asynchronous external inputs.

Asynchronous event inputs may come directly from an input pin or through the comparators.

Synchronous timed events are determined from the PSMCxTMR counter, which is derived from internal clock sources. See **Section 24.2.5 "PSMC Time Base Clock Sources"** for more detail.

The active pulse stream can be further modulated by one of several internal or external sources:

- Register control bit
- Comparator output
- CCP output
- Input pin

User selectable deadtime can be inserted in the drive outputs to prevent shoot through of configurations with two devices connected in series between the supply rails.

Applications requiring very small frequency granularity control when the PWM frequency is large can do so with the fractional frequency control available in the variable frequency fixed Duty Cycle modes.

PSMC operation can be quickly terminated without software intervention by the auto-shutdown control. Auto-shutdown can be triggered by any combination of the following:

- PSMCxIN pin
- sync_C1OUT
- sync_C2OUT
- sync_C3OUT

24.3.12 3-PHASE PWM

The 3-Phase mode of operation is used in 3-phase power supply and motor drive applications configured as three half-bridges. A half-bridge configuration consists of two power driver devices in series, between the positive power rail (high side) and negative power rail (low side). The three outputs come from the junctions between the two drivers in each half-bridge. When the steering control selects a phase drive, power flows from the positive rail through a high-side power device to the load and back to the power supply through a low-side power device.

In this mode of operation, all six PSMC outputs are used, but only two are active at a time.

The two active outputs consist of a high-side driver and low-side driver output.

24.3.12.1 Mode Features

- No dead-band control is available
- PWM can be steered to the following six pairs:
  - PSMCxA and PSMCxD
  - PSMCxA and PSMCxF
  - PSMCxC and PSMCxF
  - PSMCxC and PSMCxB
  - PSMCxE and PSMCxB
  - PSMCxE and PSMCxD

24.3.12.2 Waveform Generation

3-phase steering has a more complex waveform generation scheme than the other modes. There are several factors which go into what waveforms are created.

The PSMC outputs are grouped into three sets of drivers: one for each phase. Each phase has two associated PWM outputs: one for the high-side drive and one for the low-side drive.

High Side drives are indicated by 1H, 2H and 3H.

Low Side drives are indicated by 1L, 2L, 3L.

Phase grouping is mapped as shown in Table 24-1. There are six possible phase drive combinations. Each phase drive combination activates two of the six outputs and deactivates the other four. Phase drive is selected with the steering control as shown in Table 24-2.

TABLE 24-1: PHASE GROUPING

PSMC grouping	
PSMCxA	1H
PSMCxB	1L
PSMCxC	2H
PSMCxD	2L
PSMCxE	3H
PSMCxF	3L

TABLE 24-2: 3-PHASE STEERING CONTROL

		PSMCxSTR0 Value(1)						
PSMC outputs		**00h**	**01h**	**02h**	**04h**	**08h**	**10h**	**20h**
PSMCxA	1H	inactive	**active**	**active**	inactive	inactive	inactive	inactive
PSMCxB	1L	inactive	inactive	inactive	inactive	**active**	**active**	inactive
PSMCxC	2H	inactive	inactive	inactive	**active**	**active**	inactive	inactive
PSMCxD	2L	inactive	**active**	inactive	inactive	inactive	inactive	**active**
PSMCxE	3H	inactive	inactive	inactive	inactive	inactive	**active**	**active**
PSMCxF	3L	inactive	inactive	**active**	**active**	inactive	inactive	inactive

Note 1: Steering for any value other than those shown will default to the output combination of the Least Significant steering bit that is set.

High/Low Side Modulation Enable

It is also possible to enable the PWM output on the low side or high side drive independently using the PxLSMEN and PXHSMEN bits of the PSMC Steering Control 1 (PSMCxSTR1) register (Register 24-31).

When the PxHSMEN bit is set, the active-high side output listed in Table 24-2 is modulated using the normal rising edge and falling edge events.

When the PxLSMEN bit is set, the active-low side output listed in Table 24-2 is modulated using the normal rising edge and falling edge events.

When both the PxHSMEN and PxLSMEN bits are cleared, the active outputs listed in Table 24-2 go immediately to the rising edge event states and do not change.

Rising Edge Event

- Active outputs are set to their active states

Falling Edge Event

- Active outputs are set to their inactive state

24.10 Register Updates

There are 10 double-buffered registers that can be updated “on the fly”. However, due to the asynchronous nature of the potential updates, a special hardware system is used for the updates.

There are two operating cases for the PSMC:

- module is enabled
- module is disabled

24.10.1 DOUBLE BUFFERED REGISTERS

The double-buffered registers that are affected by the special hardware update system are:

- PSMCxPRL
- PSMCxPRH
- PSMCxDCL
- PSMCxDCH
- PSMCxPHL
- PSMCxPHH
- PSMCxDBR
- PSMCxDBF
- PSMCxBLKR
- PSMCxBLKF
- PSMCxSTR0 (when the PxSSYNC bit is set)

24.10.2 MODULE DISABLED UPDATES

When the PSMC module is disabled (PSMCxEN = 0), any write to one of the buffered registers will also write directly to the buffer. This means that all buffers are loaded and ready for use when the module is enabled.

24.10.3 MODULE ENABLED UPDATES

When the PSMC module is enabled (PSMCxEN = 1), the PSMCxLD bit of the PSMC Control (PSMCxCON) register (Register 24-1) must be used.

When the PSMCxLD bit is set, the transfer from the register to the buffer occurs on the next period event. The PSMCxLD bit is automatically cleared by hardware after the transfer to the buffers is complete.

The reason that the PSMCxLD bit is required is that depending on the customer application and operation conditions, all 10 registers may not be updated in one PSMC period. If the buffers are loaded at different times (i.e., DCL gets updated, but DCH does not OR DCL and DCL are updated by PRH and PRL are not), then unintended operation may occur.

The sequence for loading the buffer registers when the PSMC module is enabled is as follows:

1. Software updates all registers.
2. Software sets the PSMCxLD bit.
3. Hardware updates all buffers on the next period event.
4. Hardware clears PSMCxLD bit.

24.11 Operation During Sleep

The PSMC continues to operate in Sleep with the following clock sources:

- Internal 64 MHz
- External clock

FIGURE 26-3: MSSP BLOCK DIAGRAM (I^2C™ SLAVE MODE)

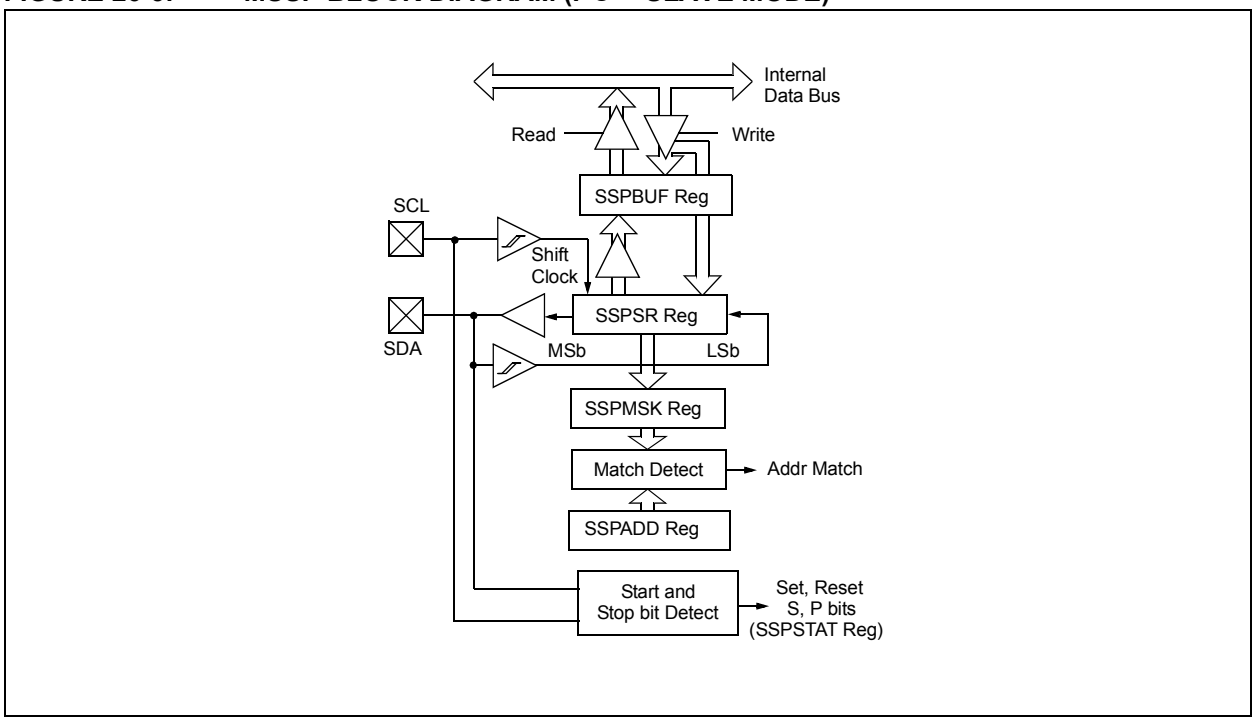
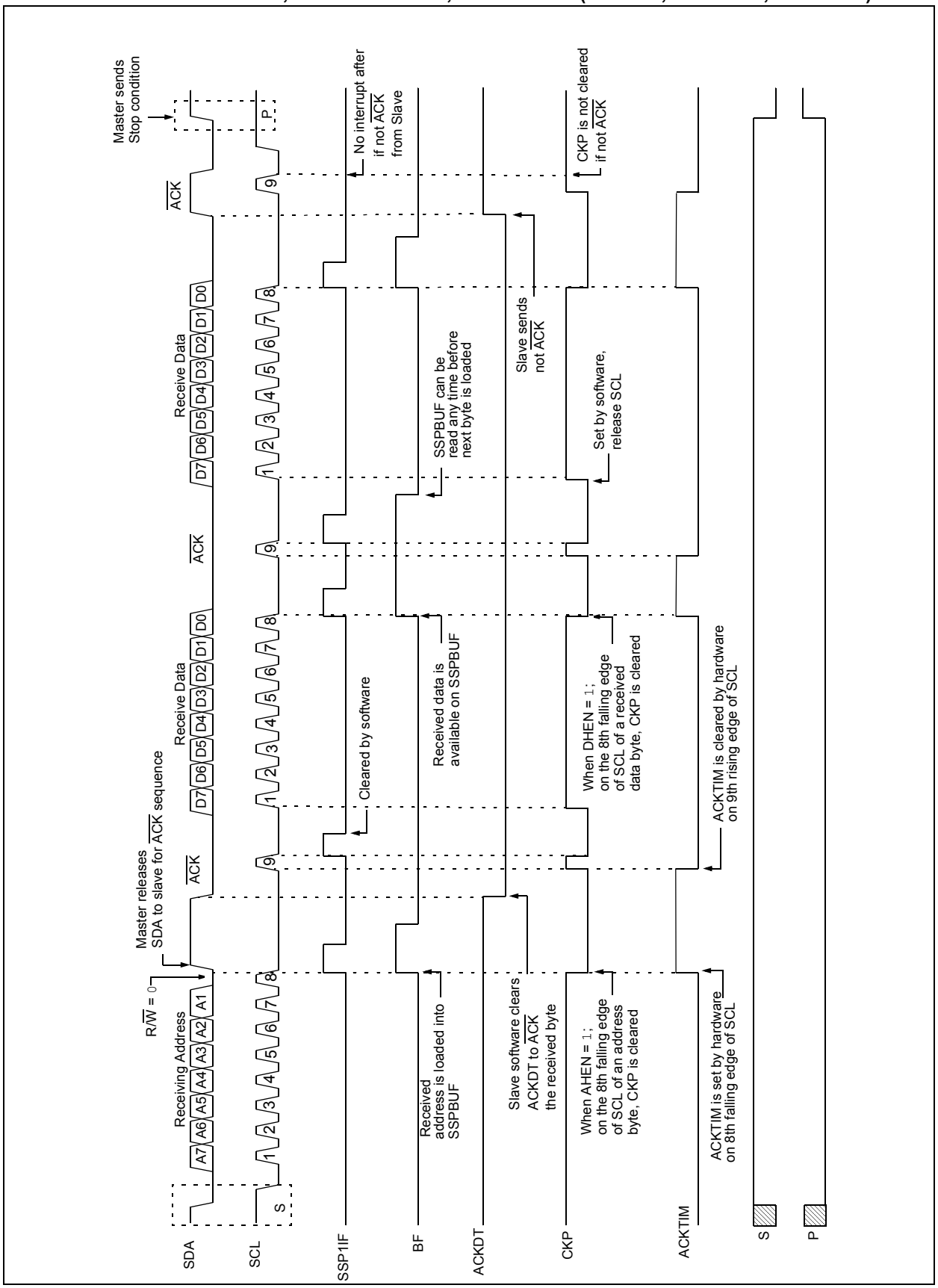


FIGURE 26-17: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 1, DHEN = 1)



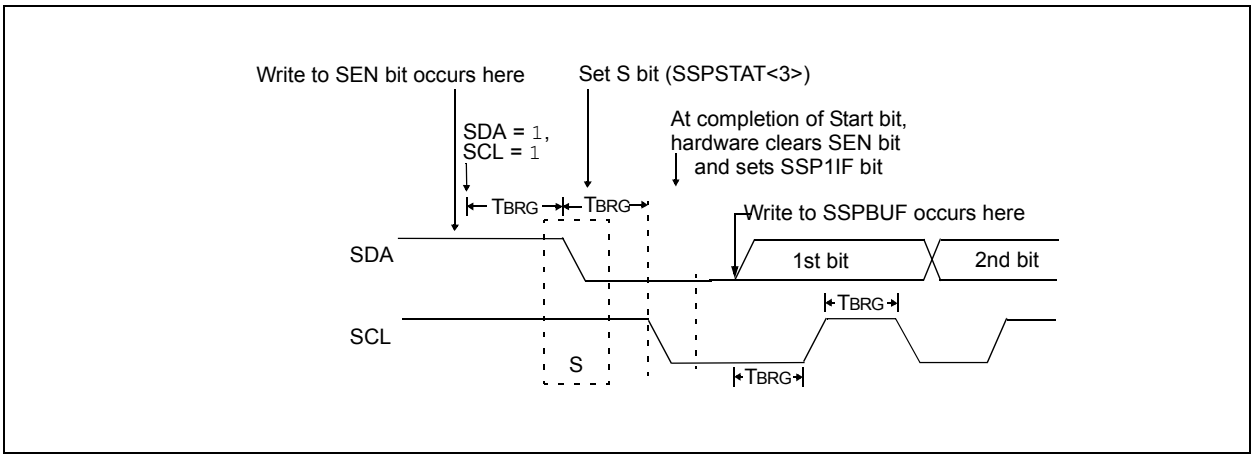
26.6.4 I²C MASTER MODE START CONDITION TIMING

To initiate a Start condition, the user sets the Start Enable bit, SEN bit of the SSPCON2 register. If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the Start condition and causes the S bit of the SSPSTAT1 register to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit of the SSPCON2 register will be automatically cleared by hardware; the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

Note 1: If at the beginning of the Start condition, the SDA and SCL pins are already sampled low, or if during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCL1IF, is set, the Start condition is aborted and the I²C module is reset into its Idle state.

2: The Philips I²C specification states that a bus collision cannot occur on a Start.

FIGURE 26-26: FIRST START BIT TIMING



27.6 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

27.6.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (see **Section 27.5.2.4 "Synchronous Slave Reception Set-up:"**).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the `SLEEP` instruction will be executed. If the Global Interrupt Enable (GIE) bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

27.6.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for synchronous slave transmission (see **Section 27.5.2.2 "Synchronous Slave Transmission Set-up:"**).
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

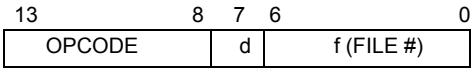
Upon waking from Sleep, the instruction following the `SLEEP` instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

27.6.3 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register, APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 13.1 "Alternate Pin Function"** for more information.

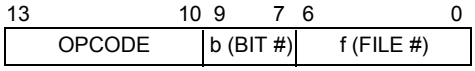
FIGURE 29-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations



d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

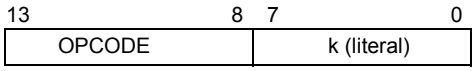
Bit-oriented file register operations



b = 3-bit bit address
f = 7-bit file register address

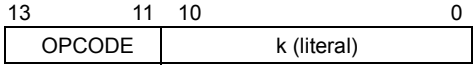
Literal and control operations

General



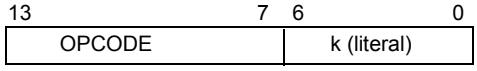
k = 8-bit immediate value

CALL and GOTO instructions only



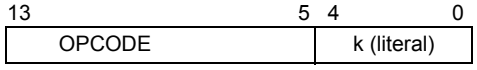
k = 11-bit immediate value

MOVLP instruction only



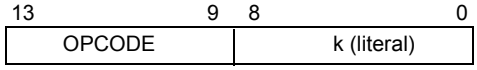
k = 7-bit immediate value

MOVLB instruction only



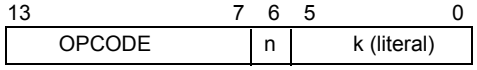
k = 5-bit immediate value

BRA instruction only



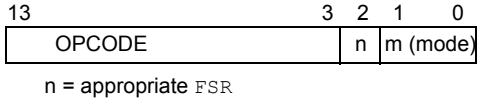
k = 9-bit immediate value

FSR Offset instructions



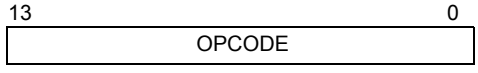
n = appropriate FSR
k = 6-bit immediate value

FSR Increment instructions



n = appropriate FSR
m = 2-bit mode value

OPCODE only



RETFIE **Return from Interrupt**

Syntax: [*label*] RETFIE

Operands: None

Operation: TOS → PC,
1 → GIE

Status Affected: None

Description: Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.

Words: 1

Cycles: 2

Example:

```
RETFIE
```

After Interrupt
PC = TOS
GIE = 1

RETLW **Return with literal in W**

Syntax: [*label*] RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W);
TOS → PC

Status Affected: None

Description: The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.

Words: 1

Cycles: 2

Example:

```
CALL TABLE;W contains table
    ;offset value
•   ;W now has table value
•
•
ADDWF PC  ;W = offset
RETLW k1  ;Begin table
RETLW k2  ;
•
•
•
RETLW kn  ; End of table
```

```
TABLE
```

Before Instruction
W = 0x07
After Instruction
W = value of k8

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC

Status Affected: None

Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

RLF **Rotate Left f through Carry**

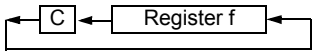
Syntax: [*label*] RLF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction
REG1 = 1110 0110
C = 0
After Instruction
REG1 = 1110 0110
W = 1100 1100
C = 1

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

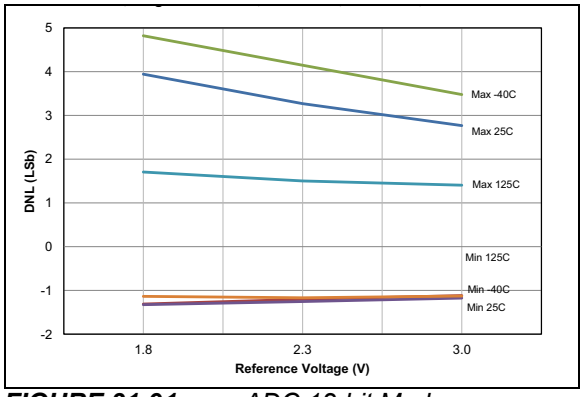


FIGURE 31-91: *ADC 12-bit Mode, Single-Ended DNL, VDD = 3.0V, TAD = 1 µS.*

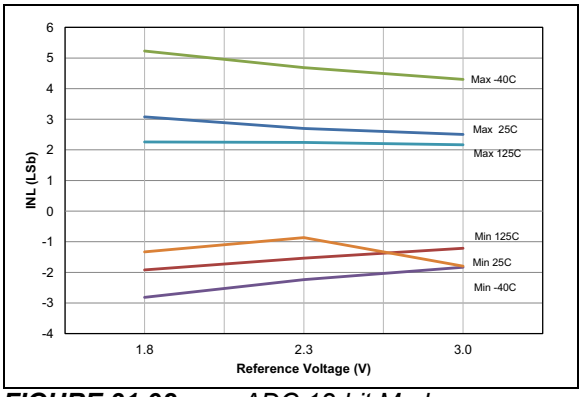


FIGURE 31-92: *ADC 12-bit Mode, Single-Ended INL, VDD = 3.0V, TAD = 1 µS.*

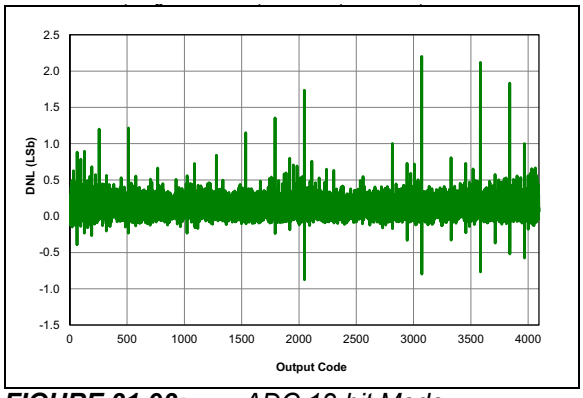


FIGURE 31-93: *ADC 12-bit Mode, Single-Ended DNL, VDD = 5.5V, TAD = 1 µS, 25°C.*

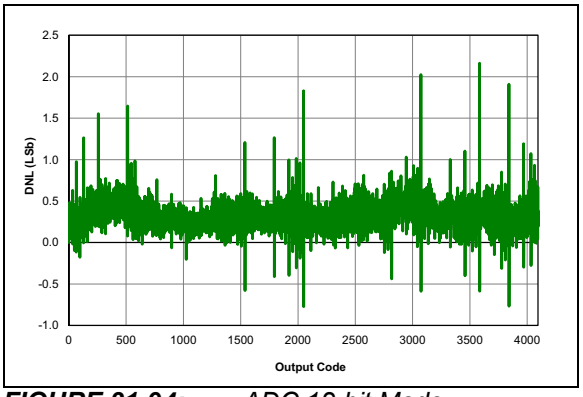


FIGURE 31-94: *ADC 12-bit Mode, Single-Ended DNL, VDD = 5.5V, TAD = 4 µS, 25°C.*

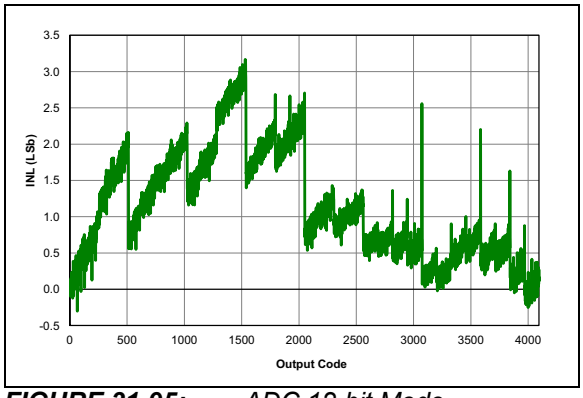


FIGURE 31-95: *ADC 12-bit Mode, Single-Ended INL, VDD = 5.5V, TAD = 1 µS, 25°C.*

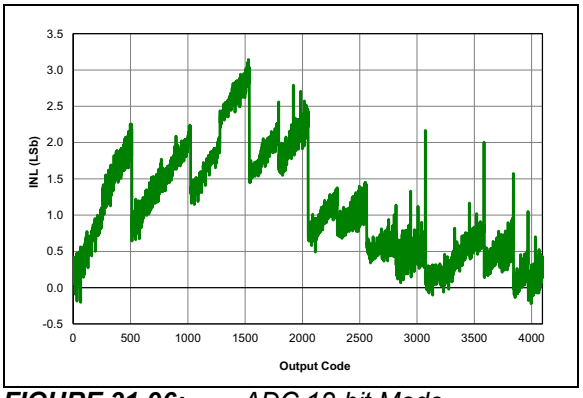


FIGURE 31-96: *ADC 12-bit Mode, Single-Ended INL, VDD = 5.5V, TAD = 4 µS, 25°C.*