What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1783-e-ml

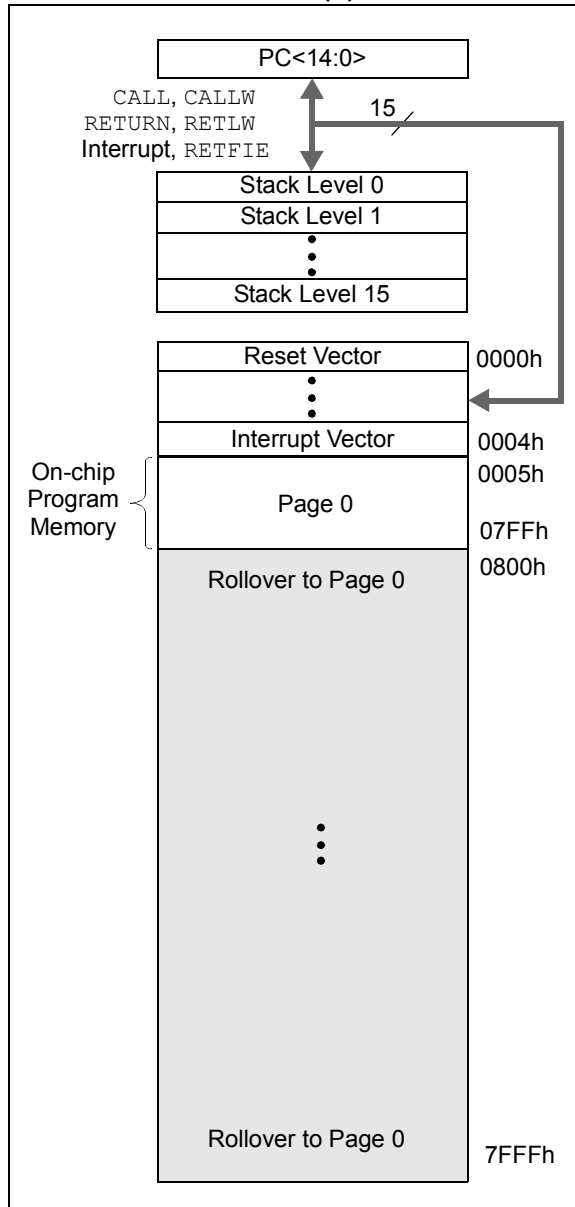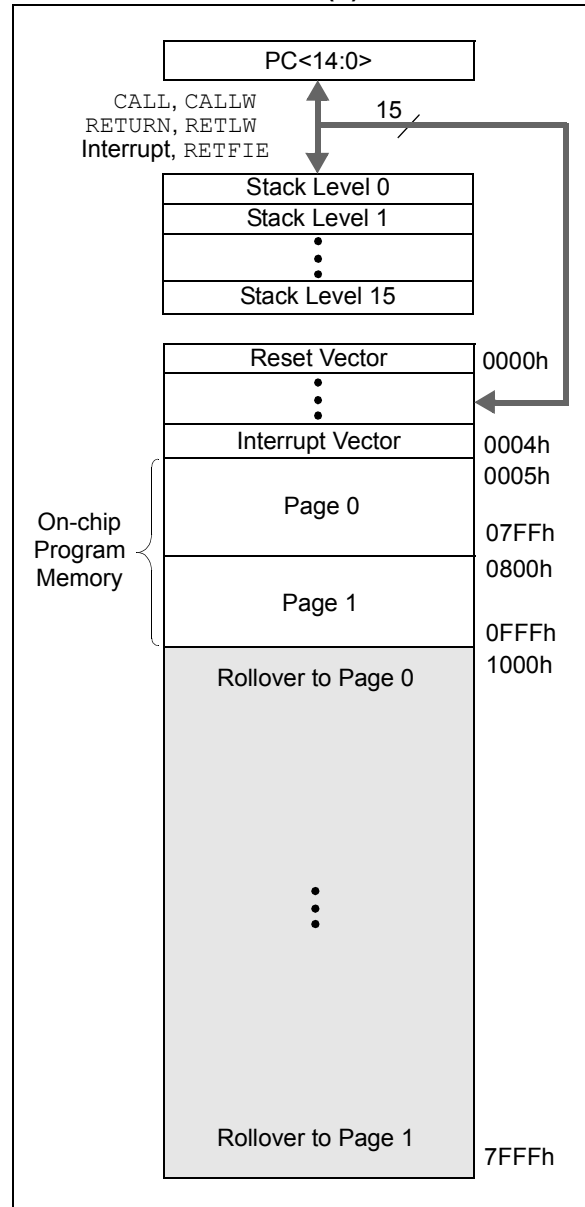**FIGURE 3-1:** **PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1782**

FIGURE 3-2: **PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1783**

4.2   Register Definitions: Configuration Words

REGISTER 4-1:   CONFIG1: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FCMEN	IESO	CLKOUTEN	BOREN<1:0>		CPD
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	MCLRE	PWRTE	WDTE<1:0>		FOSC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13   **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor and internal/external switchover are both enabled.
0 = Fail-Safe Clock Monitor is disabled

bit 12   **IESO:** Internal External Switchover bit
1 = Internal/External Switchover mode is enabled
0 = Internal/External Switchover mode is disabled

bit 11   **CLKOUTEN:** Clock Out Enable bit
If FOSC configuration bits are set to LP, XT, HS modes:
     This bit is ignored, CLKOUT function is disabled. Oscillator function on the CLKOUT pin.
All other FOSC modes:
     1 = CLKOUT function is disabled. I/O function on the CLKOUT pin.
     0 = CLKOUT function is enabled on the CLKOUT pin

bit 10-9   **BOREN<1:0>:** Brown-out Reset Enable bits
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the BORCON register
00 = BOR disabled

bit 8   **CPD:** Data Code Protection bit[1]
1 = Data memory code protection is disabled
0 = Data memory code protection is enabled

bit 7   **CP:** Code Protection bit
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6   **MCLRE:** MCLR/VPP Pin Function Select bit
If LVP bit = 1:
     This bit is ignored.
If LVP bit = 0:
     1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
     0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of
          WPUE3 bit.

bit 5   **PWRTE:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 4-3   **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled

5.0   RESETS

There are multiple ways to reset this device:

- Power-On Reset (POR)
- Brown-Out Reset (BOR)
- Low-Power Brown-Out Reset (LPBOR)
- MCLR Reset
- WDT Reset
- RESET instruction
- Stack Overflow
- Stack Underflow
- Programming mode exit

To allow VDD to stabilize, an optional Power-up Timer can be enabled to extend the Reset time after a BOR or POR event.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 5-1.

FIGURE 5-1:   **SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**

Note   1:   See Table 5-1 for BOR active conditions.
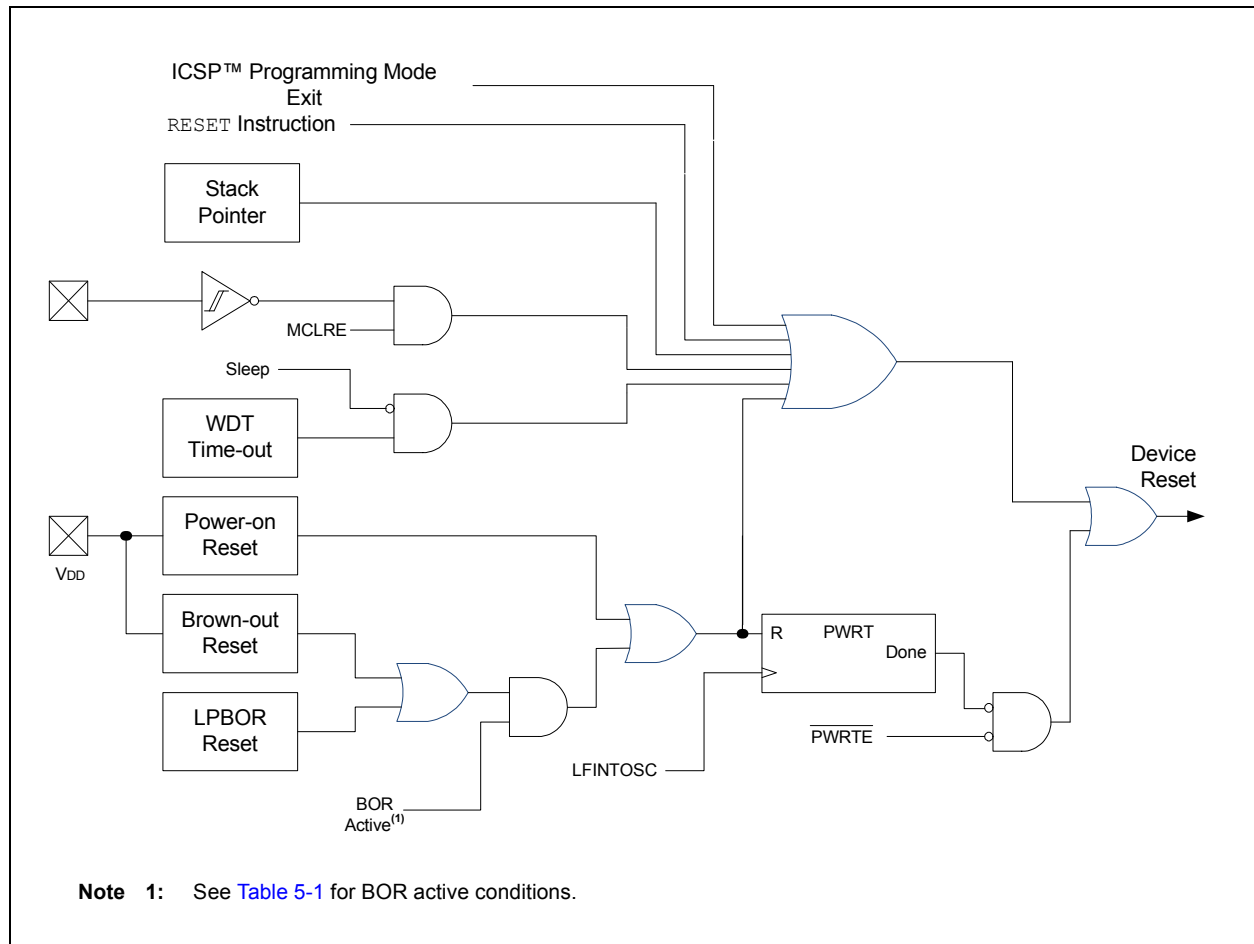
13.9 PORTE Registers

RE3 is input only, and also functions as $\overline{\text{MCLR}}$. The $\overline{\text{MCLR}}$ feature can be disabled via a configuration fuse. RE3 also supplies the programming voltage. The TRIS bit for RE3 (TRISE3) always reads '1'.

13.9.1 INPUT THRESHOLD CONTROL

The INLVLE register (Register 13-28) controls the input voltage threshold for each of the available PORTE input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTE register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See **Section TABLE 30-1: "Supply Voltage"** for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

13.9.2 PORTE FUNCTIONS AND OUTPUT PRIORITIES

No output priorities. RE3 is an input-only pin.

PIC16(L)F1782/3

24.2.9 OUTPUT WAVEFORM GENERATION

The PSMC PWM output waveform is generated based upon the different input events. However, there are several other factors that affect the PWM waveshapes:

- Output Control
  - Output Enable
  - Output Polarity
- Waveform Mode Selection
- Dead-band Control
- Steering control

24.2.10 OUTPUT CONTROL

24.2.10.1 Output Pin Enable

Each PSMC PWM output pin has individual output enable control.

When the PSMC output enable control is disabled, the module asserts no control over the pin. In this state, the pin can be used for general purpose I/O or other associate peripheral use.

When the PSMC output enable is enabled, the active PWM waveform is applied to the pin per the port priority selection.

PSMC output enable selections are made with the PSMC Output Enable Control (PSMCxOEN) register (Register 24-6).

24.2.10.2 Output Steering

PWM output will be presented only on pins for which output steering is enabled. The PSMC has up to six PWM outputs. The PWM signal in some modes can be steered to one or more of these outputs.

Steering differs from output enable in the following manner: When the output is enabled but the PWM steering to the corresponding output is not enabled, then general purpose output to the pin is disabled and the pin level will remain constantly in the inactive PWM state. Output steering is controlled with the PSMCS Steering Control 0 (PSMCxSTR0) register (Register 24-30).

Steering operates only in the following modes:

- Single-phase
- Complementary Single-phase
- 3-phase 6-step PWM

24.2.10.3 Polarity Control

Each PSMC output has individual output polarity control. Polarity is set with the PSMC Polarity Control (PSMCxPOL) register (Register 24-7).

24.3 Modes of Operation

All modes of operation use the period, rising edge, and falling edge events to generate the various PWM output waveforms.

The 3-phase 6-step PWM mode makes special use of the software controlled steering to generate the required waveform.

Modes of operation are selected with the PSMC Control (PSMCxCON) register (Register 24-1).

24.3.1 SINGLE-PHASE MODE

The single PWM is the most basic of all the waveshapes generated by the PSMC module. It consists of a single output that uses all three events (rising edge, falling edge and period events) to generate the waveform.

24.3.1.1 Mode Features

- No dead-band control available
- PWM can be steered to any combination of the following PSMC outputs:
  - PSMCxA
  - PSMCxB
  - PSMCxC
  - PSMCxD
  - PSMCxE
  - PSMCxF
- Identical PWM waveform is presented to all pins for which steering is enabled.

24.3.1.2 Waveform Generation

Rising Edge Event

- All outputs with PxSTR enabled are set to the active state

Falling Edge Event

- All outputs with PxSTR enabled are set to the inactive state

Code for setting up the PSMC generate the single-phase waveform shown in Figure 24-4, and given in Example 24-1.

24.3.11 VARIABLE FREQUENCY - FIXED DUTY CYCLE PWM WITH COMPLEMENTARY OUTPUTS

This mode is the same as the single output Fixed Duty Cycle mode except a complementary output with dead-band control is generated.

The rising edge and falling edge events are unused in this mode. Therefore, a different triggering mechanism is required for the dead-band counters.

A period events that generate a rising edge on PSMCxA use the rising edge dead-band counters.

A period events that generate a falling edge on PSMCxA use the falling edge dead-band counters.

24.3.11.1 Mode Features

- Dead-band control is available
- No steering control available
- Fractional Frequency Adjust
  - Fine period adjustments are made with the PSMC Fractional Frequency Adjust (PSMCxFFA) register (Register 24-27)
- Primary PWM is output to the following pin:
  - PSMCxA
- Complementary PWM is output to the following pin:
  - PSMCxB

#### 24.3.11.2 Waveform Generation

Period Event

When output is going inactive to active:

- Complementary output is set inactive
- FFA counter is incremented by the 4-bit value in PSMCFFA register.
- Dead-band rising is activated (if enabled)
- Primary output is set active

When output is going active to inactive:

- Primary output is set inactive
- FFA counter is incremented by the 4-bit value in PSMCFFA register
- Dead-band falling is activated (if enabled)
- Complementary output is set active

FIGURE 24-14: VARIABLE FREQUENCY – FIXED DUTY CYCLE PWM WITH COMPLEMENTARY OUTPUTS WAVEFORM

PIC16(L)F1782/3
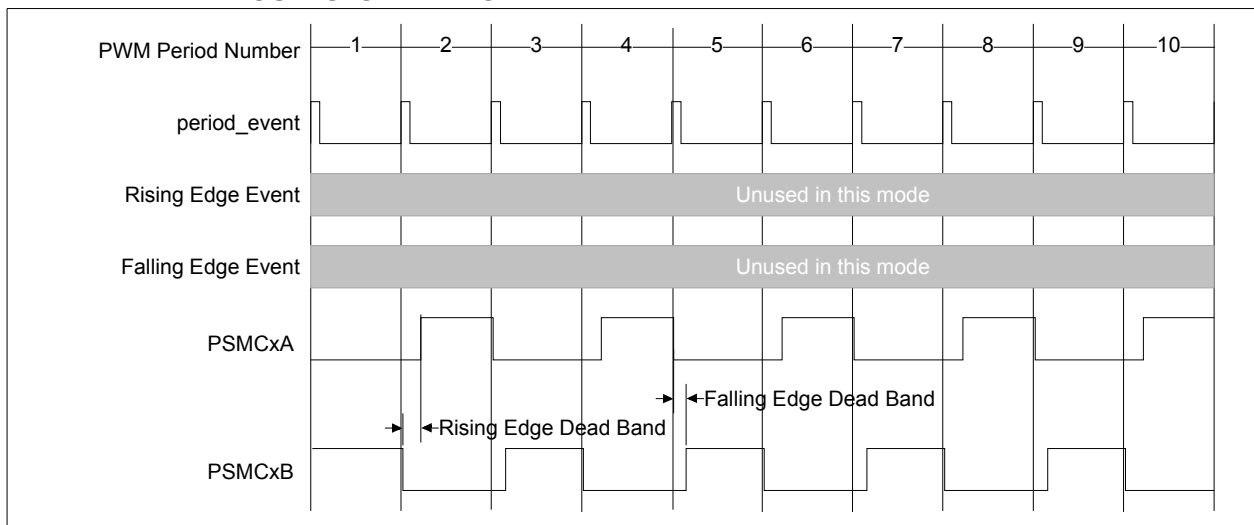
24.6 PSMC Modulation (Burst Mode)

PSMC modulation is a method to stop/start PWM operation of the PSMC without having to disable the module. It also allows other modules to control the operational period of the PSMC. This is also referred to as Burst mode.

This is a method to implement PWM dimming.

24.6.1 MODULATION ENABLE

The modulation function is enabled by setting the PxMDLEN bit of PSMC Modulation Control (PSMCxMDL) register (Register 24-2).

When modulation is enabled, the modulation source controls when the PWM signals are active and inactive.

When modulation is disabled, the PWM signals operate continuously, regardless of the selected modulation source.

24.6.2 MODULATION SOURCES

There are multiple sources that can be used for modulating the PSMC. However, unlike the PSMC input sources, only one modulation source can be selected at a time. Modulation sources include:

- PSMCxIN pin
- Any CCP output
- Any Comparator output
- PxMDLBIT of the PSMCxMDL register

24.6.2.1 PxMDLBIT Bit

The PxMDLBIT bit of the PSMC Modulation Control (PSMCxMDL) register (Register 24-2) allows for software modulation control without having to enable/disable other module functions.

24.6.3 MODULATION EFFECT ON PWM SIGNALS

When modulation starts, the PSMC begins operation on a new period, just as if it had rolled over from one period to another during continuous operation.

When modulation stops, its operation depends on the type of waveform being generated.

In operation modes other than Fixed Duty Cycle, the PSMC completes its current PWM period and then freezes the module. The PSMC output pins are forced into the default inactive state ready for use when modulation starts.

In Fixed Duty Cycle mode operation, the PSMC continues to operate until the period event changes the PWM to its inactive state, at which point the PSMC module is frozen. The PSMC output pins are forced into the default inactive state ready for use when modulation starts.
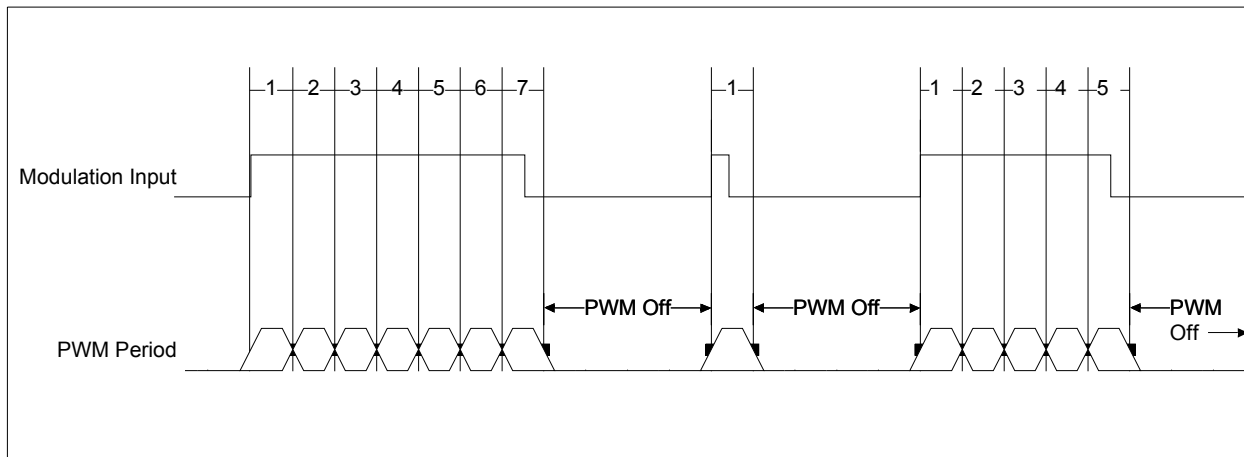
FIGURE 24-19: **PSMC MODULATION WAVEFORM**

TABLE 24-4: **SAMPLE FFA OUTPUT PERIODS/FREQUENCIES**

FFA number	Output Frequency (kHz)	Step Size (Hz)
0	125.000	0
1	124.970	-30.4
2	124.939	-60.8
3	124.909	-91.2
4	124.878	-121.6
5	124.848	-152.0
6	124.818	-182.4
7	124.787	-212.8
8	124.757	-243.2
9	124.726	-273.6
10	124.696	-304.0
11	124.666	-334.4
12	124.635	-364.8
13	124.605	-395.2
14	124.574	-425.6
15	124.544	-456.0

REGISTER 24-2: PSMCxMDL: PSMC MODULATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PxMDLEN	PxMDLPOL	PxMDLBIT	—	PxMSRC<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PxMDLEN:** PSMC Periodic Modulation Mode Enable bit

1 = PSMCx is active when input signal selected by PxMSRC<3:0> is in its active state (see PxMPOL)
0 = PSMCx module is always active

bit 6 **PxMDLPOL:** PSMC Periodic Modulation Polarity bit

1 = PSMCx is active when the PSMCx Modulation source output equals logic '0' (active-low)
0 = PSMCx is active when the PSMCx Modulation source output equals logic '1' (active-high)

bit 5 **PxMDLBIT:** PSMC Periodic Modulation Software Control bit

PxMDLEN = 1 AND PxMSRC<3:0> = 0000
1 = PSMCx is active when the PxMDLPOL equals logic '0'
0 = PSMCx is active when the PxMDLPOL equals logic '1'
PxMDLEN = 0 OR (PxMDLEN = 1 and PxMSRC<3:0> <> '0000')
Does not affect module operation

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **PxMSRC<3:0>** PSMC Periodic Modulation Source Selection bits

1111 = Reserved
1110 = Reserved
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = PSMCx Modulation Source is PSMCxIN pin
0111 = Reserved
0110 = PSMCx Modulation Source is CCP2
0101 = PSMCx Modulation Source is CCP1
0100 = Reserved
0011 = PSMCx Modulation Source is sync_C3OUT
0010 = PSMCx Modulation Source is sync_C2OUT
0001 = PSMCx Modulation Source is sync_C1OUT
0000 = PSMCx Modulation Source is PxMDLBIT register bit

25.1.5   CAPTURE DURING SLEEP

Capture mode depends upon the Timer1 module for proper operation. There are two options for driving the Timer1 module in Capture mode. It can be driven by the instruction clock ($F_{OSC}/4$), or by an external clock source.

When Timer1 is clocked by $F_{OSC}/4$, Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state.

Capture mode will operate during Sleep when Timer1 is clocked by an external clock source.

25.1.6   ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 13.1 "Alternate Pin Function"** for more information.

PIC16(L)F1782/3

FIGURE 26-3: **MSSP BLOCK DIAGRAM (I²C™ SLAVE MODE)**
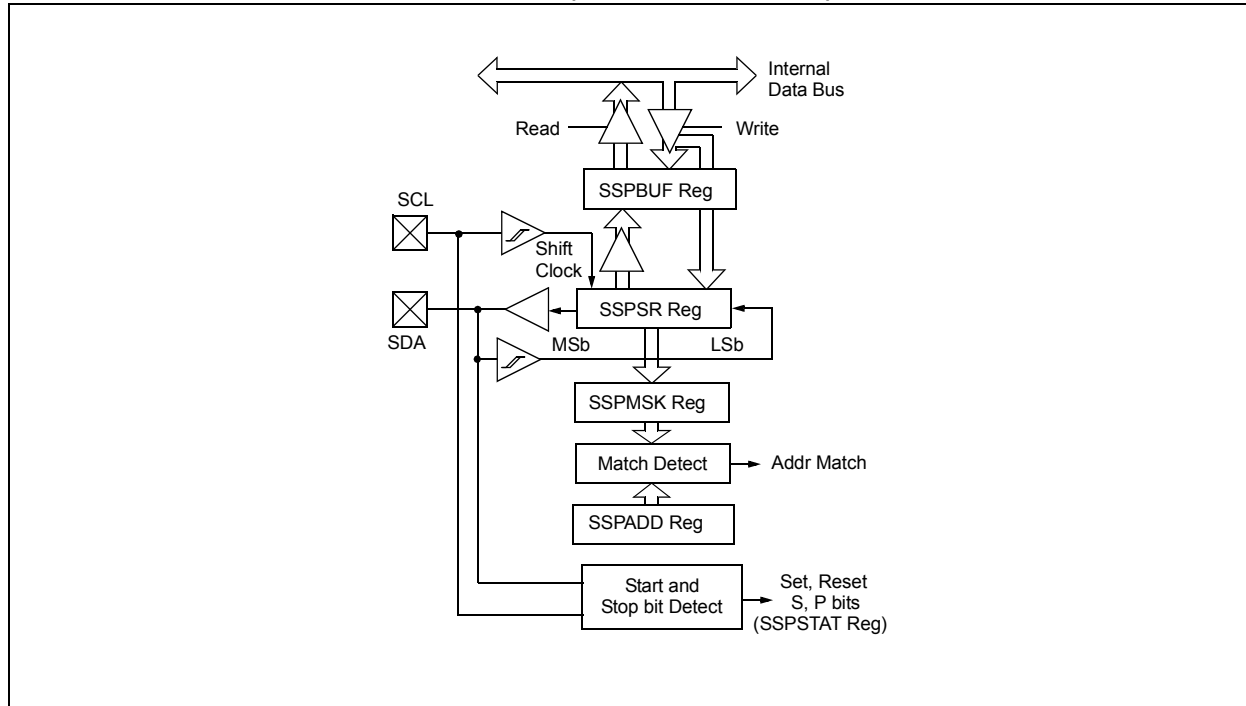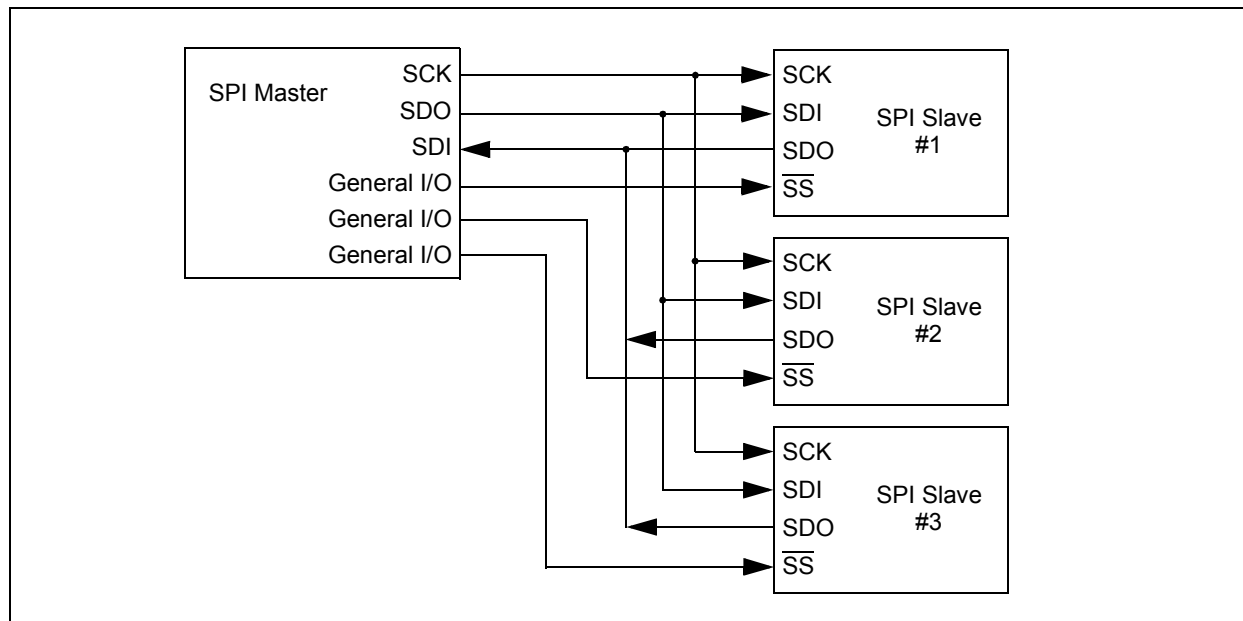
FIGURE 26-4: SPI MASTER AND MULTIPLE SLAVE CONNECTION

26.2.1 SPI MODE REGISTERS

The MSSP module has five registers for SPI mode operation. These are:

- MSSP STATUS register (SSPSTAT)
- MSSP Control register 1 (SSPCON1)
- MSSP Control register 3 (SSPCON3)
- MSSP Data Buffer register (SSPBUF)
- MSSP Address register (SSPADD)
- MSSP Shift register (SSPSR)
  (Not directly accessible)

SSPCON1 and SSPSTAT are the control and STATUS registers in SPI mode operation. The SSPCON1 register is readable and writable. The lower 6 bits of the SSPSTAT are read-only. The upper 2 bits of the SSPSTAT are read/write.

In one SPI master mode, SSPADD can be loaded with a value used in the Baud Rate Generator. More information on the Baud Rate Generator is available in **Section 26.7 "Baud Rate Generator"**.

SSPSR is the shift register used for shifting data in and out. SSPBUF provides indirect access to the SSPSR register. SSPBUF is the buffer register to which data bytes are written, and from which data bytes are read.

In receive operations, SSPSR and SSPBUF together create a buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSP1IF interrupt is set.

During transmission, the SSPBUF is not buffered. A write to SSPBUF will write to both SSPBUF and SSPSR.

26.3 I²C MODE OVERVIEW

The Inter-Integrated Circuit Bus (I²C) is a multi-master serial data communication bus. Devices communicate in a master/slave environment where the master devices initiate the communication. A Slave device is controlled through addressing.

The I²C bus specifies two signal connections:

• Serial Clock (SCL)
• Serial Data (SDA)

Figure 26-11 shows the block diagram of the MSSP module when operating in I²C mode.

Both the SCL and SDA connections are bidirectional open-drain lines, each requiring pull-up resistors for the supply voltage. Pulling the line to ground is considered a logical zero and letting the line float is considered a logical one.

Figure 26-11 shows a typical connection between two processors configured as master and slave devices.

The I²C bus can operate with one or more master devices and one or more slave devices.

There are four potential modes of operation for a given device:

• Master Transmit mode
  (master is transmitting data to a slave)
• Master Receive mode
  (master is receiving data from a slave)
• Slave Transmit mode
  (slave is transmitting data to a master)
• Slave Receive mode
  (slave is receiving data from the master)

To begin communication, a master device starts out in Master Transmit mode. The master device sends out a Start bit followed by the address byte of the slave it intends to communicate with. This is followed by a single Read/Write bit, which determines whether the master intends to transmit to or receive data from the slave device.

If the requested slave exists on the bus, it will respond with an Acknowledge bit, otherwise known as an $\overline{ACK}$. The master then continues in either Transmit mode or Receive mode and the slave continues in the complement, either in Receive mode or Transmit mode, respectively.

A Start bit is indicated by a high-to-low transition of the SDA line while the SCL line is held high. Address and data bytes are sent out, Most Significant bit (MSb) first. The Read/Write bit is sent out as a logical one when the master intends to read data from the slave, and is sent out as a logical zero when it intends to write data to the slave.

FIGURE 26-11: I²C MASTER/ SLAVE CONNECTION
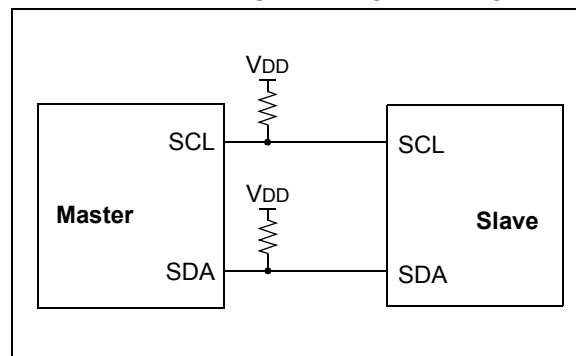
The Acknowledge bit ($\overline{ACK}$) is an active-low signal, which holds the SDA line low to indicate to the transmitter that the slave device has received the transmitted data and is ready to receive more.

The transition of a data bit is always performed while the SCL line is held low. Transitions that occur while the SCL line is held high are used to indicate Start and Stop bits.

If the master intends to write to the slave, then it repeatedly sends out a byte of data, with the slave responding after each byte with an $\overline{ACK}$ bit. In this example, the master device is in Master Transmit mode and the slave is in Slave Receive mode.

If the master intends to read from the slave, then it repeatedly receives a byte of data from the slave, and responds after each byte with an $\overline{ACK}$ bit. In this example, the master device is in Master Receive mode and the slave is Slave Transmit mode.

On the last byte of data communicated, the master device may end the transmission by sending a Stop bit. If the master device is in Receive mode, it sends the Stop bit in place of the last $\overline{ACK}$ bit. A Stop bit is indicated by a low-to-high transition of the SDA line while the SCL line is held high.

In some cases, the master may want to maintain control of the bus and re-initiate another transmission. If so, the master device may send another Start bit in place of the Stop bit or last $\overline{ACK}$ bit when it is in receive mode.

The I²C bus specifies three message protocols;

• Single message where a master writes data to a slave.
• Single message where a master reads data from a slave.
• Combined message where a master initiates a minimum of two writes, or two reads, or a combination of writes and reads, to one or more slaves.

FIGURE 26-22: I²C SLAVE, 10-BIT ADDRESS, TRANSMISSION (SEN = 0, AHEN = 0, DHEN = 0)

PIC16(L)F1782/3
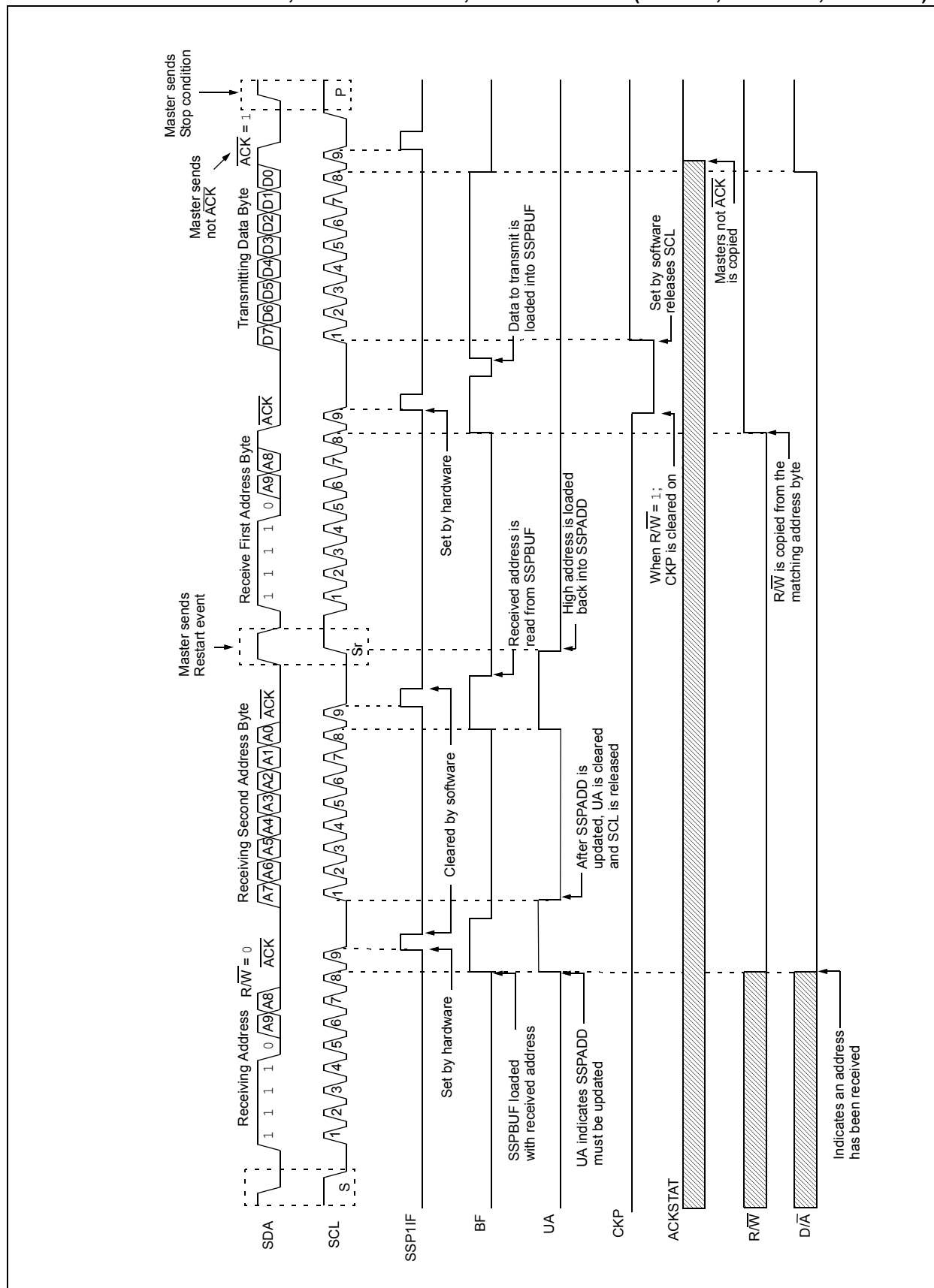
27.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 27-1 and Figure 27-2.

FIGURE 27-1: **EUSART TRANSMIT BLOCK DIAGRAM**

PIC16(L)F1782/3
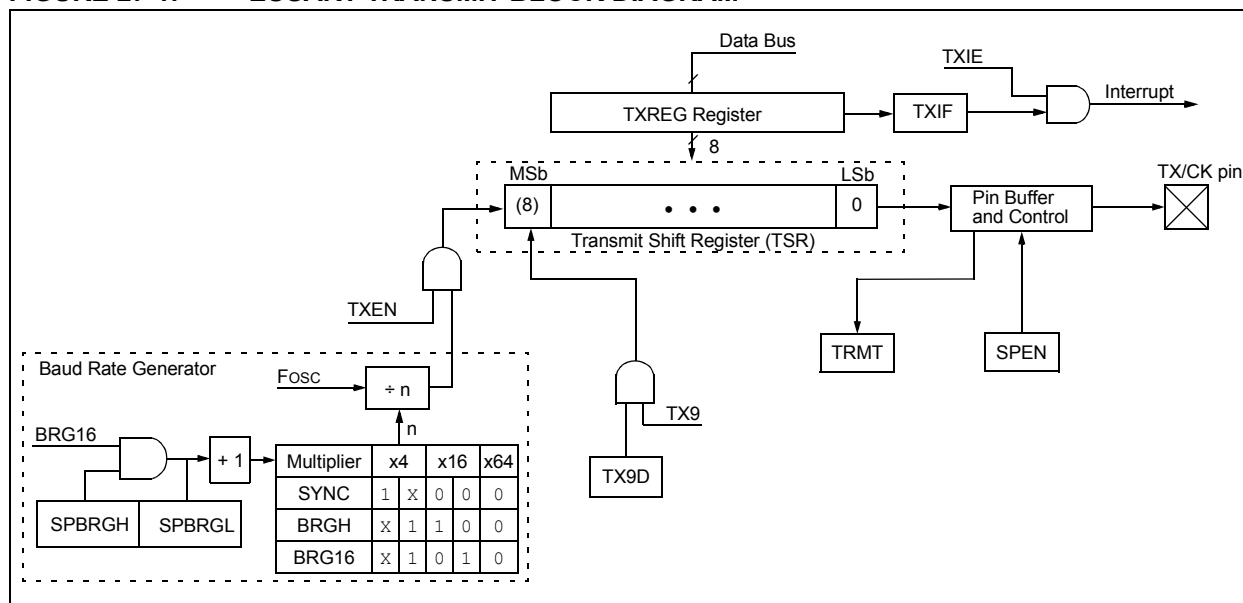
27.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a V_{OH} mark state which represents a '1' data bit, and a V_{OL} space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is 8 bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 27-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

27.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 27-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

27.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

> **Note:** The TXIF Transmitter Interrupt flag is set when the TXEN enable bit is set.

27.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one T_{CY} immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

27.1.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the SCKP bit of the BAUDxCON register. The default state of this bit is '0' which selects high true transmit idle and data bits. Setting the SCKP bit to '1' will invert the transmit data resulting in low true idle and data bits. The SCKP bit controls transmit data polarity in Asynchronous mode only. In Synchronous mode, the SCKP bit has a different function. See **Section 27.5.1.2 "Clock Polarity"**.

27.1.1.4 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXREG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXREG.
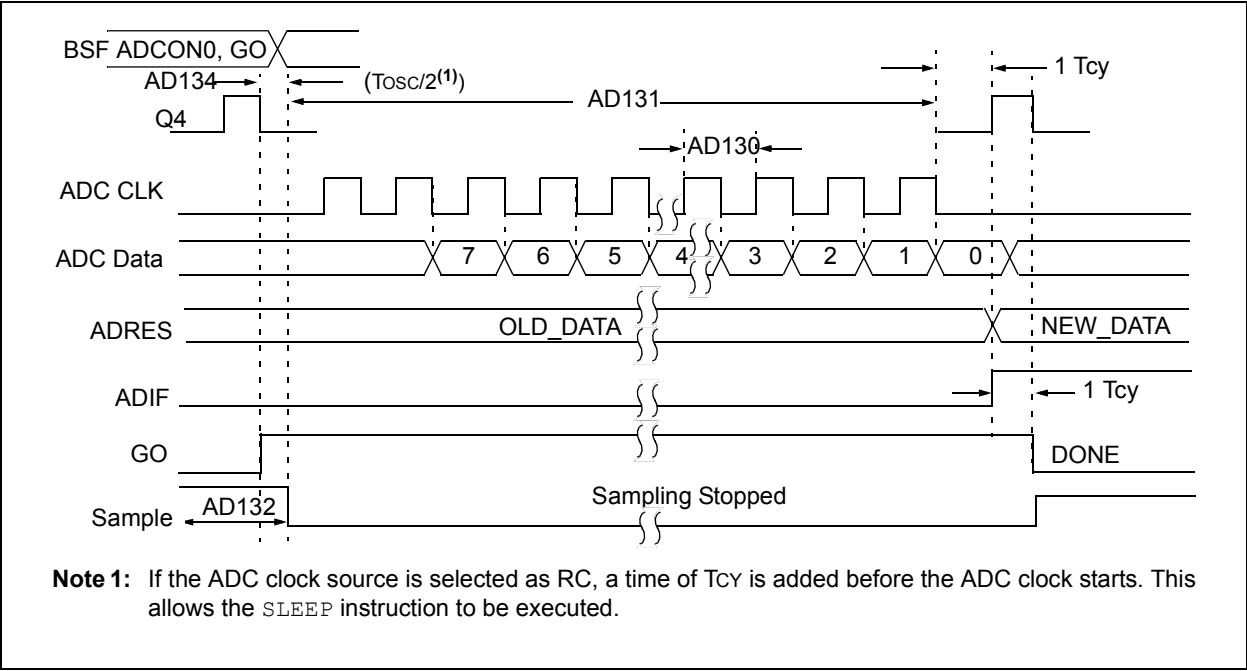
FIGURE 30-12: **ADC CONVERSION TIMING (NORMAL MODE)**

Note 1: If the ADC clock source is selected as RC, a time of T_{CY} is added before the ADC clock starts. This allows the SLEEP instruction to be executed.

FIGURE 30-13: **ADC CONVERSION TIMING (SLEEP MODE)**

Note 1: If the ADC clock source is selected as RC, a time of T_{CY} is added before the ADC clock starts. This allows the SLEEP instruction to be executed.
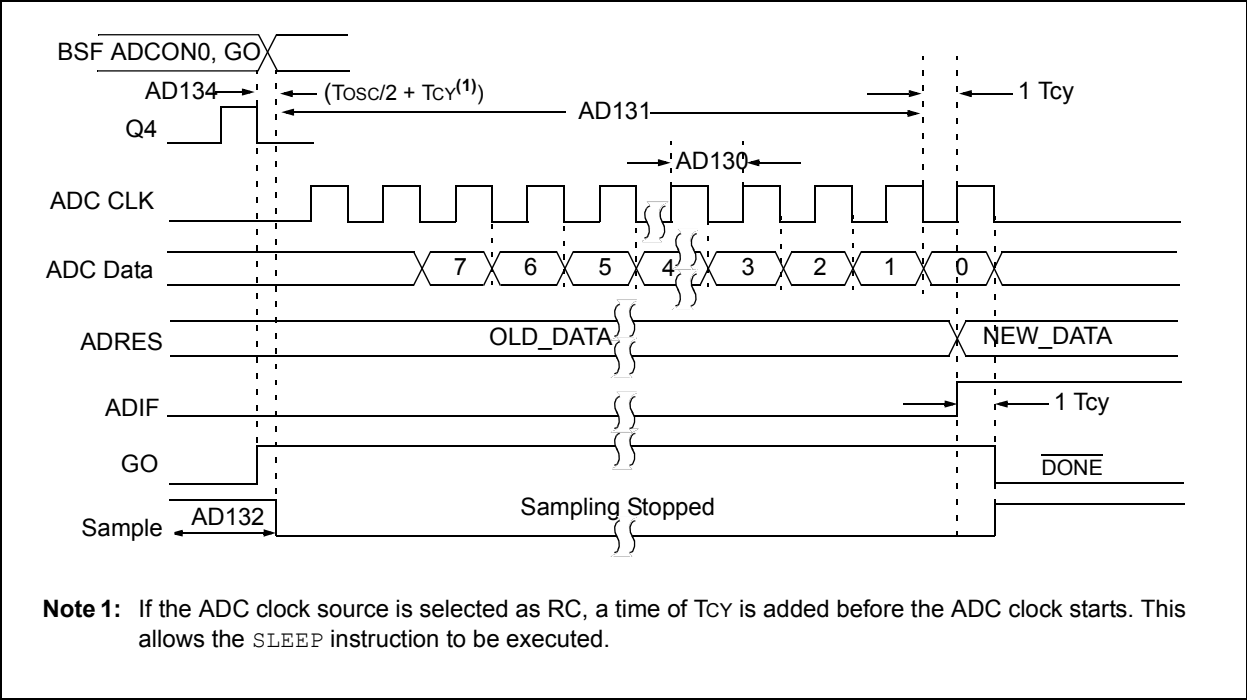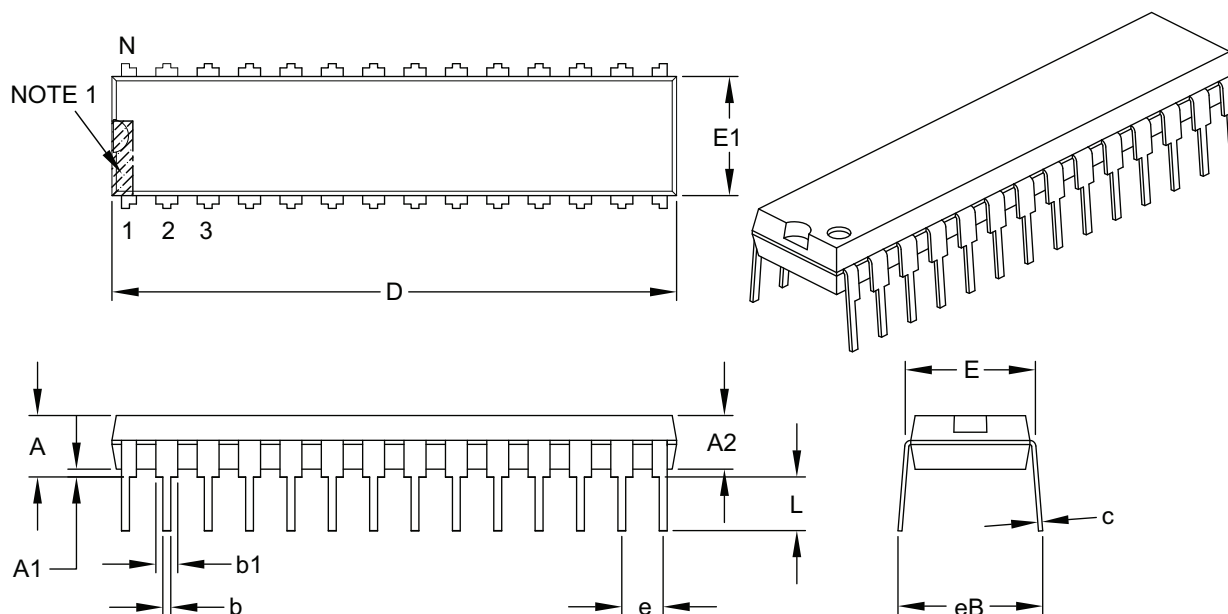
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33.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Units		INCHES	
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN]
with 0.55 mm Contact Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

BOTTOM VIEW
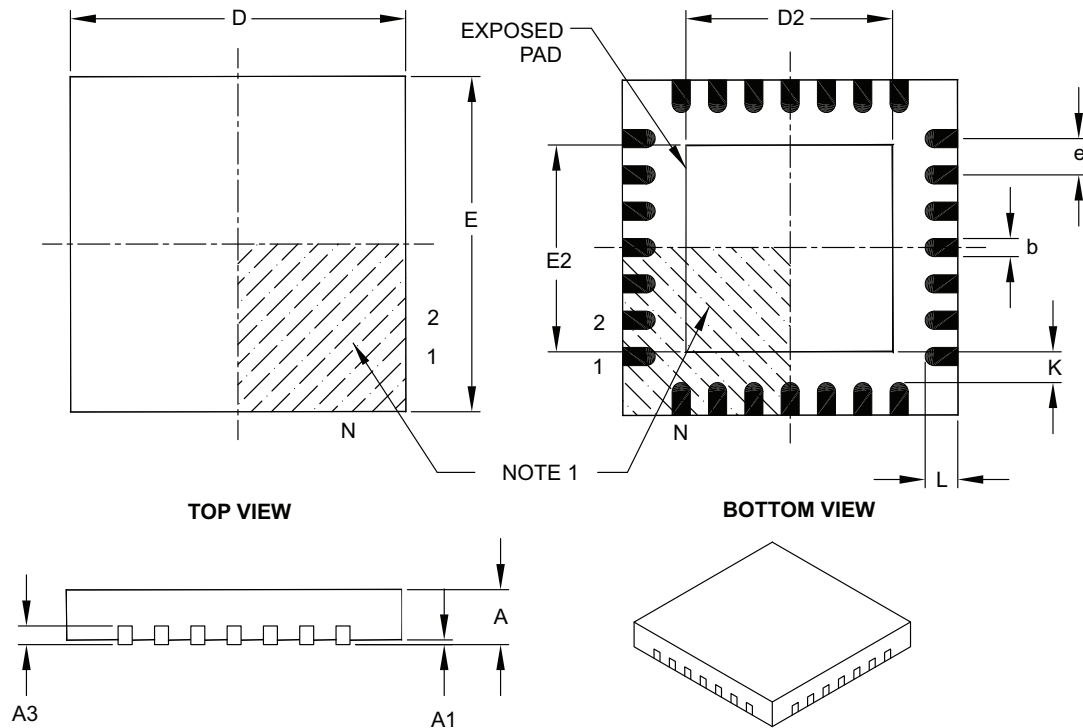
	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (04/2011)

Original release.

Revision B (06/2011)

Revised Section 18.0; Revised Table 30-8; Add Operational Amplifier Table.

Revision C (03/2012)

Electrical Specifications update.

Revision D (11/2012)

Revised: Table 5-4, Section 6.2.1.3, 9.0, Table 15-1 (LDO), Figure 16-1, Section 17.1.6, 17.2.3, 20.7, 24.1, 24.1.1-24.1.3, 24.2.7, 24.2.8, 24.3.4.1, 24.3.11, 24.8.1.1-24.8.1.3; Register 24.2 (PxMSRC description); Registers 24-9-24-13, 24-16, 25-1 (Bits 0-3 descriptions); Add Table 16-2, Section 24.2.7.3.

Electrical Specifications update: Revised 30.2 (D010, D012), 30.3 (D023, D025, D026, D029-D031); Table 30-4 (delete Note 2); Table 30-1 (Param. OPA08, OPA09), Table 30-11, Table 30-12 (Param. DAC02).

Revision E (3/2014)

Change from Preliminary to Final data sheet.

Corrected the following Tables: Family Types Table on page 3, Table 3-3, Table 3-8, Table 20-3, Table 22-2, Table 22-3, Table 23-1, Table 25-3, Table 30-1, Table 30-2, Table 30-3, Table 30-6, Table 30-7, Table 30-13, Table 30-14, Table 30-15, Table 30-16, Table 30-20.

Corrected the following Sections: Section 3.2, Section 9.2, Section 13.3, Section 17.1.6, Section 15.1, Section 15.3, Section 17.2.5, Section 18.2, Section 18.3, Section 19.0, Section 22.6.5, Section 22.9, Section 23.0, Section 23.1, Section 24.2.4, Section 24.2.5, Section 24.2.7, Section 24.8, Section 25.0, Section 26.6.7.4, Section 30.3.

Corrected the following Registers: Register 4-2, Register 8-2, Register 8-5, Register 17-3, Register 18-1, Register 24-3, Register 24-4.

Corrected Equation 17-1.

Corrected Figure 30-9. Removed Figure 24-21.