



#### Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1783-e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 4.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data EEPROM protection are controlled independently. Internal access to the program memory and data EEPROM are unaffected by any code protection setting.

#### 4.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the  $\overline{CP}$  bit in Configuration Words. When  $\overline{CP} = 0$ , external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See Section 4.4 "Write Protection" for more information.

## 4.3.2 DATA EEPROM PROTECTION

The entire data EEPROM is protected from external reads and writes by the CPD bit. When CPD = 0, external reads and writes of data EEPROM are inhibited. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

## 4.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as bootloader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Words define the size of the program memory block that is protected.

## 4.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 12.5 "User ID, Device ID and Configuration Word Access**" for more information on accessing these memory locations. For more information on checksum calculation, see the *"PIC16(L)F178X Memory Programming Specification"* (DS41457).

# PIC16(L)F1782/3

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	BORFS			_	_	_	BORRDY	47
PCON	STKOVF	STKUNF	_	RWDT	RMCLR	RI	POR	BOR	51
STATUS	—	_	_	TO	PD	Z	DC	С	18
WDTCON	—		WDTPS<4:0>					SWDTEN	94

## TABLE 5-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

#### 6.2.2.7 Internal Oscillator Clock Switch Timing

When switching between the HFINTOSC, MFINTOSC and the LFINTOSC, the new oscillator may already be shut down to save power (see Figure 6-7). If this is the case, there is a delay after the IRCF<3:0> bits of the OSCCON register are modified before the frequency selection takes place. The OSCSTAT register will reflect the current active status of the HFINTOSC, MFINTOSC and LFINTOSC oscillators. The sequence of a frequency selection is as follows:

- 1. IRCF<3:0> bits of the OSCCON register are modified.
- 2. If the new clock is shut down, a clock start-up delay is started.
- 3. Clock switch circuitry waits for a falling edge of the current clock.
- 4. The current clock is held low and the clock switch circuitry waits for a rising edge in the new clock.
- 5. The new clock is now active.
- 6. The OSCSTAT register is updated as required.
- 7. Clock switch is complete.

See Figure 6-7 for more details.

If the internal oscillator speed is switched between two clocks of the same source, there is no start-up delay before the new frequency is selected. Clock switching time delays are shown in Table 6-1.

Start-up delay specifications are located in the oscillator tables of **Section 30.0** "**Electrical Specifications**".

## 8.6 Register Definitions: Interrupt Control

R/W-0/	0 R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0
GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF <sup>(1)</sup>
bit 7				1			bit 0
Legend:							
R = Reada	able bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
u = Bit is u	unchanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets
'1' = Bit is	set	'0' = Bit is clea	ared				
bit 7	<b>GIE:</b> Global Ir 1 = Enables a 0 = Disables a	nterrupt Enable Ill active interru all interrupts	e bit ipts				
bit 6	PEIE: Periphe 1 = Enables a 0 = Disables a	eral Interrupt E all active periph all peripheral ir	nable bit eral interrupts iterrupts	6			
bit 5	<b>TMR0IE:</b> Time 1 = Enables the 0 = Disables the	er0 Overflow Ir he Timer0 inter the Timer0 inte	nterrupt Enabl rrupt rrupt	e bit			
bit 4	INTE: INT Ex 1 = Enables t 0 = Disables t	ternal Interrupt he INT externa the INT externa	Enable bit I interrupt al interrupt				
bit 3	IOCIE: Interru 1 = Enables t 0 = Disables t	upt-on-Change he interrupt-on the interrupt-or	Enable bit -change -change				
bit 2	<b>TMR0IF:</b> Time 1 = TMR0 reg 0 = TMR0 reg	er0 Overflow Ir jister has overf jister did not ov	iterrupt Flag b lowed /erflow	pit			
bit 1	<pre>it 1 INTF: INT External Interrupt Flag bit 1 = The INT external interrupt occurred 0 = The INT external interrupt did not occur</pre>						
bit 0 IOCIF: Interrupt-on-Change Interrupt Flag bit <sup>(1)</sup> 1 = When at least one of the interrupt-on-change pins changed state 0 = None of the interrupt-on-change pins have changed state							
Note 1:	The IOCIF Flag bit have been cleared	is read-only a by software.	nd cleared wh	en all the Inter	rupt-on-change	flags in the IO	CBF register

#### REGISTER 8-1: INTCON: INTERRUPT CONTROL REGISTER

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	
		PSMC2TIE	PSMC1TIE	_		PSMC2SIE	PSMC1SIE	
bit 7						•	bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	as '0'		
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value	at POR and BOI	R/Value at all o	ther Resets	
'1' = Bit is set		'0' = Bit is clea	ared					
bit 7-6	Unimplemen	ted: Read as '	0'					
bit 5	PSMC2TIE: F	PSMC2 Time B	ase Interrupt I	Enable bit				
	1 = Enables	PSMC2 time ba	ase generated	l interrupts				
	0 = Disables	PSMC2 time b	ase generated	d interrupts				
bit 4	PSMC1TIE: F	PSMC1 Time B	ase Interrupt I	Enable bit				
	1 = Enables	PSMC1 time b	ase generated	l interrupts				
<b>h</b> # 0 0			ase generated $a$ ,	a interrupts				
DIT 3-2	Unimplemen	ted: Read as	0					
bit 1	PSMC2SIE: F	PSMC2 Auto-S	hutdown Inter	rupt Enable bit	t			
	1 = Enables	PSMC2 auto-s	hutdown interr	rupts				
	0 = Disables	PSMC2 auto-s	shutdown inter	rupts				
bit 0	bit 0 PSMC1SIE: PSMC1 Auto-Shutdown Interrupt Enable bit							
	1 = Enables	PSMC1 auto-s	hutdown interr	rupts				
	0 = Disables	PSMC1 auto-s	shutdown inter	rupts				

## REGISTER 8-4: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	
bit 7		I	I			I	bit 0	
Legend:								
R = Readable bit		W = Writable	bit	U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is		x = Bit is unkr	x = Bit is unknown		at POR and BO	R/Value at all o	ther Resets	
'1' = Bit is set		'0' = Bit is clea	ared					
bit 7	TMR1GIF: In	ner1 Gate Inte	rrupt Flag bit					
	1 = Interrupt is 0 = Interrupt is	s penaing s not pendina						
bit 6	ADIF: ADC C	onverter Interri	upt Flag bit					
	1 = Interrupt is	s pending						
	0 = Interrupt is	s not pending						
bit 5	RCIF: USART	Receive Inter	rupt Flag bit					
	1 = Interrupt is	s pending						
hit 4		s not pending Transmit Inter	runt Elog hit					
DIL 4	1 = Interrunt in		Tupt Flag bit					
	0 = Interrupt is	s not pending						
bit 3	SSP1IF: Sync	hronous Seria	I Port (MSSP)	Interrupt Flag	bit			
	1 = Interrupt is	s pending						
	0 = Interrupt is	s not pending						
bit 2	CCP1IF: CCF	1 Interrupt Fla	g bit					
	1 = Interrupt is	s pending						
bit 1	TMR2IF: Time	er2 to PR2 Inte	rrupt Flag bit					
	1 = Interrupt is	s pendina	in up thing bit					
	0 = Interrupt is	s not pending						
bit 0	TMR1IF: Time	er1 Overflow In	iterrupt Flag bi	t				
	1 = Interrupt is	s pending						
	0 = Interrupt is	s not pending						
Note: Int	terrupt flag bits a	re set when an	interrupt					
CO	ndition occurs, re	egardless of the	e state of					
lts Fr	corresponding e	f the INTCON	register					
Us	ser software	should ensu	ure the					
ар	propriate interru	upt flag bits a	are clear					
pri	ior to enabling ar	n interrupt.						

## REGISTER 8-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

## 21.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (independent of Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- · Interrupt on overflow
- TMR0 can be used to gate Timer1

Figure 21-1 is a block diagram of the Timer0 module.

## 21.1 Timer0 Operation

The Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

#### 21.1.1 8-BIT TIMER MODE

The Timer0 module will increment every instruction cycle, if used without a prescaler. 8-bit Timer mode is selected by clearing the TMR0CS bit of the OPTION\_REG register.

When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

**Note:** The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

## FIGURE 21-1: BLOCK DIAGRAM OF THE TIMER0

#### 21.1.2 8-BIT COUNTER MODE

In 8-Bit Counter mode, the Timer0 module will increment on every rising or falling edge of the T0CKI pin.

8-Bit Counter mode using the T0CKI pin is selected by setting the TMR0CS bit in the OPTION\_REG register to '1'.

The rising or falling transition of the incrementing edge for either input source is determined by the TMR0SE bit in the OPTION\_REG register.



## 23.1 Timer2 Operation

The clock input to the Timer2 modules is the system instruction clock (Fosc/4).

A 4-bit counter/prescaler on the clock input allows direct input, divide-by-4 and divide-by-16 prescale options. These options are selected by the prescaler control bits, T2CKPS<1:0> of the T2CON register. The value of TMR2 is compared to that of the Period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see Section 23.2 "Timer2 Interrupt").

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, whereas the PR2 register initializes to FFh. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- a write to the T2CON register
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- MCLR Reset
- Watchdog Timer (WDT) Reset
- · Stack Overflow Reset
- Stack Underflow Reset
- RESET Instruction

Note: TMR2 is not cleared when T2CON is written.

## 23.2 Timer2 Interrupt

Timer2 can also generate an optional device interrupt. The Timer2 output signal (TMR2-to-PR2 match) provides the input for the 4-bit counter/postscaler. This counter generates the TMR2 match interrupt flag which is latched in TMR2IF of the PIR1 register. The interrupt is enabled by setting the TMR2 Match Interrupt Enable bit, TMR2IE, of the PIE1 register.

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, T2OUTPS<3:0>, of the T2CON register.

## 23.3 Timer2 Output

The unscaled output of TMR2 is available primarily to the CCP modules, where it is used as a time base for operations in PWM mode.

Timer2 can be optionally used as the shift clock source for the MSSP module operating in SPI mode. Additional information is provided in Section 26.0 "Master Synchronous Serial Port (MSSP) Module"

## 23.4 Timer2 Operation During Sleep

The Timer2 timers cannot be operated while the processor is in Sleep mode. The contents of the TMR2 and PR2 registers will remain unchanged while the processor is in Sleep mode.

#### 24.2.7 ASYNCHRONOUS INPUTS

The PSMC module supports asynchronous inputs alone or in combination with the synchronous inputs. asynchronous inputs include:

- Analog
  - sync\_C1OUT
- sync\_C2OUT
- sync\_C3OUT
- Digital
  - PSMCxIN pin

#### 24.2.7.1 Comparator Inputs

The outputs of any combination of the synchronized comparators may be used to trigger any of the three events as well as auto-shutdown.

The event triggers on the rising edge of the comparator output. Except for auto-shutdown, the event input is not level sensitive.

#### 24.2.7.2 PSMCxIN Pin Input

The PSMCxIN pin may be used to trigger PSMC events. Data is passed through straight to the PSMC module without any synchronization to a system clock. This is so that input blanking may be applied to any external circuit using the module.

The event triggers on the rising edge of the PSMCxIN signal.

#### 24.2.8 INPUT BLANKING

Input blanking is a function whereby the inputs from any selected asynchronous input may be driven inactive for a short period of time. This is to prevent electrical transients from the turn-on/off of power components from generating a false event.

Blanking is initiated by either or both:

- Rising event
- Falling event

Blanked inputs are suppressed from causing all asynchronous events, including:

- Rising
- Falling
- Period
- Shutdown

Rising edge and falling edge blanking are controlled independently. The following features are available for blanking:

- · Blanking enable
- Blanking time counters
- · Blanking mode

The following Blanking modes are available:

- Blanking disabled
- · Immediate blanking

The Falling Edge Blanking mode is set with the PxFEBM<1:0> bits of the PSMCx Blanking Control (PSMCxBLNK) register (Register 24-8).

The Rising Edge Blanking mode is set with the PxREBM<1:0> bits of the PSMCx Blanking Control (PSMCxBLNK) register (Register 24-8).

#### 24.2.8.1 Blanking Disabled

With blanking disabled, the asynchronous inputs are passed to the PSMC module without any intervention.

#### 24.2.8.2 Immediate Blanking

With Immediate blanking, a counter is used to determine the blanking period. The desired blanking time is measured in psmc\_clk periods. A rising edge event will start incrementing the rising edge blanking counter. A falling edge event will start incrementing the falling edge blanking counter.

The rising edge blanking time is set with the PSMC Rising Edge Blanking Time (PSMCxBLKR) register (Register 24-28). The inputs to be blanked are selected with the PSMC Rising Edge Blanked Source (PSMCxREBS) register (Register 24-9). During rising edge blanking, the selected blanked sources are suppressed for falling edge as well as rising edge, auto-shutdown and period events.

The falling edge blanking time is set with the PSMC Falling Edge Blanking Time (PSMCxBLKF) register (Register 24-29). The inputs to be blanked are selected with the PSMC Falling Edge Blanked Source (PSMCxFEBS) register (Register 24-10). During falling edge blanking, the selected blanked sources are suppressed for rising edge, as well as falling edge, auto-shutdown, and period events.

The blanking counters are incremented on the rising edge of psmc\_clk. Blanked sources are suppressed until the counter value equals the blanking time register causing the blanking to terminate.

As the rising and falling edge events are from asynchronous inputs, there may be some uncertainty in the actual blanking time implemented in each cycle. The maximum uncertainty is equal to one psmc\_clk period.

PSMCxSTR0	01h	7				
		02h	04h	08h	10h	20h
Period Event						
Rising Edge Event						
Falling Edge Event						
PSMCxA (1H)						
PSMCxB (1L)						
PSMCxC (2H)						
PSMCxD (2L)						
PSMCxE (3H)						-
PSMCxF (3L)						

## FIGURE 24-15: 3-PHASE PWM STEERING WAVEFORM (PXHSMEN = 0 AND PXLSMEN = 1)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
PSMCxTMRL<7:0>								
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'		
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets	
'1' = Bit is set		'0' = Bit is clea	ared					

## REGISTER 24-17: PSMCxTMRL: PSMC TIME BASE COUNTER LOW REGISTER

bit 7-0 **PSMCxTMRL<7:0>:** 16-bit PSMCx Time Base Counter Least Significant bits = PSMCxTMR<7:0>

## REGISTER 24-18: PSMCxTMRH: PSMC TIME BASE COUNTER HIGH REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1
			PSMCxTN	//RH<7:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0

PSMCxTMRH<7:0>: 16-bit PSMCx Time Base Counter Most Significant bits

= PSMCxTMR<15:8>

## 25.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 25-3 shows a typical waveform of the PWM signal.

#### 25.3.1 STANDARD PWM OPERATION

The standard PWM function described in this section is available and identical for all CCP modules.

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to 10 bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- · PR2 registers
- T2CON registers
- CCPRxL registers
- · CCPxCON registers

Figure 25-4 shows a simplified block diagram of PWM operation.

- Note 1: The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.
  - 2: Clearing the CCPxCON register will relinquish control of the CCPx pin.

#### FIGURE 25-3: CCP PWM OUTPUT SIGNAL





SIMPLIFIED PWM BLOCK DIAGRAM



#### 26.6.6 I<sup>2</sup>C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPBUF register. This action will set the Buffer Full flag bit, BF and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted. SCL is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCL is released high. When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an ACK bit during the ninth bit time if an address match occurred, or if data was received properly. The status of ACK is written into the ACKSTAT bit on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSP1IF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 26-27).

After the write to the SSPBUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will release the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT Status bit of the SSPCON2 register. Following the falling edge of the ninth clock transmission of the address, the SSP1IF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

#### 26.6.6.1 BF Status Flag

In Transmit mode, the BF bit of the SSPSTAT register is set when the CPU writes to SSPBUF and is cleared when all 8 bits are shifted out.

#### 26.6.6.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write does not occur).

WCOL must be cleared by software before the next transmission.

#### 26.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit of the SSPCON2 register is cleared when the slave has sent an Acknowledge (ACK = 0) and is set when the slave does not Acknowledge (ACK = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

26.6.6.4 Typical transmit sequence:

- 1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
- 2. SSP1IF is set by hardware on completion of the Start.
- 3. SSP1IF is cleared by software.
- 4. The MSSP module will wait the required start time before any other operation takes place.
- 5. The user loads the SSPBUF with the slave address to transmit.
- 6. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
- The MSSP module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
- 8. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
- 9. The user loads the SSPBUF with eight bits of data.
- 10. Data is shifted out the SDA pin until all 8 bits are transmitted.
- 11. The MSSP module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
- 12. Steps 8-11 are repeated for all transmitted data bytes.
- The user generates a Stop or Restart condition by setting the PEN or RSEN bits of the SSP-CON2 register. Interrupt is generated once the Stop/Restart condition is complete.



### FIGURE 27-10: SYNCHRONOUS TRANSMISSION





## TABLE 27-7:SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER<br/>TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	111
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	322
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	79
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	80
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	83
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	321
SPBRGL				BRG<	7:0>				323
SPBRGH				BRG<	15:8>				323
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	125
TXREG	EUSART Transmit Data Register								312*
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	320

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous master transmission. \* Page provides register information.

## 27.5.1.5 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCSTA register) or the Continuous Receive Enable bit (CREN of the RCSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

Note:	If the RX/DT function is on an analog pin,
	the corresponding ANSEL bit must be
	cleared for the receiver to function.

## 27.5.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

**Note:** If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared.

## 27.5.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCREG is read to access the FIFO. When this happens the OERR bit of the RCSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters

will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

### 27.5.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift 9-bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

## 27.5.1.9 Synchronous Master Reception Set-up:

- 1. Initialize the SPBRGH, SPBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- 3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 4. Ensure bits CREN and SREN are clear.
- 5. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 6. If 9-bit reception is desired, set bit RX9.
- 7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
- 8. Interrupt flag bit RCIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 10. Read the 8-bit received data by reading the RCREG register.
- 11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

# PIC16(L)F1782/3

Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, CIN = 0.1 µF, TA = 25°C.



FIGURE 31-49: IPD, Comparator, NP Mode (CxSP = 1), PIC16LF1782/3 Only.



FIGURE 31-50: IPD, Comparator, NP Mode (CxSP = 1), PIC16F1782/3 Only.



FIGURE 31-51: Voh vs. Ioh Over Temperature, VDD = 5.0V, PIC16F1782/3 Only.



FIGURE 31-53: Voh vs. Ioh Over Temperature, VDD = 3.0V.



FIGURE 31-52: Vol vs. Iol Over Temperature, VDD = 5.0V, PIC16F1782/3 Only.



FIGURE 31-54: Vol vs. Iol Over Temperature, VDD = 3.0V.

3.5

3.0

2.5

2.0

1.0

0.5

ε

М 1.5

# PIC16(L)F1782/3

Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, CIN = 0.1  $\mu$ F, TA = 25°C.







FIGURE 31-69: PWRT Period, PIC16F1782/3 Only.









FIGURE 31-72: POR Rearm Voltage, NP Mode (VREGPM = 0), PIC16F1782/3 Only.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	N	<b>IILLIMETER</b>	S	
Dimension	MIN	NOM	MAX	
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

## 28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A