What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1783t-i-ml

3.6.1 TRADITIONAL DATA MEMORY

The traditional data memory is a region from FSR address 0x000 to FSR address 0xFFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.
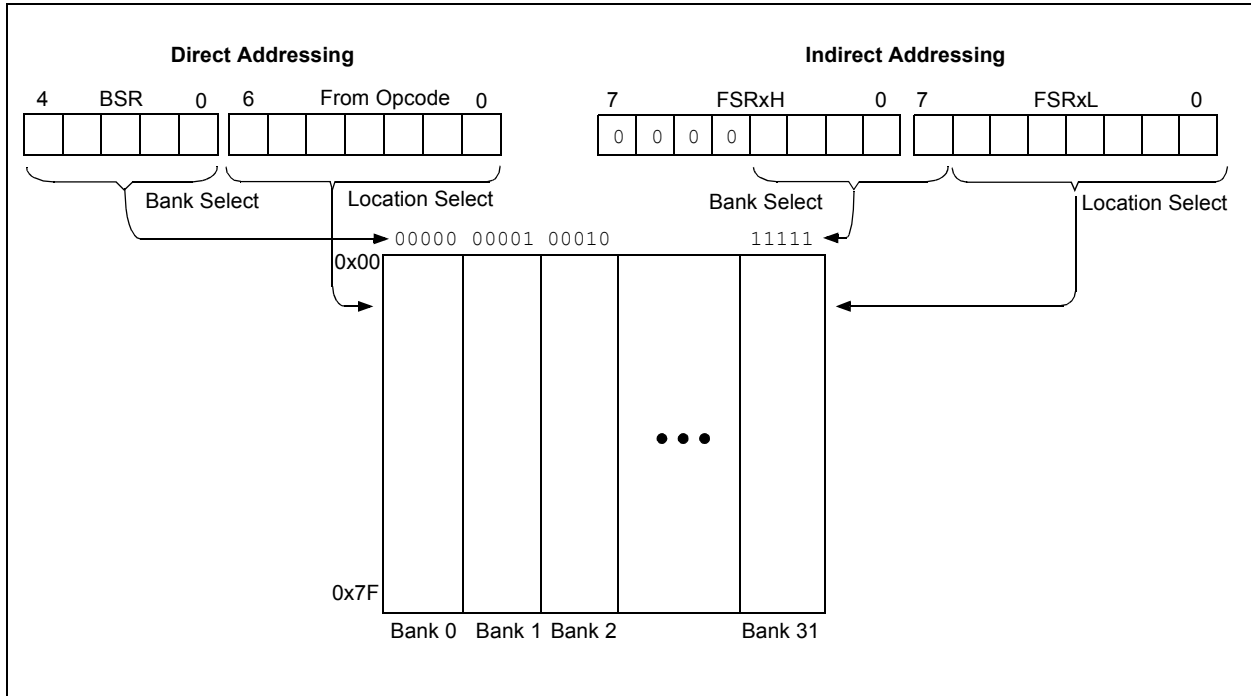
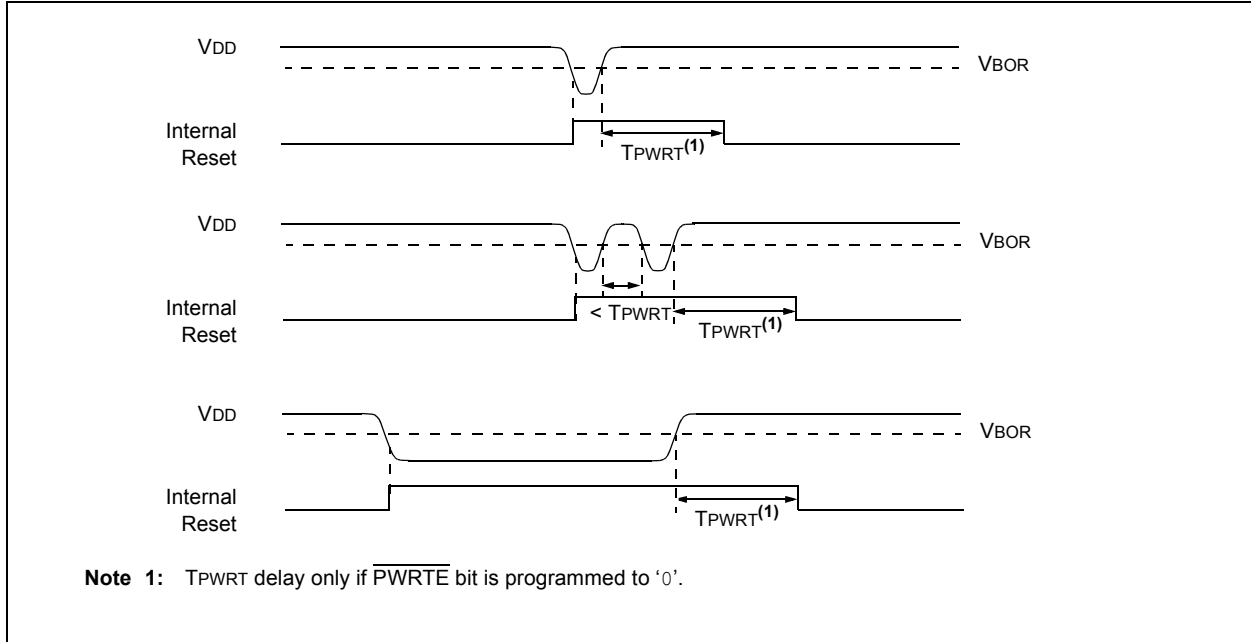**FIGURE 3-10: TRADITIONAL DATA MEMORY MAP**

FIGURE 5-2: **BROWN-OUT SITUATIONS**

Note 1: T$_{PWRT}$ delay only if $\overline{PWRTE}$ bit is programmed to '0'.

5.3 Register Definitions: BOR Control

REGISTER 5-1: **BORCON: BROWN-OUT RESET CONTROL REGISTER**

R/W-1/u	R/W-0/u	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN	BORFS	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7   **SBOREN:** Software Brown-out Reset Enable bit
<u>If BOREN <1:0> in Configuration Words ≠ 01:</u>
SBOREN is read/write, but has no effect on the BOR.
<u>If BOREN <1:0> in Configuration Words = 01:</u>
1 = BOR Enabled
0 = BOR Disabled

bit 6   **BORFS:** Brown-out Reset Fast Start bit[1]
<u>If BOREN<1:0> = 11 (Always on) or BOREN<1:0> = 00 (Always off)</u>
BORFS is Read/Write, but has no effect.
<u>If BOREN <1:0> = 10 (Disabled in Sleep) or BOREN<1:0> = 01 (Under software control):</u>
1 = Band gap is forced on always (covers sleep/wake-up/operating cases)
0 = Band gap operates normally, and may turn off

bit 5-1   **Unimplemented:** Read as '0'

bit 0   **BORRDY:** Brown-out Reset Circuit Ready Status bit
1 = The Brown-out Reset circuit is active
0 = The Brown-out Reset circuit is inactive

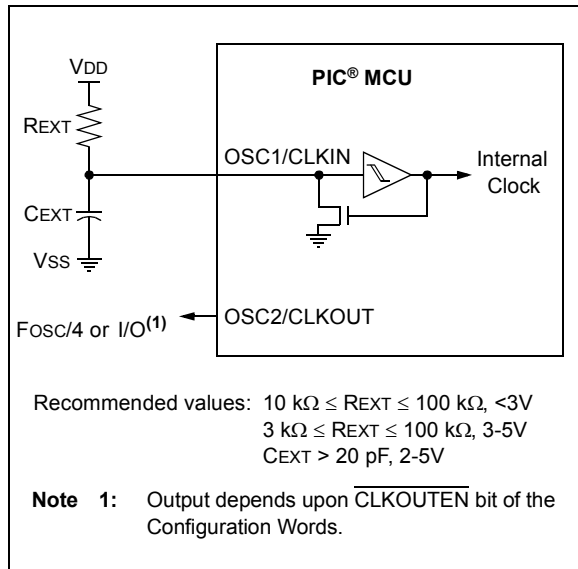**Note 1:** BOREN<1:0> bits are located in Configuration Words.

6.2.1.6 External RC Mode

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required.

The RC circuit connects to OSC1. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. The function of the OSC2/CLKOUT pin is determined by the CLKOUTEN bit in Configuration Words.

Figure 6-6 shows the external RC mode connections.

FIGURE 6-6: EXTERNAL RC MODES

Recommended values: $10\ k\Omega \leq R_{EXT} \leq 100\ k\Omega$, <3V
$3\ k\Omega \leq R_{EXT} \leq 100\ k\Omega$, 3-5V
$C_{EXT} > 20\ pF$, 2-5V

Note 1: Output depends upon CLKOUTEN bit of the Configuration Words.

The RC oscillator frequency is a function of the supply voltage, the resistor (R_{EXT}) and capacitor (C_{EXT}) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

6.2.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the FOSC<2:0> bits in Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to the internal oscillator during run-time. See **Section 6.3 "Clock Switching"** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the CLKOUTEN bit in Configuration Words.

The internal oscillator block has two independent oscillators and a dedicated Phase-Lock Loop, HFPLL that can produce one of three internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 16 MHz. The HFINTOSC source is generated from the 500 kHz MFINTOSC source and the dedicated Phase-Lock Loop, HFPLL. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 6-3).

2. The **MFINTOSC** (Medium-Frequency Internal Oscillator) is factory calibrated and operates at 500 kHz. The frequency of the MFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 6-3).

3. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

REGISTER 6-2: **OSCSTAT: OSCILLATOR STATUS REGISTER**

R-1/q	R-0/q	R-q/q	R-0/q	R-0/q	R-q/q	R-0/0	R-0/q
T1OSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Conditional

bit 7 **T1OSCR:** Timer1 Oscillator Ready bit
If T1OSCEN = 1:
1 = Timer1 oscillator is ready
0 = Timer1 oscillator is not ready
If T1OSCEN = 0:
1 = Timer1 clock source is always ready

bit 6 **PLLR** 4x PLL Ready bit
1 = 4x PLL is ready
0 = 4x PLL is not ready

bit 5 **OSTS:** Oscillator Start-up Timer Status bit
1 = Running from the clock defined by the FOSC<2:0> bits of the Configuration Words
0 = Running from an internal oscillator (FOSC<2:0> = 100)

bit 4 **HFIOFR:** High-Frequency Internal Oscillator Ready bit
1 = HFINTOSC is ready
0 = HFINTOSC is not ready

bit 3 **HFIOFL:** High-Frequency Internal Oscillator Locked bit
1 = HFINTOSC is at least 2% accurate
0 = HFINTOSC is not 2% accurate

bit 2 **MFIOFR:** Medium-Frequency Internal Oscillator Ready bit
1 = MFINTOSC is ready
0 = MFINTOSC is not ready

bit 1 **LFIOFR:** Low-Frequency Internal Oscillator Ready bit
1 = LFINTOSC is ready
0 = LFINTOSC is not ready

bit 0 **HFIOFS:** High-Frequency Internal Oscillator Stable bit
1 = HFINTOSC is at least 0.5% accurate
0 = HFINTOSC is not 0.5% accurate

REGISTER 13-5: ANSELA: PORTA ANALOG SELECT REGISTER

R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
ANSA7	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 5   **ANSA7**: Analog Select between Analog or Digital Function on pins RA7, respectively
          0 = Digital I/O. Pin is assigned to port or digital special function.
          1 = Analog input. Pin is assigned as analog input[1]. Digital input buffer disabled.

bit 6   **Unimplemented:** Read as '0'

bit 5-0   **ANSA<5:0>**: Analog Select between Analog or Digital Function on pins RA<5:0>, respectively
          0 = Digital I/O. Pin is assigned to port or digital special function.
          1 = Analog input. Pin is assigned as analog input[1]. Digital input buffer disabled.

Note   1:   When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 13-6: WPUA: WEAK PULL-UP PORTA REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0   **WPUA<7:0>**: Weak Pull-up Register bits
          1 = Pull-up enabled
          0 = Pull-up disabled

Note   1:   Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
     2:   The weak pull-up device is automatically disabled if the pin is in configured as an output.

17.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
  - Single-ended
  - Differential
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Result formatting

17.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to **Section 13.0 "I/O Ports"** for more information.

> **Note:** Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

17.1.2 CHANNEL SELECTION

There are up to 14 channel selections available:

- AN<13:8, 4:0> pins
- Temperature Indicator
- DAC_output
- FVR (Fixed Voltage Reference) Output

Refer to **Section 15.0 "Fixed Voltage Reference (FVR)"** and **Section 16.0 "Temperature Indicator Module"** for more information on these channel selections.

When converting differential signals, the negative input for the channel is selected with the CHSN<3:0> bits of the ADCON2 register. Any positive input can be paired with any negative input to determine the differential channel.

The CHS<4:0> bits of the ADCON0 register determine which positive channel is selected.

When CHSN<3:0> = 1111 then the ADC is effectively a single ended ADC converter.

When changing channels, a delay is required before starting the next conversion.

17.1.3 ADC VOLTAGE REFERENCE

The ADPREF bits of the ADCON1 register provide control of the positive voltage reference. The positive voltage reference can be:

- V$_{REF}$+
- V$_{DD}$
- FVR Buffer1

The ADNREF bits of the ADCON1 register provide control of the negative voltage reference. The negative voltage reference can be:

- V$_{REF}$- pin
- V$_{SS}$

See **Section 15.0 "Fixed Voltage Reference (FVR)"** for more details on the Fixed Voltage Reference.

17.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- F$_{OSC}$/2
- F$_{OSC}$/4
- F$_{OSC}$/8
- F$_{OSC}$/16
- F$_{OSC}$/32
- F$_{OSC}$/64
- F$_{RC}$ (dedicated internal F$_{RC}$ oscillator)

The time to complete one bit conversion is defined as T$_{AD}$. One full 12-bit conversion requires 15 T$_{AD}$ periods as shown in Figure 17-2.

For correct conversion, the appropriate T$_{AD}$ specification must be met. Refer to the ADC conversion requirements in **Section 30.0 "Electrical Specifications"** for more information. Table 17-1 gives examples of appropriate ADC clock selections.

> **Note:** Unless using the F$_{RC}$, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

PIC16(L)F1782/3

19.0 DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 256 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- Op amp positive input
- ADC input channel
- DACOUT1 pin
- DACOUT2 pin

The Digital-to-Analog Converter (DAC) is enabled by setting the DACEN bit of the DACCON0 register.

19.1 Output Voltage Selection

The DAC has 256 voltage level ranges. The 256 levels are set with the DACR<7:0> bits of the DACCON1 register.

The DAC output voltage is determined by Equation 19-1:

EQUATION 19-1: DAC OUTPUT VOLTAGE

$$IF\ DACxEN = 1$$

$$V_{OUT} = \left((V_{SOURCE+} - V_{SOURCE-}) \times \frac{DACxR[7:0]}{2^8} \right) + V_{SOURCE-}$$

$$V_{SOURCE+} = V_{DD},\ V_{REF},\ or\ FVR\ BUFFER\ 2$$

$$V_{SOURCE-} = V_{SS}$$

19.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in **Section 30.0 "Electrical Specifications"**.

19.3 DAC Voltage Reference Output

The DAC voltage can be output to the DACOUT1 and DACOUT2 pins by setting the respective DACOE1 and DACOE2 pins of the DACCON0 register. Selecting the DAC reference voltage for output on either DACOUTx pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DACOUTx pin when it has been configured for DAC reference voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to either DACOUTx pin. Figure 19-2 shows an example buffering technique.

TABLE 23-1:   SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				255
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	79
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	80
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	83
PR2	Timer2 Module Period Register								186*
T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		188
TMR2	Holding Register for the 8-bit TMR2 Register								186*

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.

*   Page provides register information.

24.3.4 PUSH-PULL PWM WITH COMPLEMENTARY OUTPUTS

The complementary push-pull PWM is used to drive transistor bridge circuits as well as synchronous switches on the secondary side of the bridge. The PWM waveform is output on four pins presented as two pairs of two-output signals with a normal and complementary output in each pair. Dead band can be inserted between the normal and complementary outputs at the transition times.

24.3.4.1 Mode Features

- Dead-band control is available
- No steering control available
- Primary PWM output is only on:
  - PSMCxA
  - PSMCxB
- Complementary PWM output is only on:
  - PSMCxE
  - PSMCxF

> **Note:** This is a subset of the 6-pin output of the push-pull PWM output, which is why pin functions are fixed in these positions, so they are compatible with that mode. See **Section 24.3.6 "Push-Pull PWM with Four Full-Bridge and Complementary Outputs"**.

24.3.4.2 Waveform Generation

Push-Pull waveforms generate alternating outputs on the output pairs. Therefore, there are two sets of rising edge events and two sets of falling edge events

Odd numbered period rising edge event:

- PSMCxE is set inactive
- Dead-band rising is activated (if enabled)
- PSMCxA is set active

Odd numbered period falling edge odd event:

- PSMCxA is set inactive
- Dead-band falling is activated (if enabled)
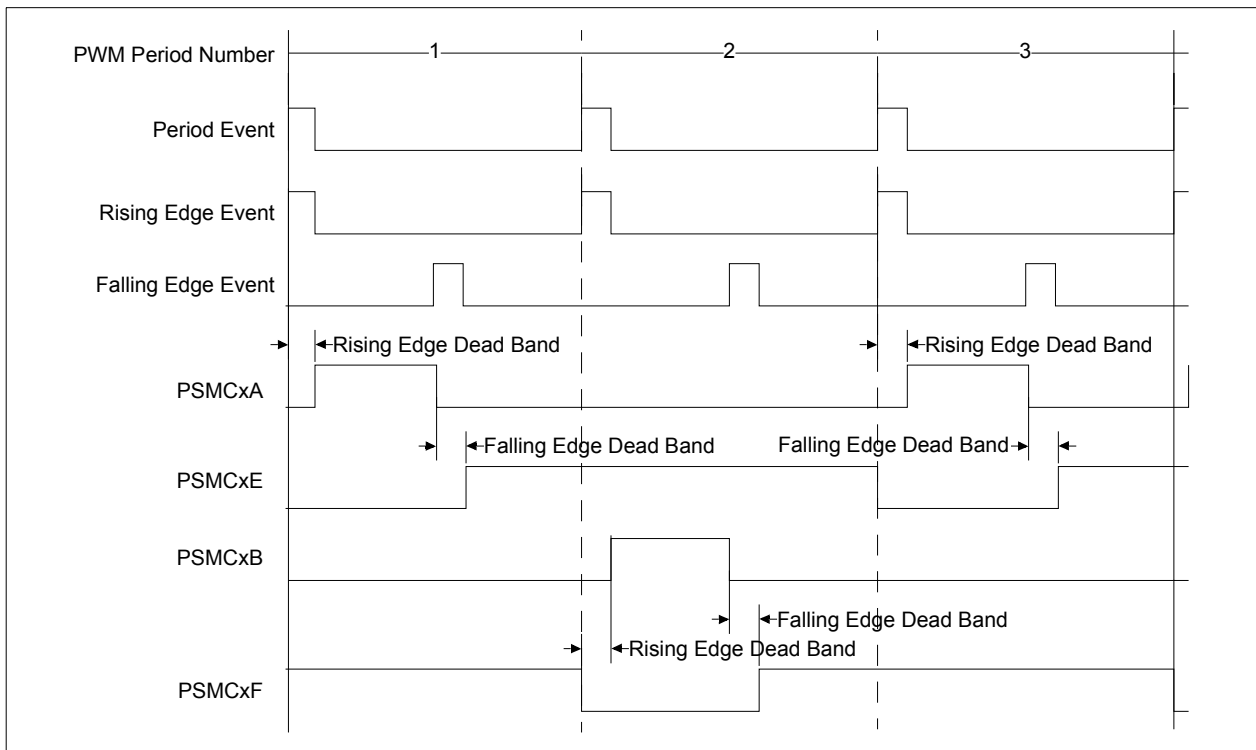- PSMCxE is set active

Even numbered period rising edge event:

- PSMCxF is set inactive
- Dead-band rising is activated (if enabled)
- PSMCxB is set active

Even numbered period falling edge event:

- PSMCxB is set inactive
- Dead-band falling is activated (if enabled)
- PSMCxF is set active

FIGURE 24-7: PUSH-PULL WITH COMPLEMENTARY OUTPUTS PWM WAVEFORM

PIC16(L)F1782/3

24.3.10 VARIABLE FREQUENCY – FIXED DUTY CYCLE PWM

This mode of operation is quite different from all of the other modes. It uses only the period event for waveform generation. At each period event, the PWM output is toggled.

The rising edge and falling edge events are unused in this mode.
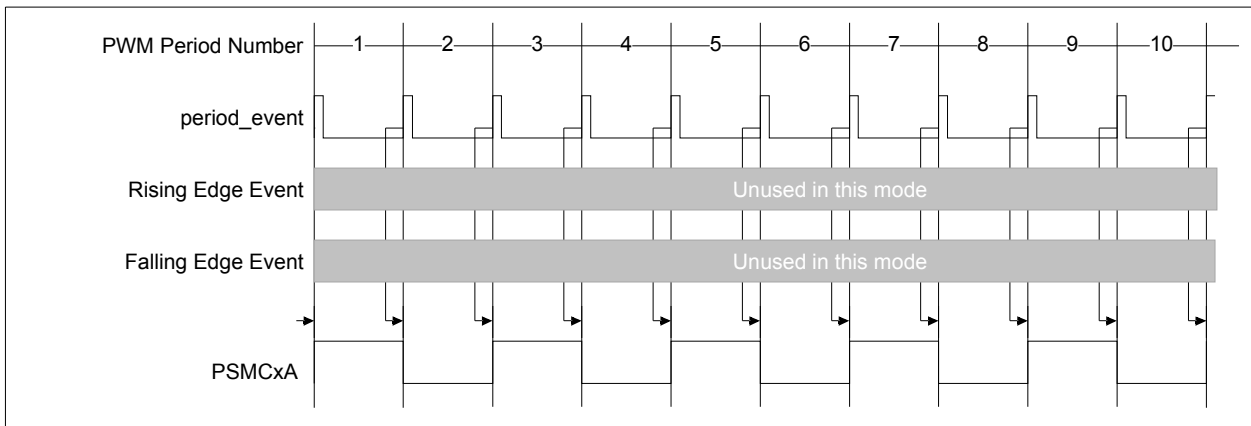
24.3.10.1 Mode Features

• No dead-band control available

• No steering control available

• Fractional Frequency Adjust
  - Fine period adjustments are made with the PSMC Fractional Frequency Adjust (PSMCxFFA) register (Register 24-27)

• PWM is output on the following pin only:
  - PSMCxA

24.3.10.2 Waveform Generation

Period Event

• Output of PSMCxA is toggled

• FFA counter is incremented by the 4-bit value in PSMCxF FA

FIGURE 24-13: VARIABLE FREQUENCY – FIXED DUTY CYCLE PWM WAVEFORM

24.3.11 VARIABLE FREQUENCY - FIXED DUTY CYCLE PWM WITH COMPLEMENTARY OUTPUTS

This mode is the same as the single output Fixed Duty Cycle mode except a complementary output with dead-band control is generated.

The rising edge and falling edge events are unused in this mode. Therefore, a different triggering mechanism is required for the dead-band counters.

A period events that generate a rising edge on PSMCxA use the rising edge dead-band counters.

A period events that generate a falling edge on PSMCxA use the falling edge dead-band counters.

24.3.11.1 Mode Features

- Dead-band control is available
- No steering control available
- Fractional Frequency Adjust
  - Fine period adjustments are made with the PSMC Fractional Frequency Adjust (PSMCxFFA) register (Register 24-27)
- Primary PWM is output to the following pin:
  - PSMCxA
- Complementary PWM is output to the following pin:
  - PSMCxB

24.3.11.2 Waveform Generation

Period Event

When output is going inactive to active:

- Complementary output is set inactive
- FFA counter is incremented by the 4-bit value in PSMCFFA register.
- Dead-band rising is activated (if enabled)
- Primary output is set active

When output is going active to inactive:

- Primary output is set inactive
- FFA counter is incremented by the 4-bit value in PSMCFFA register
- Dead-band falling is activated (if enabled)
- Complementary output is set active

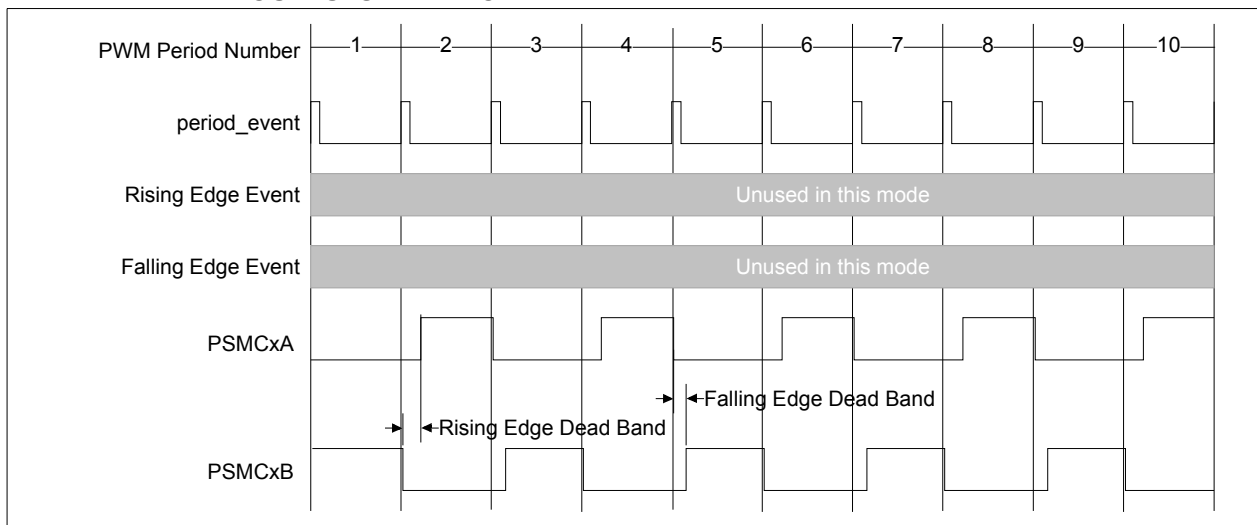**FIGURE 24-14:** VARIABLE FREQUENCY – FIXED DUTY CYCLE PWM WITH COMPLEMENTARY OUTPUTS WAVEFORM

TABLE 24-4:   SAMPLE FFA OUTPUT PERIODS/FREQUENCIES

FFA number	Output Frequency (kHz)	Step Size (Hz)
0	125.000	0
1	124.970	-30.4
2	124.939	-60.8
3	124.909	-91.2
4	124.878	-121.6
5	124.848	-152.0
6	124.818	-182.4
7	124.787	-212.8
8	124.757	-243.2
9	124.726	-273.6
10	124.696	-304.0
11	124.666	-334.4
12	124.635	-364.8
13	124.605	-395.2
14	124.574	-425.6
15	124.544	-456.0

25.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 25-3 shows a typical waveform of the PWM signal.

25.3.1 STANDARD PWM OPERATION

The standard PWM function described in this section is available and identical for all CCP modules.

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to 10 bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PR2 registers
- T2CON registers
- CCPRxL registers
- CCPxCON registers

Figure 25-4 shows a simplified block diagram of PWM operation.

Note 1:	The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.
2:	Clearing the CCPxCON register will relinquish control of the CCPx pin.

FIGURE 25-3: CCP PWM OUTPUT SIGNAL
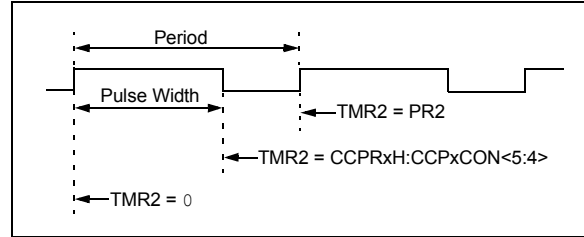
FIGURE 25-4: SIMPLIFIED PWM BLOCK DIAGRAM

Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (F_{OSC}), or 2 bits of the prescaler, to create the 10-bit time base.

2: In PWM mode, CCPR1H is a read-only register.
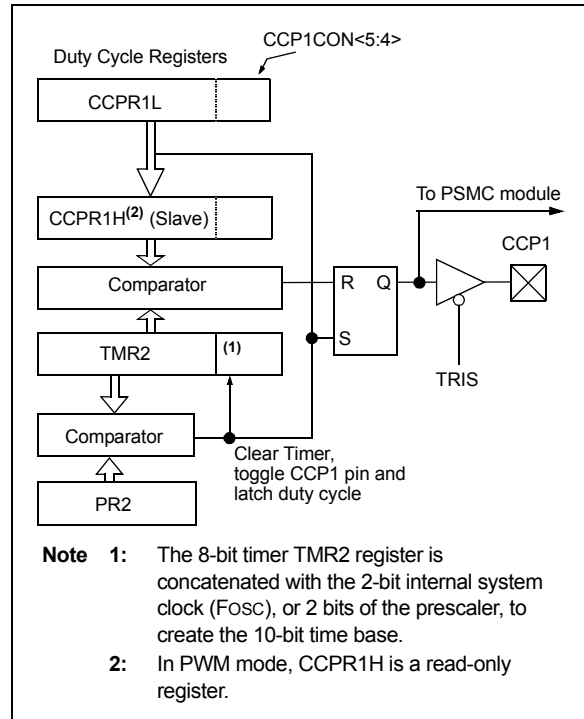
26.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 26-32).

b) SCL is sampled low before SDA is asserted low (Figure 26-33).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

• the Start condition is aborted,

• the BCL1IF flag is set and

• the MSSP module is reset to its Idle state (Figure 26-32).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 26-34). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

> **Note:** The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

FIGURE 26-33:   BUS COLLISION DURING START CONDITION (SDA ONLY)
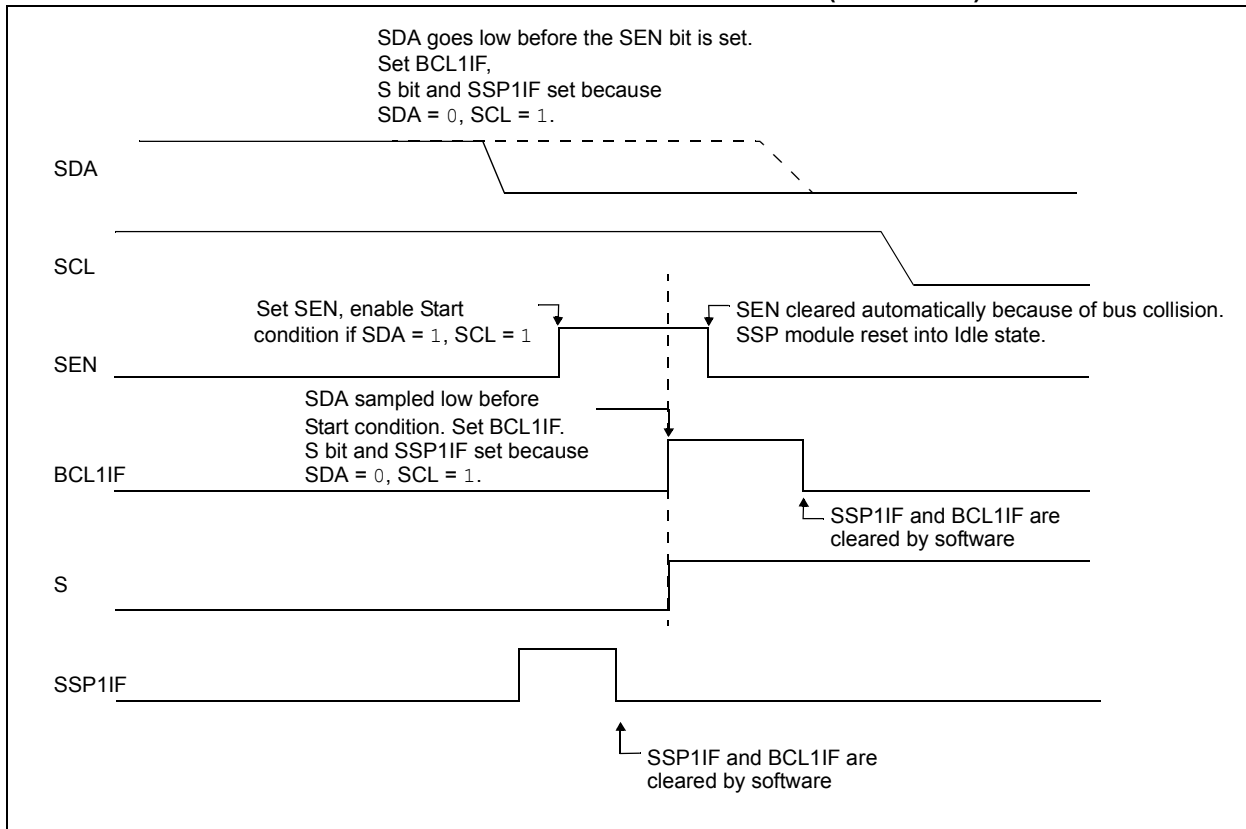
27.5 EUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The EUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

27.5.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the EUSART for synchronous master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the EUSART.

27.5.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the EUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

27.5.1.2 Clock Polarity

A clock polarity option is provided for Microwire compatibility. Clock polarity is selected with the SCKP bit of the BAUDCON register. Setting the SCKP bit sets the clock Idle state as high. When the SCKP bit is set, the data changes on the falling edge of each clock.

Clearing the SCKP bit sets the Idle state as low. When the SCKP bit is cleared, the data changes on the rising edge of each clock.

27.5.1.3 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the EUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXREG register. If the TSR still contains all or part of a previous character the new character data is held in the TXREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

> **Note:** The TSR register is not mapped in data memory, so it is not available to the user.

27.5.1.4 Synchronous Master Transmission Set-up:

1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 27.4 "EUSART Baud Rate Generator (BRG)"**).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
3. Disable Receive mode by clearing bits SREN and CREN.
4. Enable Transmit mode by setting the TXEN bit.
5. If 9-bit transmission is desired, set the TX9 bit.
6. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
8. Start transmission by loading data to the TXREG register.

MOVIW	Move INDFn to W
Syntax:	[*label*] MOVIW ++FSRn [*label*] MOVIW --FSRn [*label*] MOVIW FSRn++ [*label*] MOVIW FSRn-- [*label*] MOVIW k[FSRn]
Operands:	$n \in [0,1]$ $mm \in [00,01, 10, 11]$ $-32 \le k \le 31$
Operation:	INDFn $\rightarrow$ W Effective address is determined by • FSR + 1 (preincrement) • FSR - 1 (predecrement) • FSR + k (relative offset) After the Move, the FSR value will be either: • FSR + 1 (all increments) • FSR - 1 (all decrements) • Unchanged
Status Affected:	Z

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

Description:	This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it. Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn. FSRn is limited to the range 0000h - FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

MOVLB	Move literal to BSR
Syntax:	[*label*] MOVLB k
Operands:	$0 \le k \le 31$
Operation:	k $\rightarrow$ BSR
Status Affected:	None
Description:	The 5-bit literal 'k' is loaded into the Bank Select Register (BSR).

MOVLP	Move literal to PCLATH
Syntax:	[*label*] MOVLP k
Operands:	$0 \le k \le 127$
Operation:	k $\rightarrow$ PCLATH
Status Affected:	None
Description:	The 7-bit literal 'k' is loaded into the PCLATH register.

MOVLW	Move literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k $\rightarrow$ (W)
Status Affected:	None
Description:	The 8-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
Example:	MOVLW 0x5A

After Instruction
        W   =   0x5A

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	$0 \le f \le 127$
Operation:	(W) $\rightarrow$ (f)
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example:	MOVWF OPTION_REG

Before Instruction
        OPTION_REG = 0xFF
                W = 0x4F
After Instruction
        OPTION_REG = 0x4F
                W = 0x4F

TABLE 30-19:   EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
		Standard Operating Conditions (unless otherwise stated)				
US125	$T_{DTV2CKL}$	SYNC RCV (Master and Slave) Data-hold before CK ↓ (DT hold time)	10	—	ns	
US126	$T_{CKL2DTL}$	Data-hold after CK ↓ (DT hold time)	15	—	ns	

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.
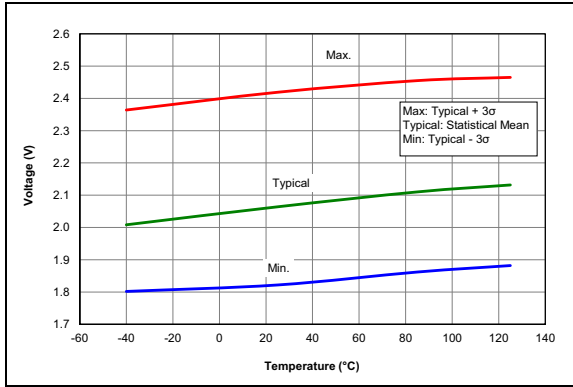
FIGURE 31-67: *LPBOR Reset Voltage.*
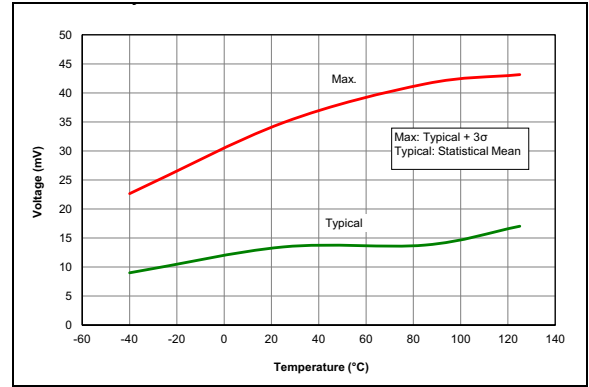
FIGURE 31-68: *LPBOR Reset Hysteresis.*
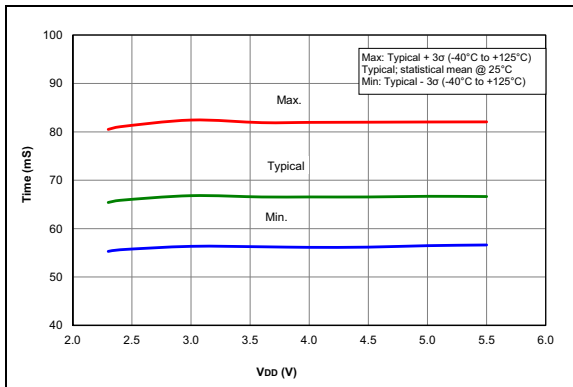

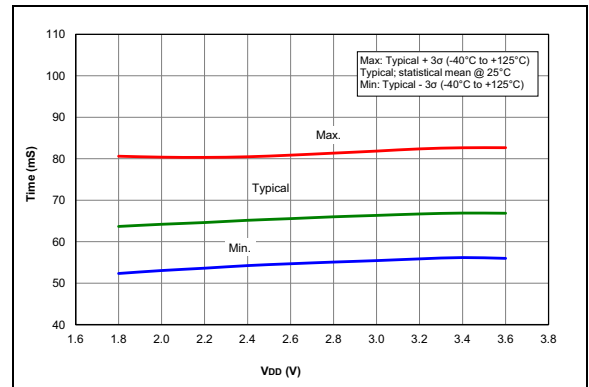**FIGURE 31-69:** *PWRT Period, PIC16F1782/3 Only.*

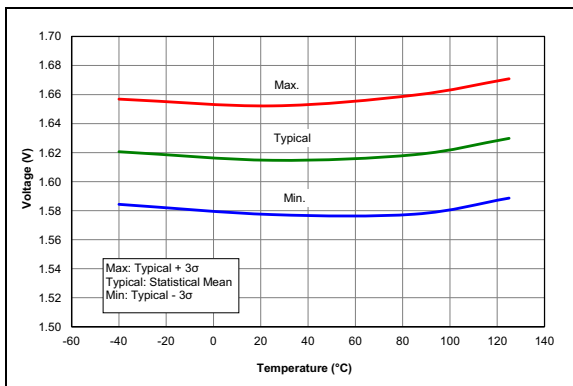**FIGURE 31-70:** *PWRT Period, PIC16LF1782/3 Only.*

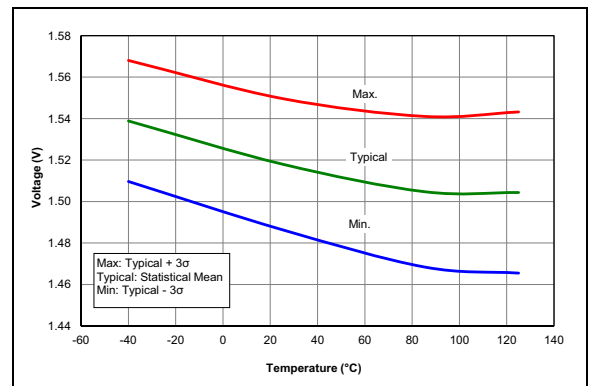**FIGURE 31-71:** *POR Release Voltage.*

FIGURE 31-72: *POR Rearm Voltage, NP Mode (VREGPM = 0), PIC16F1782/3 Only.*

PIC16(L)F1782/3

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 4x4 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	W2			2.35
Optional Center Pad Length	T2			2.35
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2152A

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APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (04/2011)

Original release.

Revision B (06/2011)

Revised Section 18.0; Revised Table 30-8; Add Operational Amplifier Table.

Revision C (03/2012)

Electrical Specifications update.

Revision D (11/2012)

Revised: Table 5-4, Section 6.2.1.3, 9.0, Table 15-1 (LDO), Figure 16-1, Section 17.1.6, 17.2.3, 20.7, 24.1, 24.1.1-24.1.3, 24.2.7, 24.2.8, 24.3.4.1, 24.3.11, 24.8.1.1-24.8.1.3; Register 24.2 (PxMSRC description); Registers 24-9-24-13, 24-16, 25-1 (Bits 0-3 descriptions); Add Table 16-2, Section 24.2.7.3.

Electrical Specifications update: Revised 30.2 (D010, D012), 30.3 (D023, D025, D026, D029-D031); Table 30-4 (delete Note 2); Table 30-1 (Param. OPA08, OPA09), Table 30-11, Table 30-12 (Param. DAC02).

Revision E (3/2014)

Change from Preliminary to Final data sheet.

Corrected the following Tables: Family Types Table on page 3, Table 3-3, Table 3-8, Table 20-3, Table 22-2, Table 22-3, Table 23-1, Table 25-3, Table 30-1, Table 30-2, Table 30-3, Table 30-6, Table 30-7, Table 30-13, Table 30-14, Table 30-15, Table 30-16, Table 30-20.

Corrected the following Sections: Section 3.2, Section 9.2, Section 13.3, Section 17.1.6, Section 15.1, Section 15.3, Section 17.2.5, Section 18.2, Section 18.3, Section 19.0, Section 22.6.5, Section 22.9, Section 23.0, Section 23.1, Section 24.2.4, Section 24.2.5, Section 24.2.7, Section 24.8, Section 25.0, Section 26.6.7.4, Section 30.3.

Corrected the following Registers: Register 4-2, Register 8-2, Register 8-5, Register 17-3, Register 18-1, Register 24-3, Register 24-4.

Corrected Equation 17-1.

Corrected Figure 30-9. Removed Figure 24-21.