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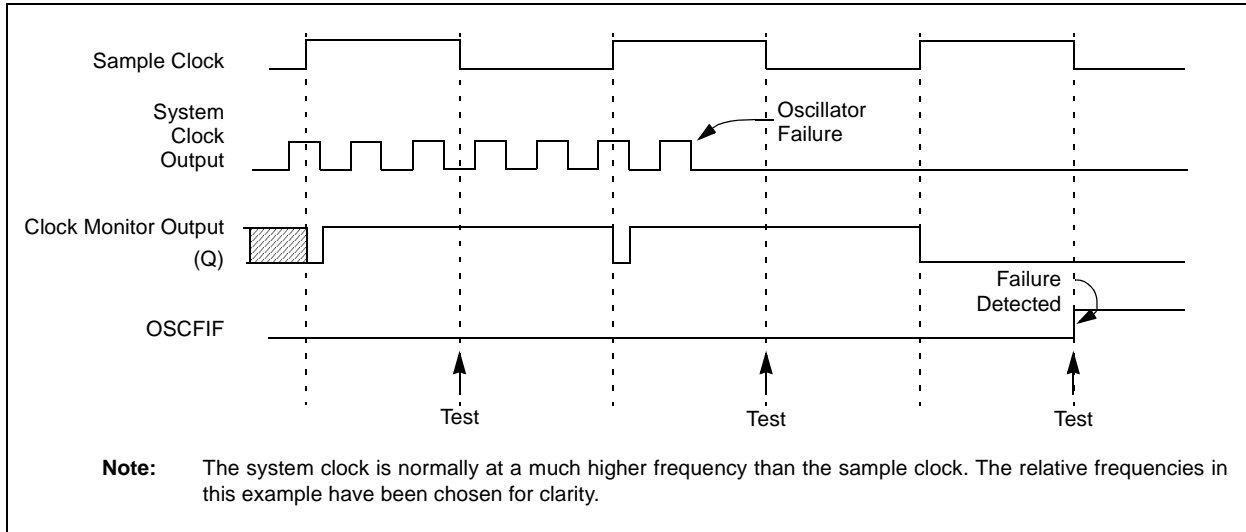
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f684-e-sl">https://www.e-xfl.com/product-detail/microchip-technology/pic16f684-e-sl</a>

# PIC16F684

**FIGURE 3-9: FSCM TIMING DIAGRAM**



**TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets <sup>(1)</sup>
CONFIG <sup>(2)</sup>	CPD	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—
OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 x000	-110 x000
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000

**Legend:** x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

**Note 1:** Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

**2:** See Configuration Word register (Register 12-1) for operation of all register bits.

## REGISTER 4-4: WPUA: WEAK PULL-UP PORTA REGISTER

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-6      **Unimplemented:** Read as '0'

bit 5-4      **WPUA<5:4>:** Weak Pull-up Control bits  
                  1 = Pull-up enabled  
                  0 = Pull-up disabled

bit 3        **Unimplemented:** Read as '0'

bit 2-0      **WPUA<2:0>:** Weak Pull-up Control bits  
                  1 = Pull-up enabled  
                  0 = Pull-up disabled

- Note 1:** Global  $\overline{\text{RAPU}}$  must be enabled for individual pull-ups to be enabled.  
**2:** The weak pull-up device is automatically disabled if the pin is in Output mode ( $\text{TRISA} = 0$ ).  
**3:** The RA3 pull-up is enabled when configured as  $\overline{\text{MCLR}}$  and disabled as an I/O in the Configuration Word.  
**4:** WPUA<5:4> always reads '1' in XT, HS and LP OSC modes.

## REGISTER 4-5: IOCA: INTERRUPT-ON-CHANGE PORTA REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-6      **Unimplemented:** Read as '0'

bit 5-0      **IOCA<5:0>:** Interrupt-on-change PORTA Control bit  
                  1 = Interrupt-on-change enabled  
                  0 = Interrupt-on-change disabled

- Note 1:** Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized.  
**2:** IOCA<5:4> always reads '1' in XT, HS and LP OSC modes.

## REGISTER 5-1: OPTION\_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 7                       **$\overline{\text{RAPU}}$** : PORTA Pull-up Enable bit  
 1 = PORTA pull-ups are disabled  
 0 = PORTA pull-ups are enabled by individual PORT latch values
- bit 6                      **INTEDG**: Interrupt Edge Select bit  
 1 = Interrupt on rising edge of INT pin  
 0 = Interrupt on falling edge of INT pin
- bit 5                      **T0CS**: TMR0 Clock Source Select bit  
 1 = Transition on T0CKI pin  
 0 = Internal instruction cycle clock ( $F_{\text{OSC}}/4$ )
- bit 4                      **T0SE**: TMR0 Source Edge Select bit  
 1 = Increment on high-to-low transition on T0CKI pin  
 0 = Increment on low-to-high transition on T0CKI pin
- bit 3                      **PSA**: Prescaler Assignment bit  
 1 = Prescaler is assigned to the WDT  
 0 = Prescaler is assigned to the Timer0 module
- bit 2-0                      **PS<2:0>**: Prescaler Rate Select bits

BIT VALUE	TMR0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

**Note 1:** A dedicated 16-bit WDT postscaler is available. See **Section 12.6 “Watchdog Timer (WDT)”** for more information.

**TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

**Legend:** — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

## 8.3 Comparator Control

The CMCON0 register (Register 8-1) provides access to the following comparator features:

- Mode selection
- Output state
- Output polarity
- Input switch

### 8.3.1 COMPARATOR OUTPUT STATE

Each comparator state can always be read internally via the associated CxOUT bit of the CMCON0 register. The comparator outputs are directed to the CxOUT pins when CM<2:0> = 110. When this mode is selected, the TRIS bits for the associated CxOUT pins must be cleared to enable the output drivers.

### 8.3.2 COMPARATOR OUTPUT POLARITY

Inverting the output of a comparator is functionally equivalent to swapping the comparator inputs. The polarity of a comparator output can be inverted by setting the CxINV bits of the CMCON0 register. Clearing CxINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 8-1.

**TABLE 8-1: OUTPUT STATE VS. INPUT CONDITIONS**

Input Conditions	CxINV	CxOUT
VIN- > VIN+	0	0
VIN- < VIN+	0	1
VIN- > VIN+	1	1
VIN- < VIN+	1	0

**Note:** CxOUT refers to both the register bit and output pin.

### 8.3.3 COMPARATOR INPUT SWITCH

The inverting input of the comparators may be switched between two analog pins in the following modes:

- CM<2:0> = 001 (Comparator C1 only)
- CM<2:0> = 010 (Comparators C1 and C2)

In the above modes, both pins remain in Analog mode regardless of which pin is selected as the input. The CIS bit of the CMCON0 register controls the comparator input switch.

## 8.4 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See Comparator and Voltage Reference specifications of **Section 15.0 “Electrical Specifications”** for more details.

## 8.5 Comparator Interrupt Operation

The comparator interrupt flag is set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 8-2 and Figure 8-3). One latch is updated with the comparator output level when the CMCON0 register is read. This latch retains the value until the next read of the CMCON0 register or the occurrence of a reset. The other latch of the mismatch circuit is updated on every Q1 system clock. A mismatch condition will occur when a comparator output change is clocked through the second latch on the Q1 clock cycle. The mismatch condition will persist, holding the CxIF bit of the PIR1 register true, until either the CMCON0 register is read or the comparator output returns to the previous state.

**Note:** A write operation to the CMCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.

Software will need to maintain information about the status of the comparator output to determine the actual change that has occurred.

The CxIF bit of the PIR1 register is the comparator interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CxIE bit of the PIE1 register and the PEIE and GIE bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CxIF bit of the PIR1 register will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- Any read or write of CMCON0. This will end the mismatch condition.
- Clear the CxIF interrupt flag.

## 8.10 Comparator Voltage Reference

The comparator voltage reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- Two 16-level voltage ranges
- Output clamped to VSS
- Ratiometric with VDD

The VRCON register (Register ) controls the voltage reference module shown in Figure 8-8.

### 8.10.1 INDEPENDENT OPERATION

The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

### 8.10.2 OUTPUT VOLTAGE SELECTION

The CVREF voltage reference has 2 ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

### EQUATION 8-1: CVREF OUTPUT VOLTAGE

$$\begin{aligned}
 &VRR = 1 \text{ (low range):} \\
 &CVREF = (VR<3:0>/24) \times VDD \\
 &VRR = 0 \text{ (high range):} \\
 &CVREF = (VDD/4) + (VR<3:0> \times VDD/32)
 \end{aligned}$$

The full range of VSS to VDD cannot be realized due to the construction of the module. See Figure 8-8.

### 8.10.3 OUTPUT CLAMPED TO VSS

The CVREF output voltage can be set to VSS with no power consumption by configuring VRCON as follows:

- VREN = 0
- VRR = 1
- VR<3:0> = 0000

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

### 8.10.4 OUTPUT RATIOMETRIC TO VDD

The comparator voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 15.0 “Electrical Specifications”**.

## VRCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	—	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 7            **VREN:** CVREF Enable bit  
                   1 = CVREF circuit powered on  
                   0 = CVREF circuit powered down, no IDD drain and CVREF = VSS.
- bit 6            **Unimplemented:** Read as '0'
- bit 5            **VRR:** CVREF Range Selection bit  
                   1 = Low range  
                   0 = High range
- bit 4            **Unimplemented:** Read as '0'
- bit 3-0        **VR<3:0>:** CVREF Value Selection bits (0 ≤ VR<3:0> ≤ 15)  
                   When VRR = 1: CVREF = (VR<3:0>/24) \* VDD  
                   When VRR = 0: CVREF = VDD/4 + (VR<3:0>/32) \* VDD

# PIC16F684

**TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
ADCON0	ADFM	VCFG	—	CHS2	CHS1	CHS0	GO/DONE	ADON	0000 0000	0000 0000
ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	-000 ----
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	EEIE	ADIE	CCPIE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCPIF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	--uu uuuu
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx 0000	--uu uuuu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

**Legend:** x = unknown, u = unchanged, — = unimplemented read as '0'. Shaded cells are not used for ADC module.

# PIC16F684

## 10.1 EECON1 and EECON2 Registers

EECON1 is the control register with four low-order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset, or a WDT Time-out Reset during normal

operation. In these situations, following Reset, the user can check the WRERR bit, clear it and rewrite the location. The data and address will be cleared. Therefore, the EEDAT and EEADR registers will need to be re-initialized.

Interrupt flag, EEIF bit of the PIR1 register, is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

**Note:** The EECON1, EEDAT and EEADR registers should not be modified during a data EEPROM write (WR bit = 1).

### REGISTER 10-3: EECON1: EEPROM CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7							bit 0

**Legend:**

S = Bit can only be set  
 R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 7-4            **Unimplemented:** Read as '0'
- bit 3            **WRERR:** EEPROM Error Flag bit
  - 1 = A write operation is prematurely terminated (any MCLR Reset, any WDT Reset during normal operation or BOR Reset)
  - 0 = The write operation completed
- bit 2            **WREN:** EEPROM Write Enable bit
  - 1 = Allows write cycles
  - 0 = Inhibits write to the data EEPROM
- bit 1            **WR:** Write Control bit
  - 1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)
  - 0 = Write cycle to the data EEPROM is complete
- bit 0            **RD:** Read Control bit
  - 1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)
  - 0 = Does not initiate an EEPROM read



# PIC16F684

## 11.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

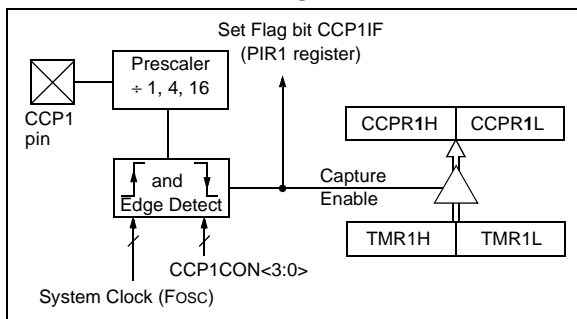
When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR1 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value (see Figure 11-1).

### 11.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

**Note:** If the CCP1 pin is configured as an output, a write to the port can cause a capture condition.

**FIGURE 11-1: CAPTURE MODE OPERATION BLOCK DIAGRAM**



### 11.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

### 11.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE1 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR1 register following any change in operating mode.

### 11.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler (see Example 11-1).

**EXAMPLE 11-1: CHANGING BETWEEN CAPTURE PRESCALERS**

```
BANKSEL CCP1CON    ;Set Bank bits to point
                   ;to CCP1CON
CLRWF  CCP1CON     ;Turn CCP module off
MOVLW  NEW_CAPT_PS;Load the W reg with
                   ; the new prescaler
MOVWF  CCP1CON     ; move value and CCP ON
MOVWF  CCP1CON     ;Load CCP1CON with this
                   ; value
```

# PIC16F684

## 11.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin. Since the CCP1 pin is multiplexed with the PORT data latch, the TRIS for that pin must be cleared to enable the CCP1 pin output driver.

**Note:** Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin.

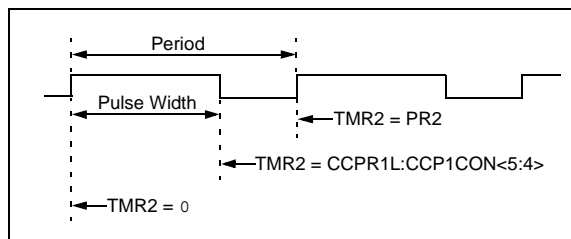
Figure 11-3 shows a simplified block diagram of PWM operation.

Figure 11-4 shows a typical waveform of the PWM signal.

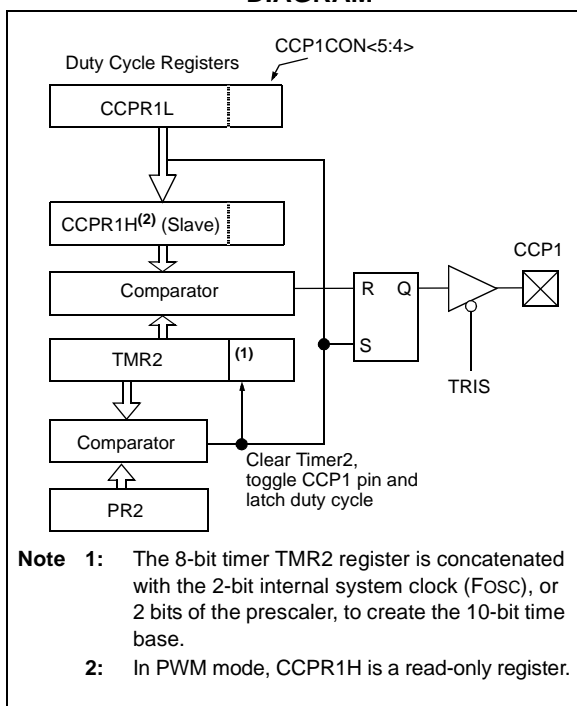
For a step by step procedure on how to set up the CCP module for PWM operation, see **Section 11.3.7 “Setup for PWM Operation”**.

The PWM output (Figure 11-4) has a time base (period) and a time that the output stays high (duty cycle).

**FIGURE 11-4: CCP PWM OUTPUT**



**FIGURE 11-3: SIMPLIFIED PWM BLOCK DIAGRAM**



# PIC16F684

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## 11.3.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

## 11.3.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 3.0 “Oscillator Module (With Fail-Safe Clock Monitor)”** for additional details.

## 11.3.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

## 11.3.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCP1) output driver by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPR1L register and CCP1 bits of the CCP1CON register.
5. Configure and start Timer2:
  - Clear the TMR2IF interrupt flag bit of the PIR1 register.
  - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
  - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
  - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
  - Enable the CCP1 pin output driver by clearing the associated TRIS bit.

## 12.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W\_TEMP and STATUS\_TEMP should be placed in the last 16 bytes of GPR (see Figure 2-2). These 16 locations are common to all banks and do not require banking. This makes context save and restore operations simpler. The code shown in Example 12-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

**Note:** The PIC16F684 does not require saving the PCLATH. However, if computed GOTOS are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

### EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF  W_TEMP           ;Copy W to TEMP register
SWAPF  STATUS,W        ;Swap status to be saved into W
                          ;Swaps are used because they do not affect the status bits
MOVWF  STATUS_TEMP     ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                  ;Insert user code here
:
SWAPF  STATUS_TEMP,W   ;Swap STATUS_TEMP register into W
                          ;(sets bank to original state)
MOVWF  STATUS          ;Move W into STATUS register
SWAPF  W_TEMP,F        ;Swap W_TEMP
SWAPF  W_TEMP,W        ;Swap W_TEMP into W
```

## 14.0 DEVELOPMENT SUPPORT

The PIC<sup>®</sup> microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB<sup>®</sup> IDE Software
- Assemblers/Compilers/Linkers
  - MPASM<sup>™</sup> Assembler
  - MPLAB C18 and MPLAB C30 C Compilers
  - MPLINK<sup>™</sup> Object Linker/  
MPLIB<sup>™</sup> Object Librarian
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB REAL ICE<sup>™</sup> In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PICSTART<sup>®</sup> Plus Development Programmer
  - MPLAB PM3 Device Programmer
  - PICKit<sup>™</sup> 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

## 14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows<sup>®</sup> operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

## 15.5 DC Characteristics: PIC16F684-I (Industrial) PIC16F684-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	V <sub>IL</sub>	<b>Input Low Voltage</b>					
D030		I/O Port: with TTL buffer	V <sub>SS</sub>	—	0.8	V	4.5V ≤ V <sub>DD</sub> ≤ 5.5V
D030A			V <sub>SS</sub>	—	0.15 V <sub>DD</sub>	V	2.0V ≤ V <sub>DD</sub> ≤ 4.5V
D031		with Schmitt Trigger buffer	V <sub>SS</sub>	—	0.2 V <sub>DD</sub>	V	2.0V ≤ V <sub>DD</sub> ≤ 5.5V
D032		MCLR, OSC1 (RC mode) <sup>(1)</sup>	V <sub>SS</sub>	—	0.2 V <sub>DD</sub>	V	
D033		OSC1 (XT and LP modes)	V <sub>SS</sub>	—	0.3	V	
D033A		OSC1 (HS mode)	V <sub>SS</sub>	—	0.3 V <sub>DD</sub>	V	
	V <sub>IH</sub>	<b>Input High Voltage</b>					
D040		I/O ports: with TTL buffer	2.0	—	V <sub>DD</sub>	V	4.5V ≤ V <sub>DD</sub> ≤ 5.5V
D040A			0.25 V <sub>DD</sub> + 0.8	—	V <sub>DD</sub>	V	2.0V ≤ V <sub>DD</sub> ≤ 4.5V
D041		with Schmitt Trigger buffer	0.8 V <sub>DD</sub>	—	V <sub>DD</sub>	V	2.0V ≤ V <sub>DD</sub> ≤ 5.5V
D042		MCLR	0.8 V <sub>DD</sub>	—	V <sub>DD</sub>	V	
D043		OSC1 (XT and LP modes)	1.6	—	V <sub>DD</sub>	V	
D043A		OSC1 (HS mode)	0.7 V <sub>DD</sub>	—	V <sub>DD</sub>	V	
D043B		OSC1 (RC mode)	0.9 V <sub>DD</sub>	—	V <sub>DD</sub>	V	(Note 1)
	I <sub>IL</sub>	<b>Input Leakage Current<sup>(2)</sup></b>					
D060		I/O ports	—	± 0.1	± 1	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , Pin at high-impedance
D061		MCLR <sup>(3)</sup>	—	± 0.1	± 5	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub>
D063		OSC1	—	± 0.1	± 5	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , XT, HS and LP oscillator configuration
D070*	I <sub>PUR</sub>	PORTA Weak Pull-up Current	50	250	400	μA	V <sub>DD</sub> = 5.0V, V <sub>PIN</sub> = V <sub>SS</sub>
	V <sub>OL</sub>	<b>Output Low Voltage<sup>(5)</sup></b>					
D080		I/O ports	—	—	0.6	V	I <sub>OL</sub> = 8.5 mA, V <sub>DD</sub> = 4.5V (Ind.)
	V <sub>OH</sub>	<b>Output High Voltage<sup>(5)</sup></b>					
D090		I/O ports	V <sub>DD</sub> - 0.7	—	—	V	I <sub>OH</sub> = -3.0 mA, V <sub>DD</sub> = 4.5V (Ind.)

\* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

**2:** Negative current is defined as current sourced by the pin.

**3:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**4:** See **Section 10.4.1 "Using the Data EEPROM"** for additional information.

**5:** Including OSC2 in CLKOUT mode.

# PIC16F684

## 15.5 DC Characteristics: PIC16F684-I (Industrial) PIC16F684-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D100	IULP	Ultra Low-Power Wake-Up Current	—	200	—	nA	See Application Note AN879, "Using the Microchip Ultra Low-Power Wake-up Module" (DS00879)
		<b>Capacitive Loading Specs on Output Pins</b>					
D101*	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	Cio	All I/O pins	—	—	50	pF	
		<b>Data EEPROM Memory</b>					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write Cycle Time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh <sup>(4)</sup>	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		<b>Program Flash Memory</b>					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

\* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 4:** See Section 10.4.1 "Using the Data EEPROM" for additional information.
- 5:** Including OSC2 in CLKOUT mode.

## 15.6 Thermal Considerations

Standard Operating Conditions (unless otherwise stated)					
Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$					
Param No.	Sym	Characteristic	Typ	Units	Conditions
TH01	$\theta_{JA}$	Thermal Resistance Junction to Ambient	69.8	C/W	14-pin PDIP package
			85.0	C/W	14-pin SOIC package
			100.4	C/W	14-pin TSSOP package
			46.3	C/W	16-pin QFN 4x0.9mm package
TH02	$\theta_{JC}$	Thermal Resistance Junction to Case	32.5	C/W	14-pin PDIP package
			31.0	C/W	14-pin SOIC package
			31.7	C/W	14-pin TSSOP package
			2.6	C/W	16-pin QFN 4x0.9mm package
TH03	$T_J$	Junction Temperature	150	C	For derated power calculations
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$ <b>(NOTE 1)</b>
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \sum (I_{OL} \times V_{OL}) + \sum (I_{OH} \times (V_{DD} - V_{OH}))$
TH07	$P_{DER}$	Derated Power	—	W	$P_{DER} = (T_J - T_A) / \theta_{JA}$ <b>(NOTE 2, 3)</b>

**Note 1:**  $I_{DD}$  is current to run the chip alone without driving any load on the output pins.

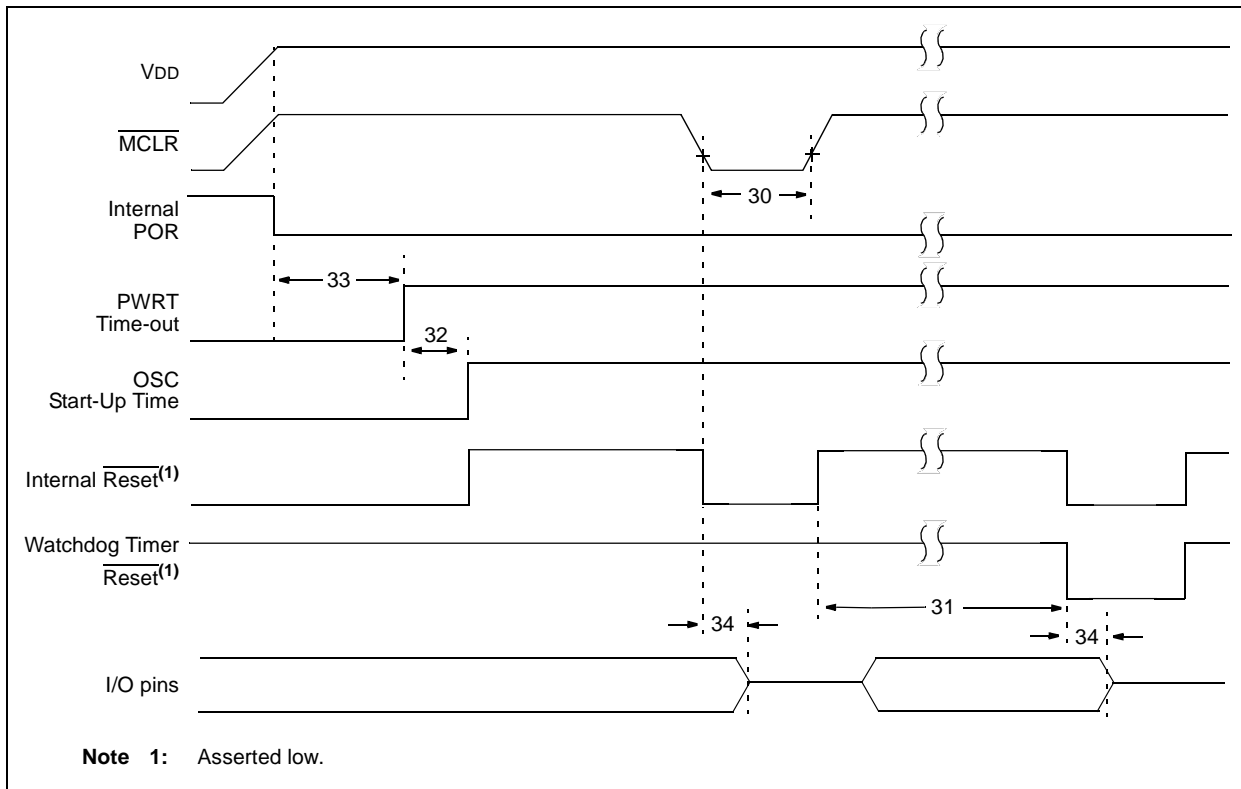
**2:**  $T_A$  = Ambient Temperature.

**3:** Maximum allowable power dissipation is the lower value of either the absolute maximum total power dissipation or derated power ( $P_{DER}$ ).

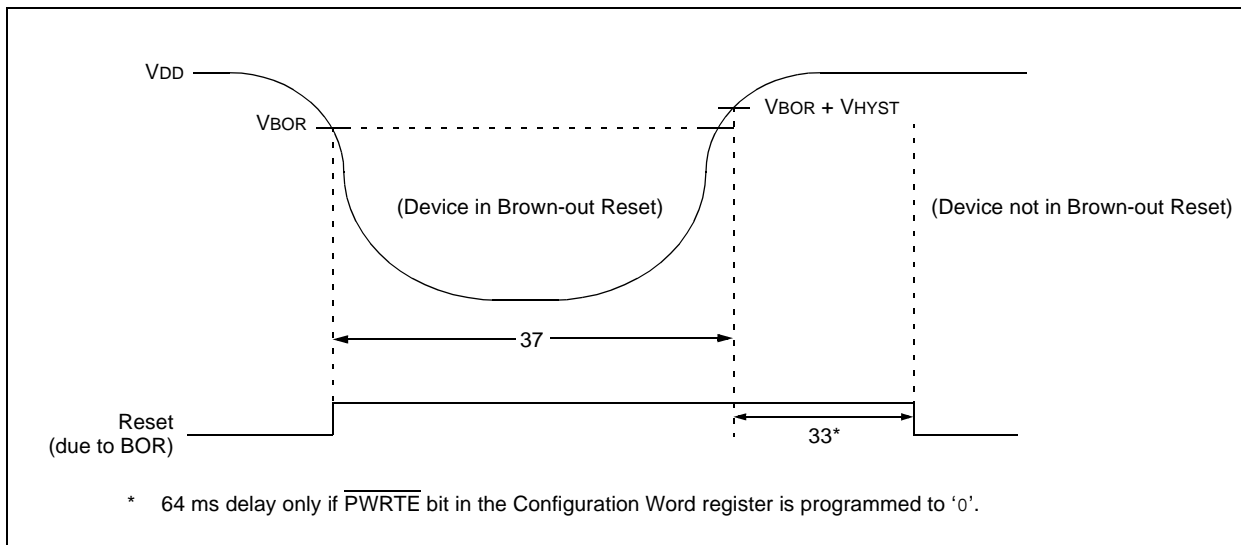


# PIC16F684

**FIGURE 15-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**



**FIGURE 15-7: BROWN-OUT RESET TIMING AND CHARACTERISTICS**



# PIC16F684

FIGURE 16-6: MAXIMUM  $I_{DD}$  vs.  $V_{DD}$  OVER  $F_{osc}$  (XT MODE)

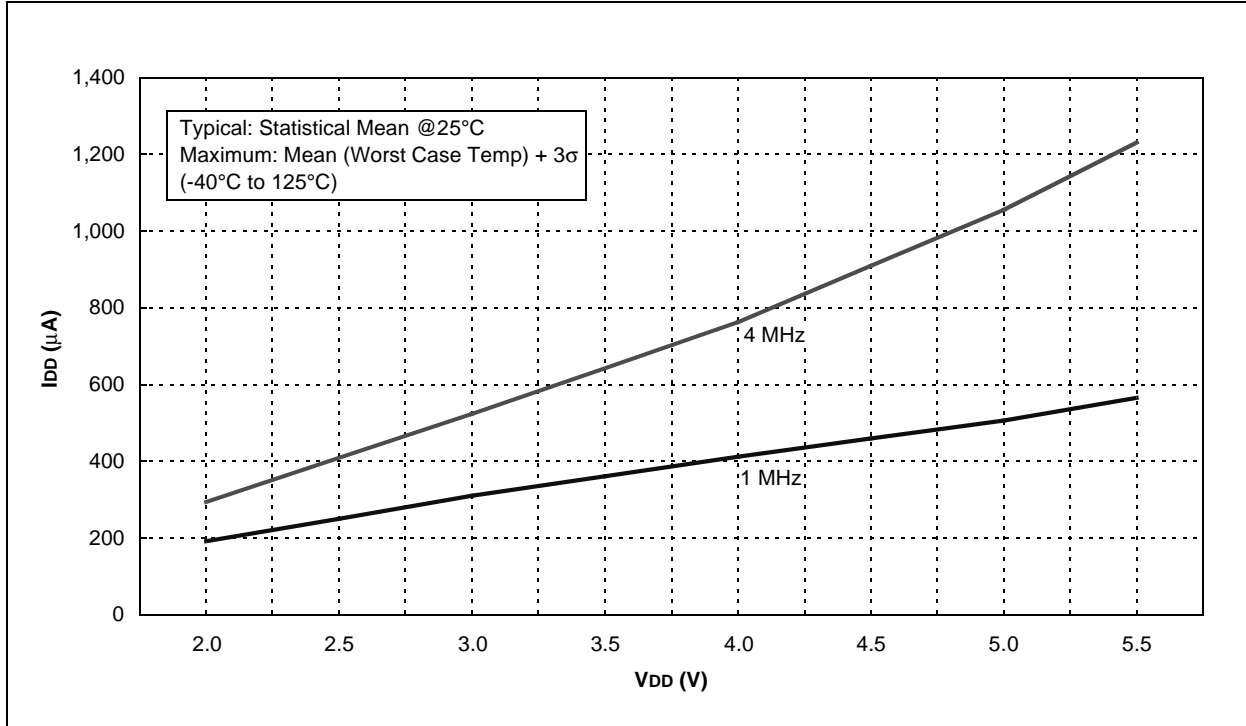
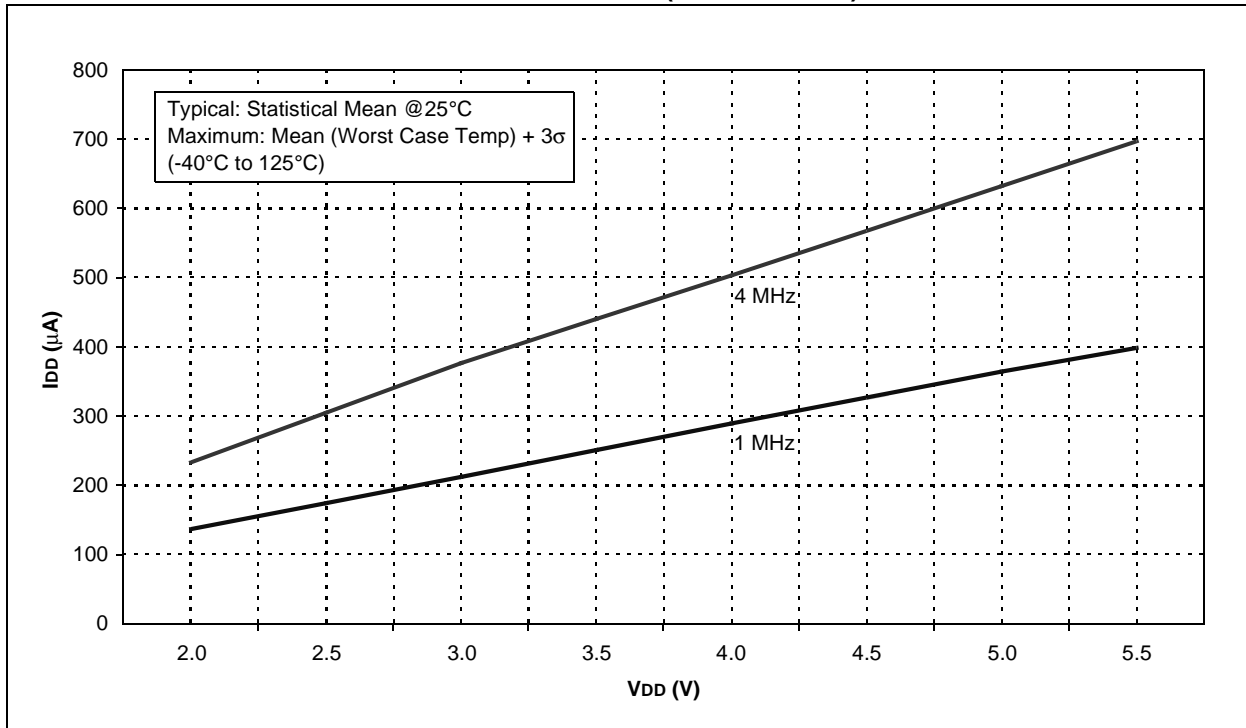
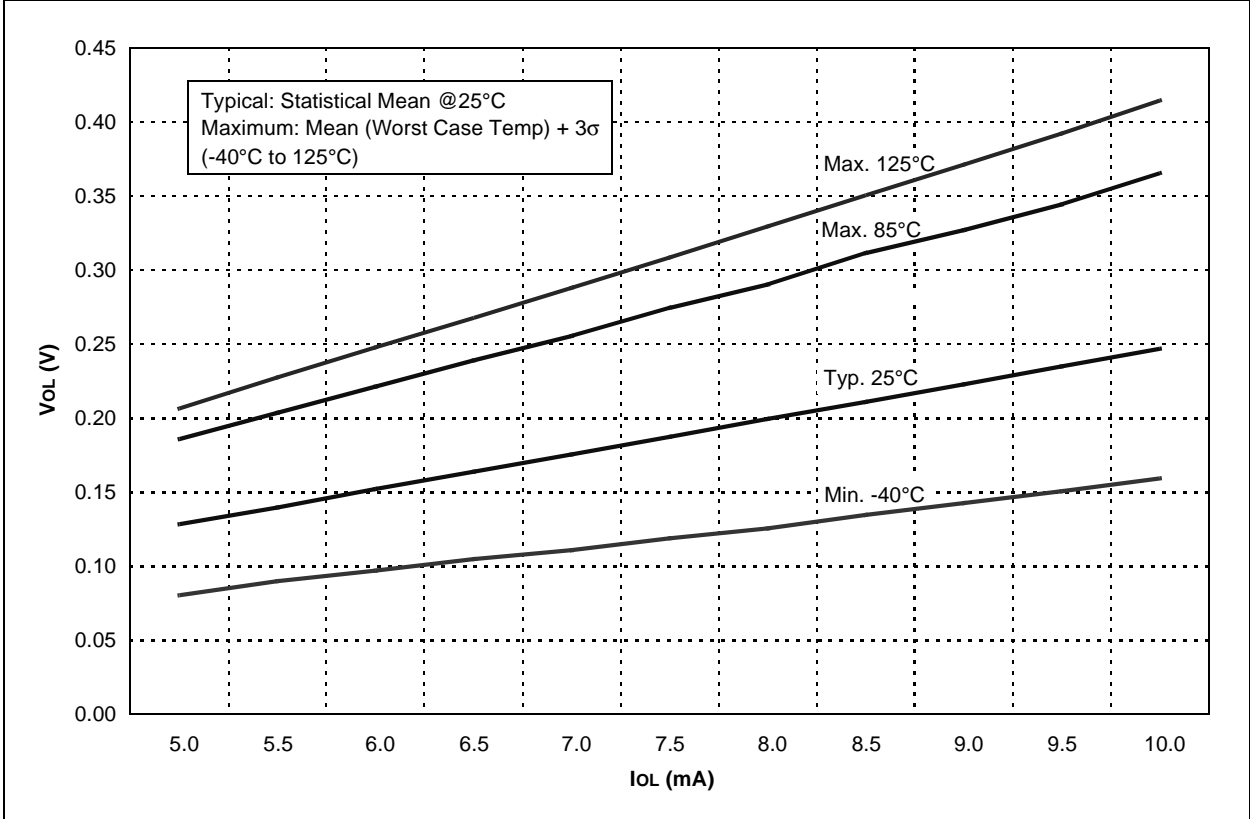


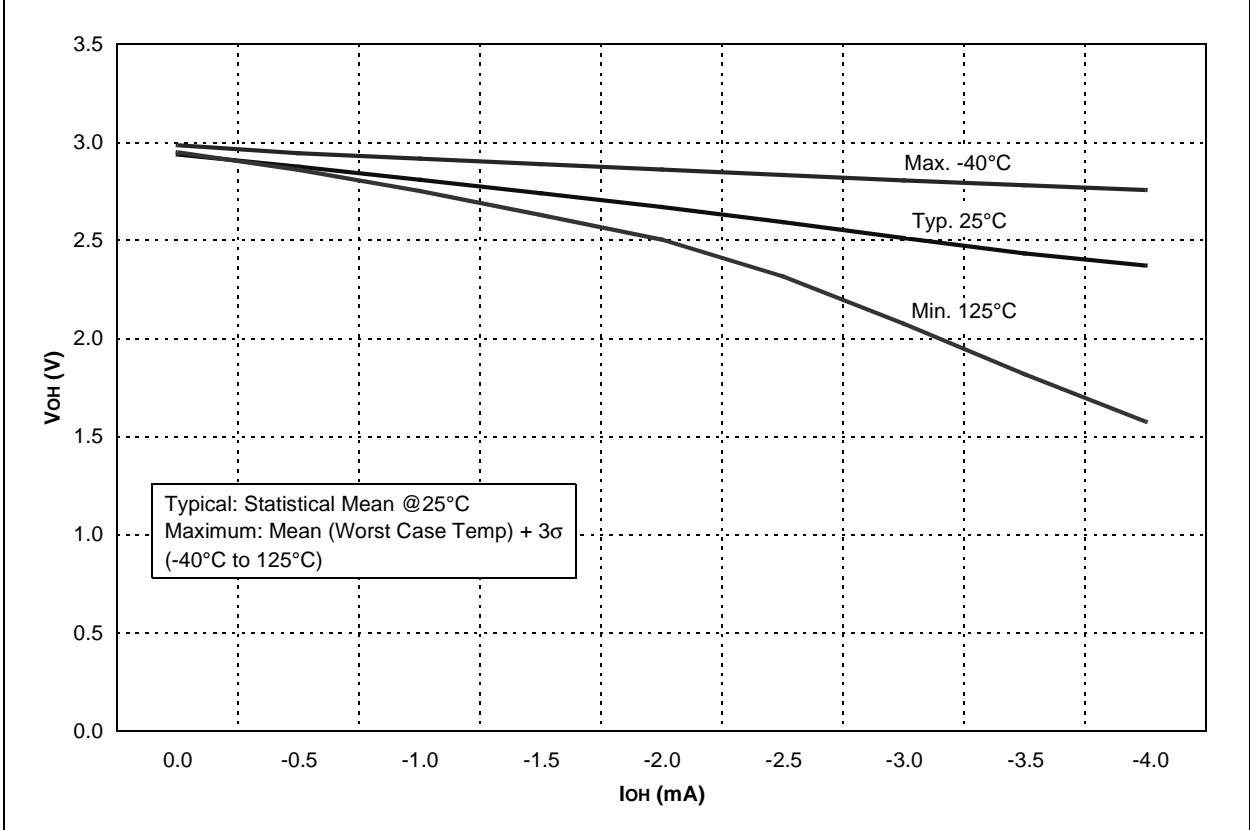
FIGURE 16-7: TYPICAL  $I_{DD}$  vs.  $V_{DD}$  OVER  $F_{osc}$  (EXTRC MODE)



**FIGURE 16-24:  $V_{OL}$  vs.  $I_{OL}$  OVER TEMPERATURE ( $V_{DD} = 5.0V$ )**



**FIGURE 16-25:  $V_{OH}$  vs.  $I_{OH}$  OVER TEMPERATURE ( $V_{DD} = 3.0V$ )**



# PIC16F684

FIGURE 16-34: TYPICAL HFINTOSC START-UP TIMES vs. V<sub>DD</sub> OVER TEMPERATURE

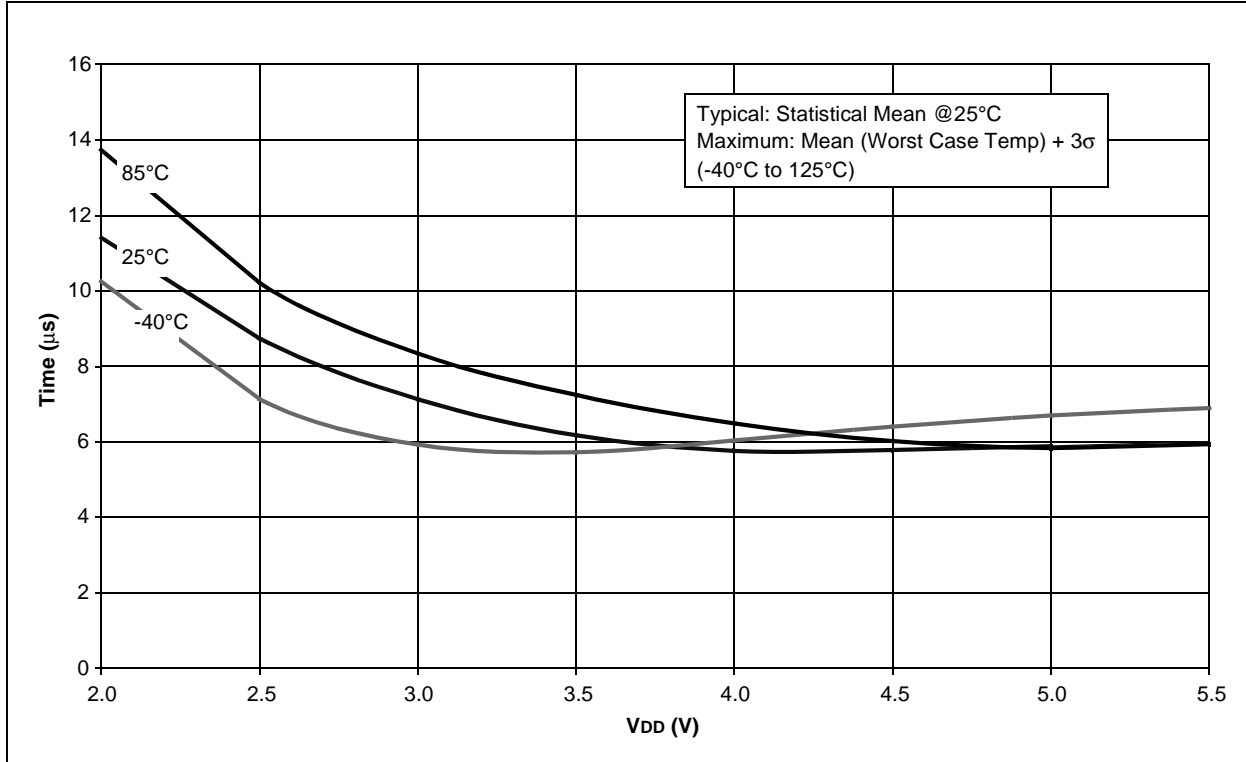
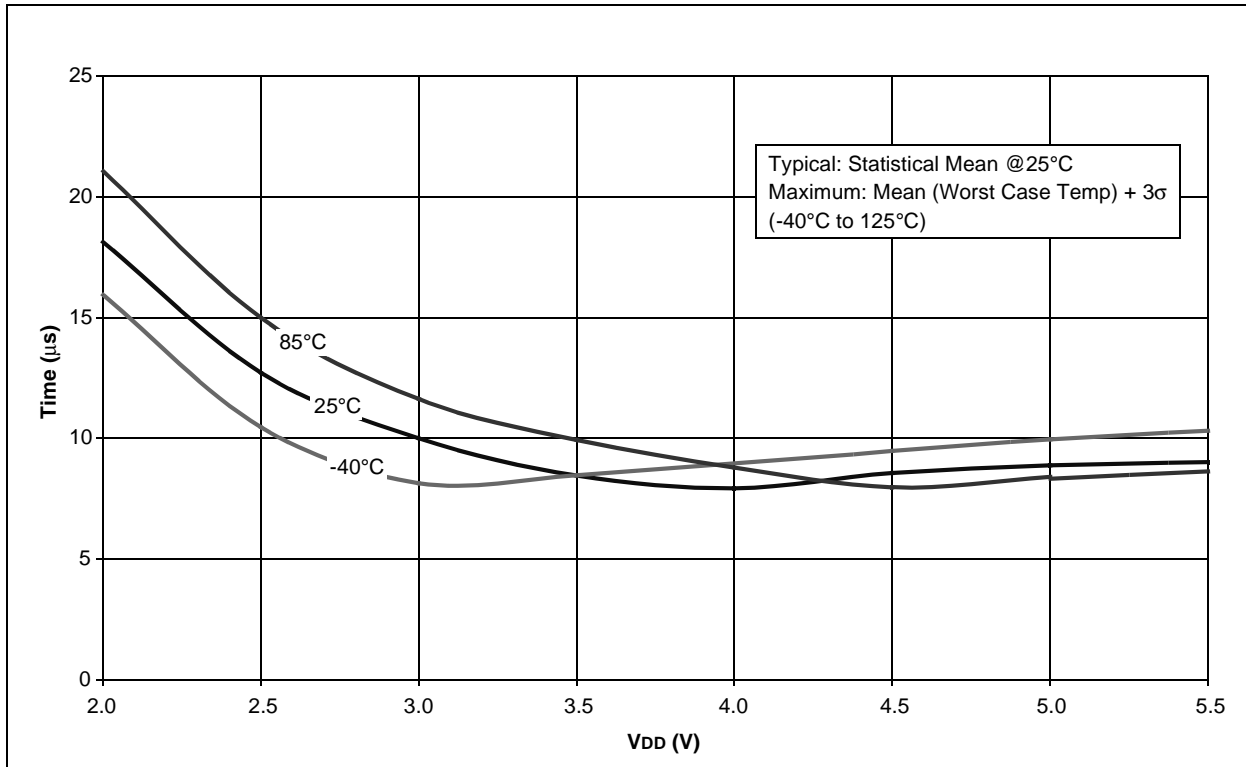


FIGURE 16-35: MAXIMUM HFINTOSC START-UP TIMES vs. V<sub>DD</sub> OVER TEMPERATURE



## APPENDIX A: DATA SHEET REVISION HISTORY

### Revision A

This is a new data sheet.

### Revision B

Rewrites of the Oscillator and Special Features of the CPU Sections. General corrections to Figures and formatting.

### Revision C

### Revision D

Added Characterization Data. Updated Electrical Specifications. Incorporated Golden Chapter Sections for the following:

- Section 3.0 “Oscillator Module (With Fail-Safe Clock Monitor)”
- Section 5.0 “Timer0 Module”
- Section 6.0 “Timer1 Module with Gate Control”
- Section 7.0 “Timer2 Module”
- Section 8.0 “Comparator Module”
- Section 9.0 “Analog-to-Digital Converter (ADC) Module”
- Section 11.0 “Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module”

### Revision E

Updated Package Drawings; Replace PICmicro with PIC.

### Revision F (03/2007)

Replaced Package Drawings (Rev. AM); Replaced Development Support Section.

## APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC devices to the PIC16F6XX Family of devices.

### B.1 PIC16F676 to PIC16F684

**TABLE B-1: FEATURE COMPARISON**

Feature	PIC16F676	PIC16F684
Max Operating Speed	20 MHz	20 MHz
Max Program Memory (Words)	1024	2048
SRAM (bytes)	64	128
A/D Resolution	10-bit	10-bit
Data EEPROM (Bytes)	128	256
Timers (8/16-bit)	1/1	2/1
Oscillator Modes	8	8
Brown-out Reset	Y	Y
Internal Pull-ups	RA0/1/2/4/5	RA0/1/2/4/5, MCLR
Interrupt-on-change	RA0/1/2/3/4/5	RA0/1/2/3/4/5
Comparator	1	2
ECCP	N	Y
Ultra Low-Power Wake-Up	N	Y
Extended WDT	N	Y
Software Control Option of WDT/BOR	N	Y
INTOSC Frequencies	4 MHz	32 kHz- 8 MHz
Clock Switching	N	Y

**Note:** This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.