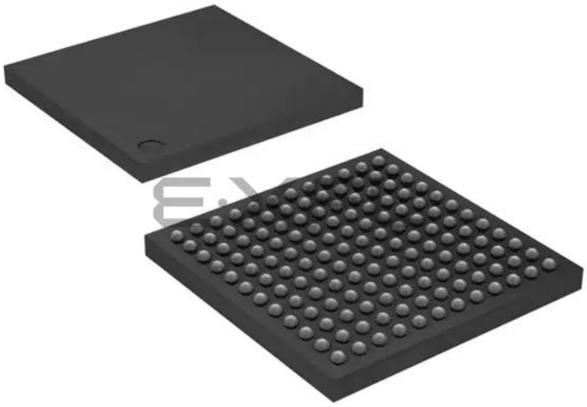
Microchip Technology - AT32UC3A0256-CTUR Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, SSC, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	109
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-FFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3a0256-ctur

1. Description

The AT32UC3A is a complete System-On-Chip microcontroller based on the AVR32 UC RISC processor running at frequencies up to 66 MHz. AVR32 UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high performance.

The processor implements a Memory Protection Unit (MPU) and a fast and flexible interrupt controller for supporting modern operating systems and real-time operating systems. Higher computation capabilities are achievable using a rich set of DSP instructions.

The AT32UC3A incorporates on-chip Flash and SRAM memories for secure and fast access. For applications requiring additional memory, an external memory interface is provided on AT32UC3A0 derivatives.

The Peripheral Direct Memory Access controller (PDCA) enables data transfers between peripherals and memories without processor involvement. PDCA drastically reduces processing overhead when transferring continuous and large data streams between modules within the MCU.

The PowerManager improves design flexibility and security: the on-chip Brown-Out Detector monitors the power supply, the CPU runs from the on-chip RC oscillator or from one of external oscillator sources, a Real-Time Clock and its associated timer keeps track of the time.

The Timer/Counter includes three identical 16-bit timer/counter channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

The PWM modules provides seven independent channels with many configuration options including polarity, edge alignment and waveform non overlap control. One PWM channel can trigger ADC conversions for more accurate close loop control implementations.

The AT32UC3A also features many communication interfaces for communication intensive applications. In addition to standard serial interfaces like UART, SPI or TWI, other interfaces like flexible Synchronous Serial Controller, USB and Ethernet MAC are available.

The Synchronous Serial Controller provides easy access to serial communication protocols and audio standards like I2S.

The Full-Speed USB 2.0 Device interface supports several USB Classes at the same time thanks to the rich End-Point configuration. The On-The-GO (OTG) Host interface allows device like a USB Flash disk or a USB printer to be directly connected to the processor.

The media-independent interface (MII) and reduced MII (RMII) 10/100 Ethernet MAC module provides on-chip solutions for network-connected devices.

AT32UC3A integrates a class 2+ Nexus 2.0 On-Chip Debug (OCD) System, with non-intrusive real-time trace, full-speed read/write memory access in addition to basic runtime control.

2. Configuration Summary

The table below lists all AT32UC3A memory and package configurations:

Device	Flash	SRAM	Ext. Bus Interface	Ethernet MAC	Package
AT32UC3A0512	512 Kbytes	64 Kbytes	yes	yes	144 pin LQFP 144 pin BGA
AT32UC3A0256	256 Kbytes	64 Kbytes	yes	yes	144 pin LQFP 144 pin BGA
AT32UC3A0128	128 Kbytes	32 Kbytes	yes	yes	144 pin LQFP 144 pin BGA
AT32UC3A1512	512 Kbytes	64 Kbytes	no	yes	100 pin TQFP
AT32UC3A1256	256 Kbytes	64 Kbytes	no	yes	100 pin TQFP
AT32UC3A1128	128 Kbytes	32 Kbytes	no	yes	100 pin TQFP

3. Abbreviations

- GCLK: Power Manager Generic Clock
- GPIO: General Purpose Input/Output
- HSB: High Speed Bus
- MPU: Memory Protection Unit
- OCD: On Chip Debug
- PB: Peripheral Bus
- PDCA: Peripheral Direct Memory Access Controller (PDC) version A
- USBB: USB On-The-GO Controller version B

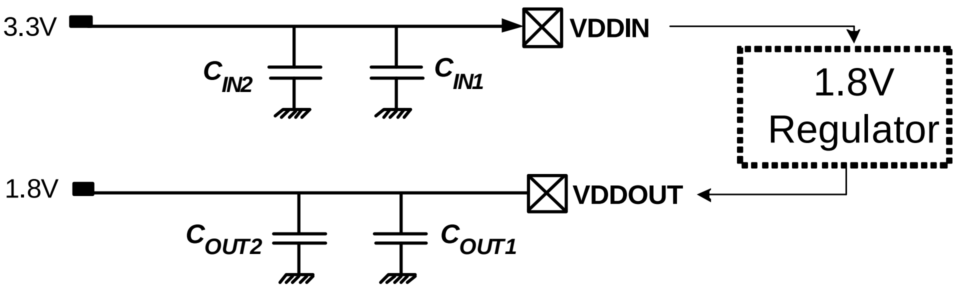
7.2 Voltage Regulator

7.2.1 Single Power Supply

The AT32UC3A embeds a voltage regulator that converts from 3.3V to 1.8V. The regulator takes its input voltage from VDDIN, and supplies the output voltage on VDDOUT. VDDOUT should be externally connected to the 1.8V domains.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. Two input decoupling capacitors must be placed close to the chip.

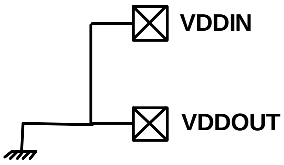
Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel between VDDOUT and GND as close to the chip as possible



Refer to Section 12.3 on page 42 for decoupling capacitors values and regulator characteristics

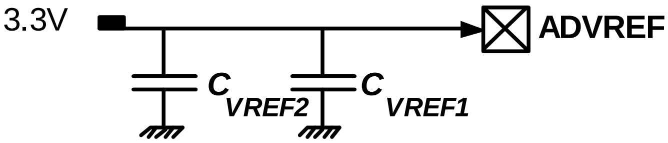
7.2.2 Dual Power Supply

In case of dual power supply, VDDIN and VDDOUT should be connected to ground to prevent from leakage current.



7.3 Analog-to-Digital Converter (A.D.C) reference.

The ADC reference (ADVREF) must be provided from an external source. Two decoupling capacitors must be used to insure proper decoupling.



Refer to Section 12.4 on page 42 for decoupling capacitors values and electrical characteristics.

In case ADC is not used, the ADVREF pin should be connected to GND to avoid extra consumption.

Table 9-2. Flash Memory Parameters

Part Number	Flash Size (*FLASH_PW*)	Number of pages (*FLASH_P*)	Page size (*FLASH_W*)	General Purpose Fuse bits (*FLASH_F*)
AT32UC3A0512	512 Kbytes	1024	128 words	32 fuses
AT32UC3A1512	512 Kbytes	1024	128 words	32 fuses
AT32UC3A0256	256 Kbytes	512	128 words	32 fuses
AT32UC3A1256	256 Kbytes	512	128 words	32 fuses
AT32UC3A1128	128 Kbytes	256	128 words	32 fuses
AT32UC3A0128	128 Kbytes	256	128 words	32 fuses

9.3 Bus Matrix Connections

Accesses to unused areas returns an error result to the master requesting such an access.

The bus matrix has the several masters and slaves. Each master has its own bus and its own decoder, thus allowing a different memory mapping per master. The master number in the table below can be used to index the HMATRIX control registers. For example, MCFG0 is associated with the CPU Data master interface.

Table 9-3. High Speed Bus masters

Master 0	CPU Data
Master 1	CPU Instruction
Master 2	CPU SAB
Master 3	PDCA
Master 4	MACB DMA
Master 5	USBB DMA

Each slave has its own arbiter, thus allowing a different arbitration per slave. The slave number in the table below can be used to index the HMATRIX control registers. For example, SCFG3 is associated with the Internal SRAM Slave Interface.

Table 9-4. High Speed Bus slaves

Slave 0	Internal Flash
Slave 1	HSB-PB Bridge 0
Slave 2	HSB-PB Bridge 1
Slave 3	Internal SRAM
Slave 4	USBB DPRAM
Slave 5	EBI

10.4.3 SPIs

Each SPI can be connected to an internally divided clock:

Table 10-6. SPI clock connections

SPI	Source	Name	Connection
0	Internal	CLK_DIV	PBA clock or PBA clock / 32
1			

10.5 Nexus OCD AUX port connections

If the OCD trace system is enabled, the trace system will take control over a number of pins, irrespectively of the PIO configuration. Two different OCD trace pin mappings are possible, depending on the configuration of the OCD AXS register. For details, see the AVR32 UC Technical Reference Manual.

Table 10-7. Nexus OCD AUX port connections

Pin	AXS=0	AXS=1
EVTI_N	PB19	PA08
MDO[5]	PB16	PA27
MDO[4]	PB14	PA26
MDO[3]	PB13	PA25
MDO[2]	PB12	PA24
MDO[1]	PB11	PA23
MDO[0]	PB10	PA22
EVTO_N	PB20	PB20
MCKO	PB21	PA21
MSEO[1]	PB04	PA07
MSEO[0]	PB17	PA28

10.6 PDC handshake signals

The PDC and the peripheral modules communicate through a set of handshake signals. The following table defines the valid settings for the Peripheral Identifier (PID) in the PDC Peripheral Select Register (PSR).

Table 10-8. PDC Handshake Signals

PID Value	Peripheral module & direction
0	ADC
1	SSC - RX
2	USART0 - RX
3	USART1 - RX

Table 10-9. GPIO Controller Function Multiplexing

41	58	PA16	GPIO 16	SSC - TX_DATA	SPI1 - MOSI	EBI - ADDR[21]
42	60	PA17	GPIO 17	SSC - RX_DATA	SPI1 - MISO	EBI - ADDR[22]
43	62	PA18	GPIO 18	SSC - RX_CLOCK	SPI1 - NPCS[1]	MACB - WOL
44	64	PA19	GPIO 19	SSC - RX_FRAME_SYNC	SPI1 - NPCS[2]	
45	66	PA20	GPIO 20	EIM - EXTINT[8]	SPI1 - NPCS[3]	
51	73	PA21	GPIO 21	ADC - AD[0]	EIM - EXTINT[0]	USB - USB_ID
52	74	PA22	GPIO 22	ADC - AD[1]	EIM - EXTINT[1]	USB - USB_VBOF
53	75	PA23	GPIO 23	ADC - AD[2]	EIM - EXTINT[2]	DAC - DATA[1]
54	76	PA24	GPIO 24	ADC - AD[3]	EIM - EXTINT[3]	DAC - DATAN[1]
55	77	PA25	GPIO 25	ADC - AD[4]	EIM - SCAN[0]	EBI - NCS[0]
56	78	PA26	GPIO 26	ADC - AD[5]	EIM - SCAN[1]	EBI - ADDR[20]
57	79	PA27	GPIO 27	ADC - AD[6]	EIM - SCAN[2]	EBI - ADDR[21]
58	80	PA28	GPIO 28	ADC - AD[7]	EIM - SCAN[3]	EBI - ADDR[22]
83	122	PA29	GPIO 29	TWI - SDA	USART2 - RTS	
84	123	PA30	GPIO 30	TWI - SCL	USART2 - CTS	
65	88	PB00	GPIO 32	MACB - TX_CLK	USART2 - RTS	USART3 - RTS
66	90	PB01	GPIO 33	MACB - TX_EN	USART2 - CTS	USART3 - CTS
70	96	PB02	GPIO 34	MACB - TXD[0]	DAC - DATA[0]	
71	98	PB03	GPIO 35	MACB - TXD[1]	DAC - DATAN[0]	
72	100	PB04	GPIO 36	MACB - CRS	USART3 - CLK	EBI - NCS[3]
73	102	PB05	GPIO 37	MACB - RXD[0]	DAC - DATA[1]	
74	104	PB06	GPIO 38	MACB - RXD[1]	DAC - DATAN[1]	
75	106	PB07	GPIO 39	MACB - RX_ER		
76	111	PB08	GPIO 40	MACB - MDC		
77	113	PB09	GPIO 41	MACB - MDIO		
78	115	PB10	GPIO 42	MACB - TXD[2]	USART3 - RXD	EBI - SDCK
81	119	PB11	GPIO 43	MACB - TXD[3]	USART3 - TXD	EBI - SDCKE
82	121	PB12	GPIO 44	MACB - TX_ER	TC - CLK0	EBI - RAS
87	126	PB13	GPIO 45	MACB - RXD[2]	TC - CLK1	EBI - CAS
88	127	PB14	GPIO 46	MACB - RXD[3]	TC - CLK2	EBI - SDWE
95	134	PB15	GPIO 47	MACB - RX_DV		
96	136	PB16	GPIO 48	MACB - COL	USB - USB_ID	EBI - SDA10
98	139	PB17	GPIO 49	MACB - RX_CLK	USB - USB_VBOF	EBI - ADDR[23]
99	141	PB18	GPIO 50	MACB - SPEED	ADC - TRIGGER	PWM - PWM[6]
100	143	PB19	GPIO 51	PWM - PWM[0]	PM - GCLK[0]	EIM - SCAN[4]
1	3	PB20	GPIO 52	PWM - PWM[1]	PM - GCLK[1]	EIM - SCAN[5]
2	5	PB21	GPIO 53	PWM - PWM[2]	PM - GCLK[2]	EIM - SCAN[6]
3	6	PB22	GPIO 54	PWM - PWM[3]	PM - GCLK[3]	EIM - SCAN[7]
6	9	PB23	GPIO 55	TC - A0	USART1 - DCD	

12. Electrical Characteristics

12.1 Absolute Maximum Ratings*

Operating Temperature	-40·C to +85·C
Storage Temperature	-60°C to +150°C
Voltage on Input Pin with respect to Ground except for PC00, PC01, PC02, PC03, PC04, PC05	-0.3V to 5.5V
Voltage on Input Pin with respect to Ground for PC00, PC01, PC02, PC03, PC04, PC05	-0.3V to 3.6V
Maximum Operating Voltage (VDDCORE, VDDPLL)	1.95V
Maximum Operating Voltage (VDDIO, VDDIN, VDDANA)	3.6V
Total DC Output Current on all I/O Pin for TQFP100 package	370 mA
for LQGP144 package	470 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 12-24. SMC Read Signals with no Hold Settings

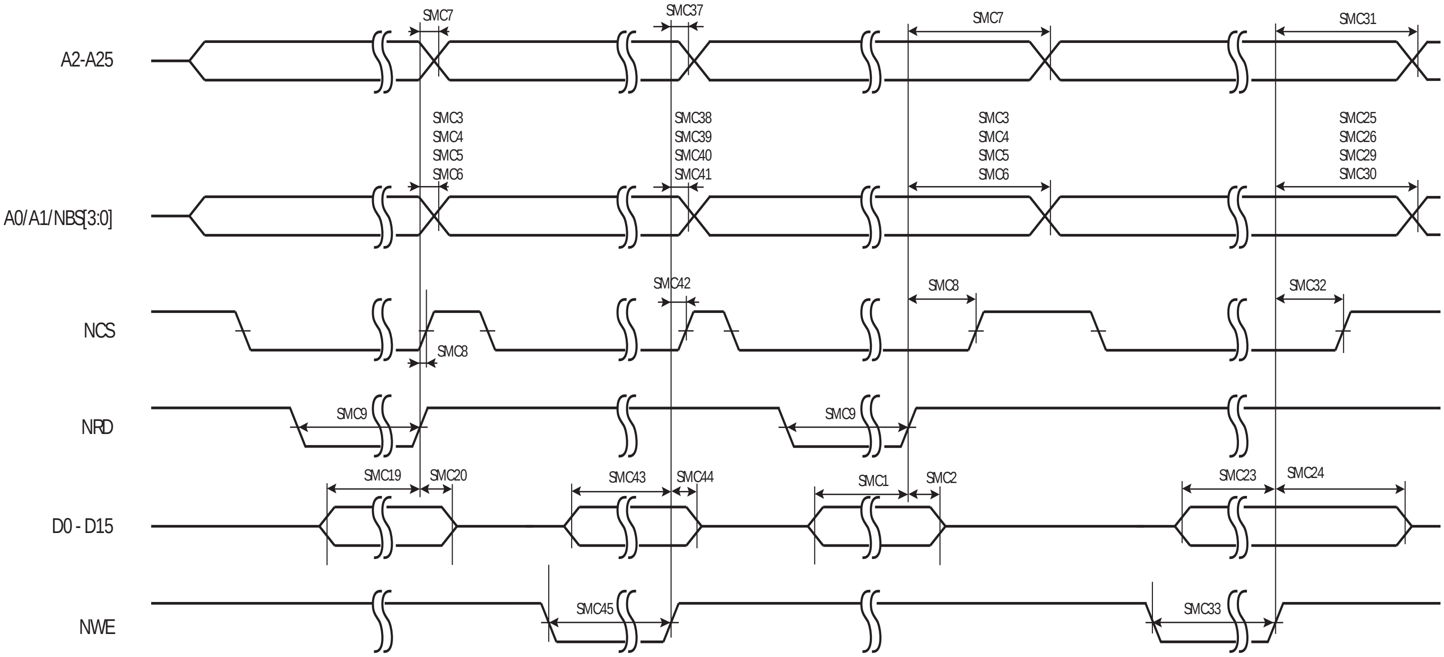
Symbol	Parameter	Min	Units
		NRD Controlled (READ_MODE = 1)	
SMC_{19}	Data Setup before NRD High	13.7	ns
SMC_{20}	Data Hold after NRD High	1	
		NRD Controlled (READ_MODE = 0)	
SMC_{21}	Data Setup before NCS High	13.3	ns
SMC_{22}	Data Hold after NCS High	0	

Table 12-25. SMC Write Signals with Hold Settings

Symbol	Parameter	Min	Units
		NRD Controlled (READ_MODE = 1)	
SMC_{23}	Data Out Valid before NWE High	(nwe pulse length - 1) * t_{CPSMC} - 0.9	ns
SMC_{24}	Data Out Valid after NWE High[1]	nwe hold length * t_{CPSMC} - 6	
SMC_{25}	NWE High to NBS0/A0 Change[1]	nwe hold length * t_{CPSMC} - 1.9	
SMC_{26}	NWE High to NBS1 Change[1]	nwe hold length * t_{CPSMC} - 1.9	
SMC_{29}	NWE High to NBS2/A1 Change[1]	nwe hold length * t_{CPSMC} - 1.9	
SMC_{30}	NWE High to NBS3 Change[1]	nwe hold length * t_{CPSMC} - 1.9	
SMC_{31}	NWE High to A2 - A25 Change[1]	nwe hold length * t_{CPSMC} - 1.7	
SMC_{32}	NWE High to NCS Inactive[1]	(nwe hold length - ncs wr hold length)* t_{CPSMC} - 2.9	
SMC_{33}	NWE Pulse Width	nwe pulse length * t_{CPSMC} - 0.9	
		NRD Controlled (READ_MODE = 0)	
SMC_{34}	Data Out Valid before NCS High	(ncs wr pulse length - 1)* t_{CPSMC} - 4.6	ns
SMC_{35}	Data Out Valid after NCS High[1]	ncs wr hold length * t_{CPSMC} - 5.8	
SMC_{36}	NCS High to NWE Inactive[1]	(ncs wr hold length - nwe hold length)* t_{CPSMC} - 0.6	

Note: 1. hold length = total cycle duration - setup duration - pulse duration. “hold length” is for “ncs wr hold length” or “nwe hold length"

Figure 12-3. SMC Signals for NRD and NRW Controlled Accesses.



12.9.1 SDRAM Signals

These timings are given for 10 pF load on SDCK and 40 pF on other signals.

Table 12-27. SDRAM Clock Signal.

Symbol	Parameter	Max[1]	Units
1/(t_{CPSDCK})	SDRAM Controller Clock Frequency	1/(t_{cpcpu})	MHz

Note: 1. The maximum frequency of the SDRAMC interface is the same as the max frequency for the HSB.

Table 12-28. SDRAM Clock Signal.

Symbol	Parameter	Min	Units
$SDRAMC_1$	SDCKE High before SDCK Rising Edge	7.4	ns
$SDRAMC_2$	SDCKE Low after SDCK Rising Edge	3.2	
$SDRAMC_3$	SDCKE Low before SDCK Rising Edge	7	
$SDRAMC_4$	SDCKE High after SDCK Rising Edge	2.9	
$SDRAMC_5$	SDCS Low before SDCK Rising Edge	7.5	
$SDRAMC_6$	SDCS High after SDCK Rising Edge	1.6	
$SDRAMC_7$	RAS Low before SDCK Rising Edge	7.2	
$SDRAMC_8$	RAS High after SDCK Rising Edge	2.3	
$SDRAMC_9$	SDA10 Change before SDCK Rising Edge	7.6	
$SDRAMC_{10}$	SDA10 Change after SDCK Rising Edge	1.9	

Table 12-28. SDRAM Clock Signal.

Symbol	Parameter	Min	Units
$SDRAMC_{11}$	Address Change before SDCK Rising Edge	6.2	ns
$SDRAMC_{12}$	Address Change after SDCK Rising Edge	2.2	
$SDRAMC_{13}$	Bank Change before SDCK Rising Edge	6.3	
$SDRAMC_{14}$	Bank Change after SDCK Rising Edge	2.4	
$SDRAMC_{15}$	CAS Low before SDCK Rising Edge	7.4	
$SDRAMC_{16}$	CAS High after SDCK Rising Edge	1.9	
$SDRAMC_{17}$	DQM Change before SDCK Rising Edge	6.4	
$SDRAMC_{18}$	DQM Change after SDCK Rising Edge	2.2	
$SDRAMC_{19}$	D0-D15 in Setup before SDCK Rising Edge	9	
$SDRAMC_{20}$	D0-D15 in Hold after SDCK Rising Edge	0	
$SDRAMC_{23}$	SDWE Low before SDCK Rising Edge	7.6	
$SDRAMC_{24}$	SDWE High after SDCK Rising Edge	1.8	
$SDRAMC_{25}$	D0-D15 Out Valid before SDCK Rising Edge	7.1	
$SDRAMC_{26}$	D0-D15 Out Valid after SDCK Rising Edge	1.5	

Figure 12-7. SPI Master mode with (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)

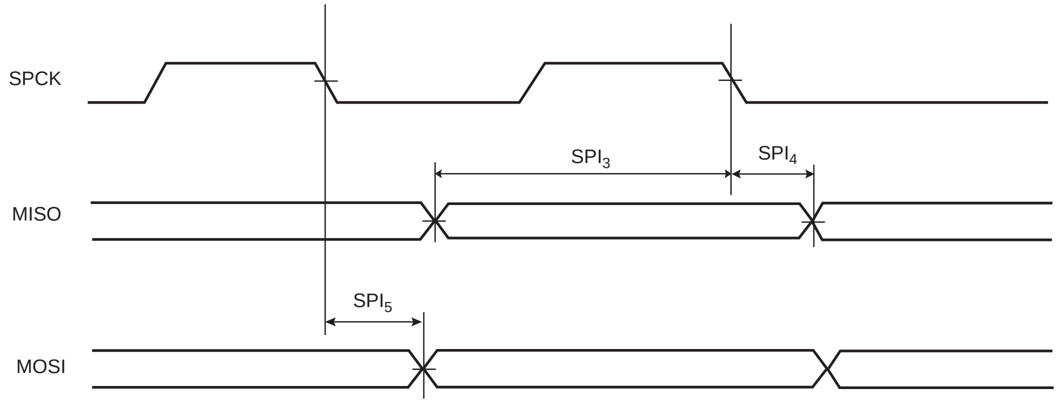


Figure 12-8. SPI Slave mode with (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)

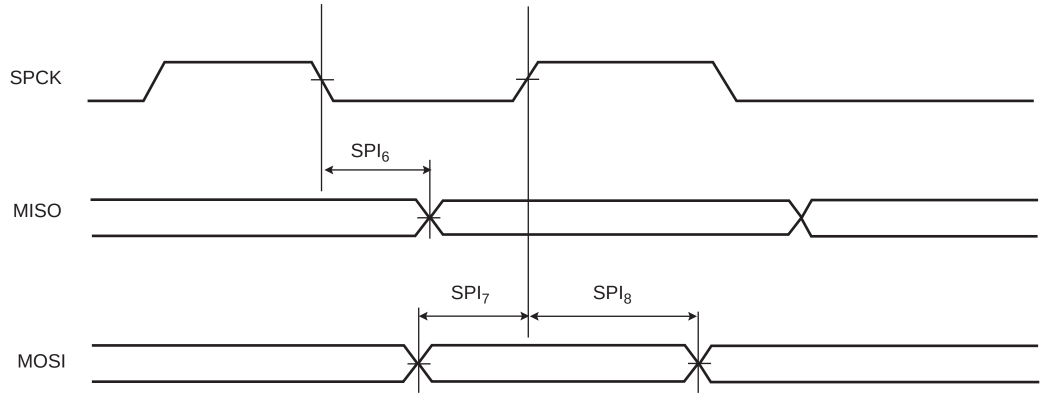


Figure 12-9. SPI Slave mode with (CPOL = NCPHA = 0) or (CPOL= NCPHA= 1)

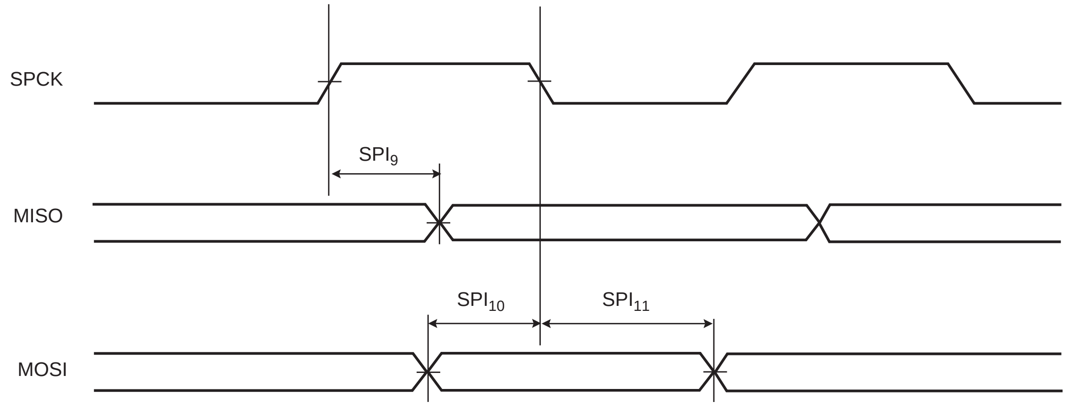


Table 12-30. SPI Timings

Symbol	Parameter	Conditions	Min	Max	Units
SPI_0	MISO Setup time before SPCK rises (master)	3.3V domain[1]	22 + (t_{CPMCK})/2[2]		ns
SPI_1	MISO Hold time after SPCK rises (master)	3.3V domain[1]	0		ns
SPI_2	SPCK rising to MOSI Delay (master)	3.3V domain[1]		7	ns
SPI_3	MISO Setup time before SPCK falls (master)	3.3V domain[1]	22 + (t_{CPMCK})/2[2]		ns
SPI_4	MISO Hold time after SPCK falls (master)	3.3V domain [1]	0		ns
SPI_5	SPCK falling to MOSI Delay (master)	3.3V domain [1]		7	ns
SPI_6	SPCK falling to MISO Delay (slave)	3.3V domain [1]		26.5	ns
SPI_7	MOSI Setup time before SPCK rises (slave)	3.3V domain [1]	0		ns
SPI_8	MOSI Hold time after SPCK rises (slave)	3.3V domain [1]	1.5		ns
SPI_9	SPCK rising to MISO Delay (slave)	3.3V domain [1]		27	ns
SPI_{10}	MOSI Setup time before SPCK falls (slave)	3.3V domain [1]	0		ns
SPI_{11}	MOSI Hold time after SPCK falls (slave)	3.3V domain [1]	1		ns

Notes: 1. 3.3V domain: V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40 pF.

2. t_{CPMCK}: Master Clock period in ns.

12.12 MACB Characteristics

Table 12-31. Ethernet MAC Signals

Symbol	Parameter	Conditions	Min (ns)	Max (ns)
$EMAC_1$	Setup for EMDIO from EMDC rising	Load: 20pF[2]		
$EMAC_2$	Hold for EMDIO from EMDC rising	Load: 20pF[2]		
$EMAC_3$	EMDIO toggling from EMDC falling	Load: 20pF[2]		

Notes: 1. f: MCK frequency (MHz)

2. V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 20 pF

Table 12-32. Ethernet MAC MII Specific Signals

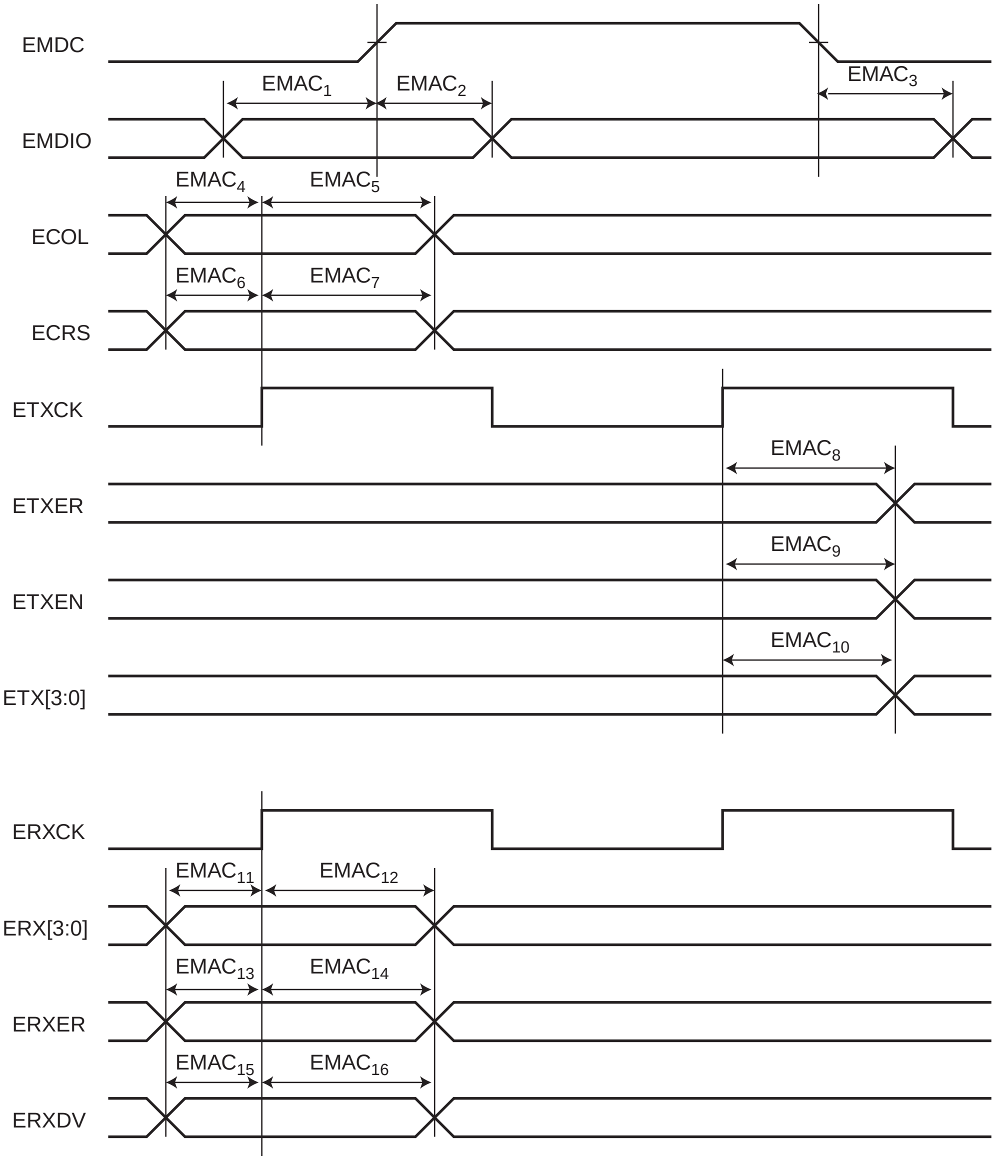
Symbol	Parameter	Conditions	Min (ns)	Max (ns)
$EMAC_4$	Setup for ECOL from ETXCK rising	Load: 20pF [1]	3	
$EMAC_5$	Hold for ECOL from ETXCK rising	Load: 20pF [1]	0	
$EMAC_6$	Setup for ECRS from ETXCK rising	Load: 20pF [1]	3	
$EMAC_7$	Hold for ECRS from ETXCK rising	Load: 20pF [1]	0	
$EMAC_8$	ETXER toggling from ETXCK rising	Load: 20pF [1]		15
$EMAC_9$	ETXEN toggling from ETXCK rising	Load: 20pF [1]		15
$EMAC_{10}$	ETX toggling from ETXCK rising	Load: 20pF [1]		15
$EMAC_{11}$	Setup for ERX from ERXCK	Load: 20pF [1]	1	

Table 12-32. Ethernet MAC MII Specific Signals

Symbol	Parameter	Conditions	Min (ns)	Max (ns)
$EMAC_{12}$	Hold for ERX from ERXCK	Load: 20pF [(1)]	1.5	
$EMAC_{13}$	Setup for ERXER from ERXCK	Load: 20pF [(1)]	1	
$EMAC_{14}$	Hold for ERXER from ERXCK	Load: 20pF [(1)]	0.5	
$EMAC_{15}$	Setup for ERXDV from ERXCK	Load: 20pF [(1)]	1.5	
$EMAC_{16}$	Hold for ERXDV from ERXCK	Load: 20pF [(1)]	1	

Note: 1. V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 20 pF

Figure 12-10. Ethernet MAC MII Mode



13. Mechanical Characteristics

13.1 Thermal Considerations

13.1.1 Thermal Data

Table 13-1 summarizes the thermal resistance data depending on the package.

Table 13-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP100	43.4	·C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP100	5.5	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	LQFP144	39.8	·C/W
θ_{JC}	Junction-to-case thermal resistance		LQFP144	8.9	

13.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

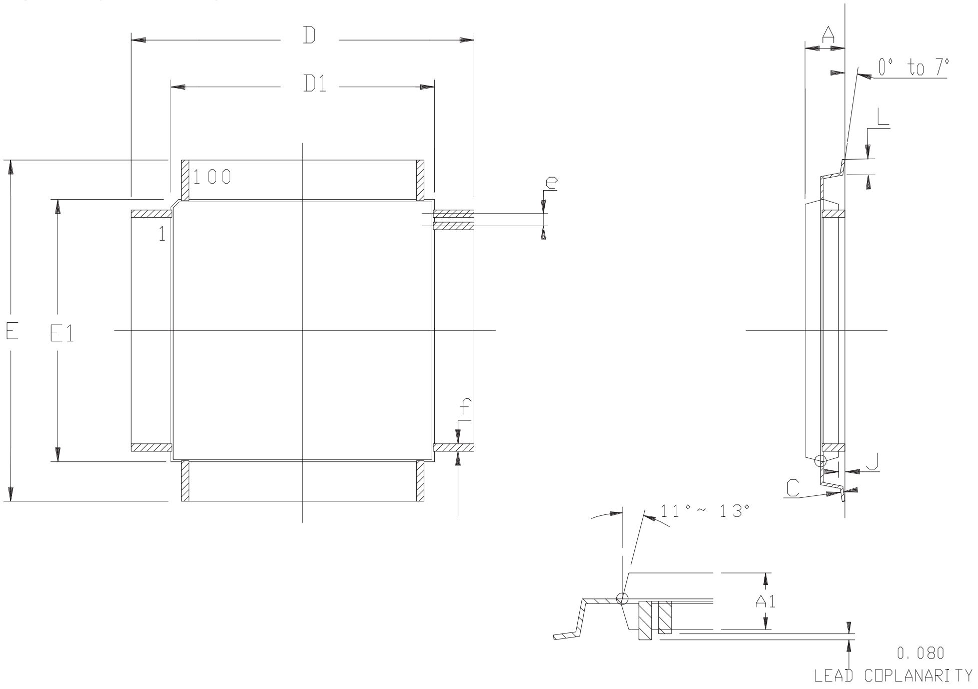
where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 13-1 on page 64.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 13-1 on page 64.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in the section ”Power Consumption” on page 44.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

13.2 Package Drawings

Figure 13-1. TQFP-100 package drawing



	MM		INCH	
	Min	Max	Min	Max
A	----	1.20	----	.047
A1	0.95	1.05	.037	.041
C	0.09	0.20	.004	.008
D	16.00 BSC		.630 BSC	
D1	14.00 BSC		.551 BSC	
E	16.00 BSC		.630 BSC	
E1	14.00 BSC		.551 BSC	
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.50 BSC		.020 BSC	
f	0.17	0.27	.007	.011

Table 13-2. Device and Package Maximum Weight

500	mg

Table 13-3. Package Characteristics

Moisture Sensitivity Level	Jdec J-STD0-20D - MSL 3

Table 13-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

15. Errata

All industrial parts labelled with -UES (engineering samples) are revision E parts.

15.1 Rev. K, L, M

15.1.1 PWM

1. **PWM channel interrupt enabling triggers an interrupt**

   When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

   Fix/Workaround

   When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

2. **PWM counter restarts at 0x0001**

   The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.

   Fix/Workaround

   - The first period is 0x0000, 0x0001, ..., period
   - Consecutive periods are 0x0001, 0x0002, ..., period

3. **PWM update period to a 0 value does not work**

   It is impossible to update a period equal to 0 by the using the PWM update register (PWM_CUPD).

   Fix/Workaround

   Do not update the PWM_CUPD register with a value equal to 0.

15.1.2 ADC

1. **Sleep Mode activation needs additional A to D conversion**

   If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

   Fix/Workaround

   Activate the sleep mode in the mode register and then perform an AD conversion.

15.1.3 SPI

1. **SPI Slave / PDCA transfer: no TX UNDERRUN flag**

   There is no TX UNDERRUN flag available, therefore in SPI slave mode, there is no way to be informed of a character lost in transmission.

   Fix/Workaround

   For PDCA transfer: none.

2. **SPI FDIV option does not work**

   Selecting clock signal using FDIV = 1 does not work as specified.

   Fix/Workaround

   Do not set FDIV = 1.

3. **SPI Bad Serial Clock Generation on 2nd chip_select when SCBR = 1, CPOL=1 and NCPHA=0**
   When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an aditional pulse will be generated on SCK.
   Fix/workaround
   When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

4. **SPI Glitch on RXREADY flag in slave mode when enabling the SPI or during the first transfer**
   In slave mode, the SPI can generate a false RXREADY signal during enabling of the SPI or during the first transfer.

   Fix/Workaround
   1. Set slave mode, set required CPOL/CPHA.
   2. Enable SPI.
   3. Set the polarity CPOL of the line in the opposite value of the required one.
   4. Set the polarity CPOL to the required one.
   5. Read the RXHOLDING register.
   Transfers can now befin and RXREADY will now behave as expected.

5. **SPI Disable does not work in Slave mode**
   Fix/workaround
   Read the last received data then perform a Software reset.

15.1.4 Power Manager

1. **If the BOD level is higher than VDDCORE, the part is constantly under reset**
   If the BOD level is set to a value higher than VDDCORE and enabled by fuses, the part will be in constant reset.

   Fix/Workaround
   Apply an external voltage on VDDCORE that is higher than the BOD level and is lower than VDDCORE max and disable the BOD.

15.1.5 PDCA

1. **Wrong PDCA behavior when using two PDCA channels with the same PID.**
   Fix/Workaround
   The same PID should not be assigned to more than one channel.

15.1.6 TWI

1. **The TWI RXRDY flag in SR register is not reset when a software reset is performed.**
   Fix/Workaround
   After a Software Reset, the register TWI RHR must be read.

15.1.7 USART

1. **ISO7816 info register US_NER cannot be read**
   The NER register always returns zero.
   Fix/Workaround
   None

15.1.8 Processor and Architecture

1. **LDM instruction with PC in the register list and without ++ increments Rp**

For LDM with PC in the register list: the instruction behaves as if the ++ field is always set, ie the pointer is always updated. This happens even if the ++ field is cleared. Specifically, the increment of the pointer is done in parallel with the testing of R12.

Fix/Workaround

None.

When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

4. **SPI Glitch on RXREADY flag in slave mode when enabling the SPI or during the first transfer**

   In slave mode, the SPI can generate a false RXREADY signal during enabling of the SPI or during the first transfer.

   Fix/Workaround

   1. Set slave mode, set required CPOL/CPHA.
   2. Enable SPI.
   3. Set the polarity CPOL of the line in the opposite value of the required one.
   4. Set the polarity CPOL to the required one.
   5. Read the RXHOLDING register.
   Transfers can now befin and RXREADY will now behave as expected.

5. **SPI Disable does not work in Slave mode**
   Fix/workaround
   Read the last received data then perform a Software reset.

15.2.4 Power Manager

1. **If the BOD level is higher than VDDCORE, the part is constantly under reset**

   If the BOD level is set to a value higher than VDDCORE and enabled by fuses, the part will be in constant reset.

   Fix/Workaround
   Apply an external voltage on VDDCORE that is higher than the BOD level and is lower than VDDCORE max and disable the BOD.

15.2.5 PDCA

1. **Wrong PDCA behavior when using two PDCA channels with the same PID.**
   Fix/Workaround
   The same PID should not be assigned to more than one channel.

15.2.6 TWI

1. **The TWI RXRDY flag in SR register is not reset when a software reset is performed.**
   Fix/Workaround
   After a Software Reset, the register TWI RHR must be read.

15.2.7 SDRAMC

1. **Code execution from external SDRAM does not work**

   Code execution from SDRAM does not work.

   Fix/Workaround
   Do not run code from SDRAM.

15.2.8 GPIO

1. **PA29 (TWI SDA) and PA30 (TWI SCL) GPIO VIH (input high voltage) is 3.6V max instead of 5V tolerant**
   The following GPIOs are not 5V tolerant : PA29 and PA30.
   Fix/Workaround