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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	Ethernet, I ² C, SPI, SSC, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	69
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3a1256-aur

- Peripheral Bus A able to run on at divided bus speeds compared to the High Speed Bus

Figure 4-1 gives an overview of the bus system. All modules connected to the same bus use the same clock, but the clock to each module can be individually shut off by the Power Manager. The figure identifies the number of master and slave interfaces of each module connected to the High Speed Bus, and which DMA controller is connected to which peripheral.

Table 5-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
MSEO0 - MSEO1	Trace Frame Control	Output		
EVTI_N	Event In	Output	Low	
EVTO_N	Event Out	Output	Low	
Power Manager - PM				
GCLK0 - GCLK3	Generic Clock Pins	Output		
RESET_N	Reset Pin	Input	Low	
Real Time Counter - RTC				
RTC_CLOCK	RTC clock	Output		
Watchdog Timer - WDT				
WDTEXT	External Watchdog Pin	Output		
External Interrupt Controller - EIC				
EXTINT0 - EXTINT7	External Interrupt Pins	Input		
KPS0 - KPS7	Keypad Scan Pins	Output		
NMI_N	Non-Maskable Interrupt Pin	Input	Low	
Ethernet MAC - MACB				
COL	Collision Detect	Input		
CRS	Carrier Sense and Data Valid	Input		
MDC	Management Data Clock	Output		
MDIO	Management Data Input/Output	I/O		
RXD0 - RXD3	Receive Data	Input		
RX_CLK	Receive Clock	Input		
RX_DV	Receive Data Valid	Input		
RX_ER	Receive Coding Error	Input		
SPEED	Speed			
TXD0 - TXD3	Transmit Data	Output		
TX_CLK	Transmit Clock or Reference Clock	Output		
TX_EN	Transmit Enable	Output		
TX_ER	Transmit Coding Error	Output		

Table 5-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
External Bus Interface - HEBI				
ADDR0 - ADDR23	Address Bus	Output		
CAS	Column Signal	Output	Low	
DATA0 - DATA15	Data Bus	I/O		
NCS0 - NCS3	Chip Select	Output	Low	
NRD	Read Signal	Output	Low	
NWAIT	External Wait Signal	Input	Low	
NWE0	Write Enable 0	Output	Low	
NWE1	Write Enable 1	Output	Low	
NWE3	Write Enable 3	Output	Low	
RAS	Row Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output		
SDCS0	SDRAM Chip Select	Output	Low	
SDWE	SDRAM Write Enable	Output	Low	
General Purpose Input/Output 2 - GPIOA, GPIOB, GPIOC				
P0 - P31	Parallel I/O Controller GPIOA	I/O		
P0 - P31	Parallel I/O Controller GPIOB	I/O		
P0 - P5	Parallel I/O Controller GPIOC	I/O		
P0 - P31	Parallel I/O Controller GPIOX	I/O		
Serial Peripheral Interface - SPI0, SPI1				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS0 - NPCS3	SPI Peripheral Chip Select	I/O	Low	
SCK	Clock	Output		
Synchronous Serial Controller - SSC				
RX_CLOCK	SSC Receive Clock	I/O		

Table 5-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
RX_DATA	SSC Receive Data	Input		
RX_FRAME_SYNC	SSC Receive Frame Sync	I/O		
TX_CLOCK	SSC Transmit Clock	I/O		
TX_DATA	SSC Transmit Data	Output		
TX_FRAME_SYNC	SSC Transmit Frame Sync	I/O		
Timer/Counter - TIMER				
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		
A2	Channel 2 Line A	I/O		
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWI				
SCL	Serial Clock	I/O		
SDA	Serial Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		
CTS	Clear To Send	Input		
DCD	Data Carrier Detect			Only USART1
DSR	Data Set Ready			Only USART1
DTR	Data Terminal Ready			Only USART1
RI	Ring Indicator			Only USART1
RTS	Request To Send	Output		
RXD	Receive Data	Input		
TXD	Transmit Data	Output		

Table 6-1. TQFP100 Package Pinout

23	PA02	48	DM	73	PB05	98	PB17
24	PA03	49	DP	74	PB06	99	PB18
25	PA04	50	GND	75	PB07	100	PB19

Figure 6-2. LQFP144 Pinout

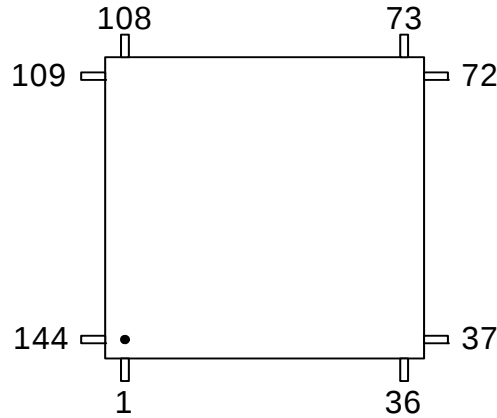


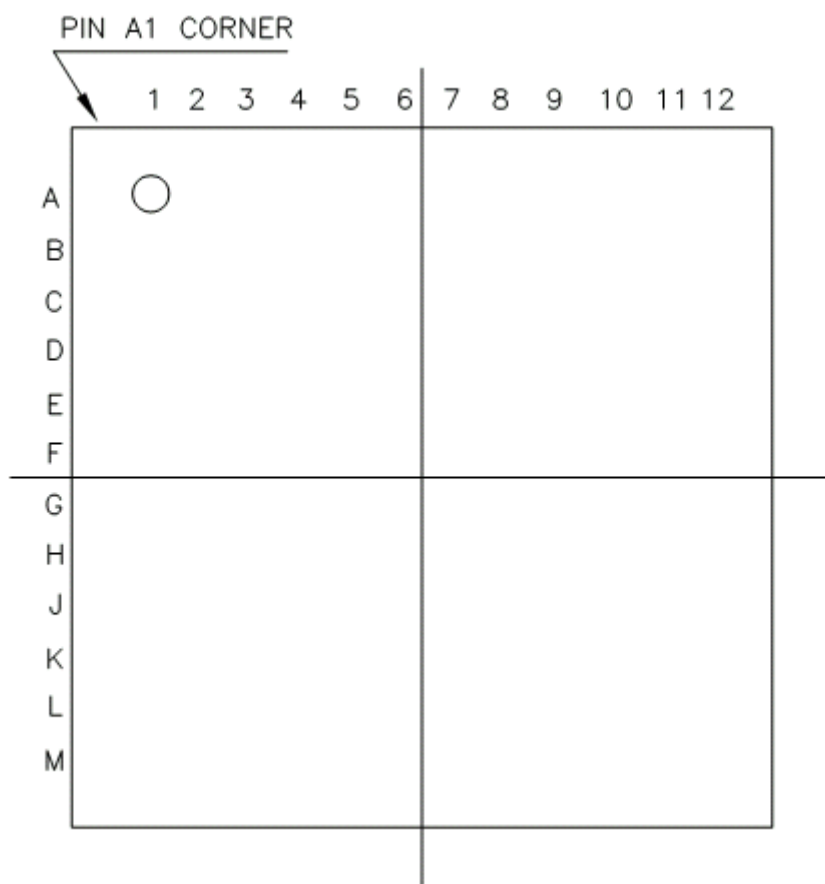
Table 6-2. VQFP144 Package Pinout

1	PX00	37	GND	73	PA21	109	GND
2	PX01	38	PX10	74	PA22	110	PX30
3	PB20	39	PA05	75	PA23	111	PB08
4	PX02	40	PX11	76	PA24	112	PX31
5	PB21	41	PA06	77	PA25	113	PB09
6	PB22	42	PX12	78	PA26	114	PX32
7	VDDIO	43	PA07	79	PA27	115	PB10
8	GND	44	PX13	80	PA28	116	VDDIO
9	PB23	45	PA08	81	VDDANA	117	GND
10	PX03	46	PX14	82	ADVREF	118	PX33
11	PB24	47	PA09	83	GNDANA	119	PB11
12	PX04	48	PA10	84	VDDPLL	120	PX34
13	PB25	49	N/C	85	PC00	121	PB12
14	PB26	50	PA11	86	PC01	122	PA29
15	PB27	51	VDDCORE	87	PX20	123	PA30
16	VDDOUT	52	GND	88	PB00	124	PC02
17	VDDIN	53	PA12	89	PX21	125	PC03
18	GND	54	PA13	90	PB01	126	PB13
19	PB28	55	VDDCORE	91	PX22	127	PB14
20	PB29	56	PA14	92	VDDIO	128	TMS
21	PB30	57	PA15	93	VDDIO	129	TCK

Table 6-2. VQFP144 Package Pinout

22	PB31	58	PA16	94	GND	130	TDO
23	RESET_N	59	PX15	95	PX23	131	TDI
24	PX05	60	PA17	96	PB02	132	PC04
25	PA00	61	PX16	97	PX24	133	PC05
26	PX06	62	PA18	98	PB03	134	PB15
27	PA01	63	PX17	99	PX25	135	PX35
28	GND	64	PA19	100	PB04	136	PB16
29	VDDCORE	65	PX18	101	PX26	137	PX36
30	PA02	66	PA20	102	PB05	138	VDDCORE
31	PX07	67	PX19	103	PX27	139	PB17
32	PA03	68	VBUS	104	PB06	140	PX37
33	PX08	69	VDDIO	105	PX28	141	PB18
34	PA04	70	DM	106	PB07	142	PX38
35	PX09	71	DP	107	PX29	143	PB19
36	VDDIO	72	GND	108	VDDIO	144	PX39

Figure 6-3. BGA144 Pinout



7. Power Considerations

7.1 Power Supplies

The AT32UC3A has several types of power supply pins:

- **VDDIO:** Powers I/O lines. Voltage is 3.3V nominal.
- **VDDANA:** Powers the ADC. Voltage is 3.3V nominal.
- **VDDIN:** Input voltage for the voltage regulator. Voltage is 3.3V nominal.
- **VDDCORE:** Powers the core, memories, and peripherals. Voltage is 1.8V nominal.
- **VDDPLL:** Powers the PLL. Voltage is 1.8V nominal.

The ground pins GND are common to VDDCORE, VDDIO, VDDPLL. The ground pin for VDDANA is GNDANA.

Refer to ["Power Consumption" on page 44](#) for power consumption on the various supply pins.

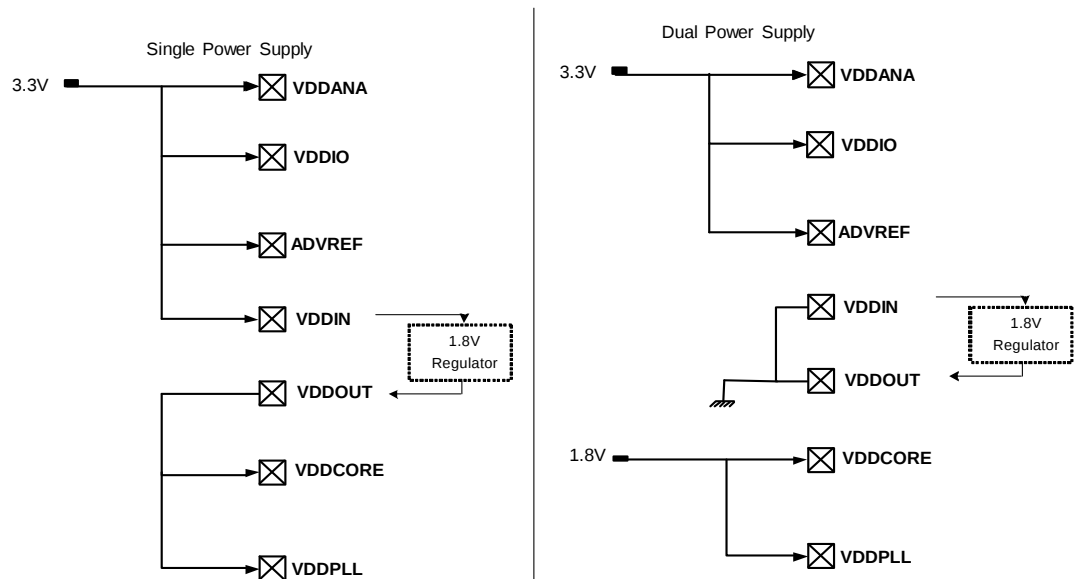


Figure 9-1. HMatrix Master / Slave Connections

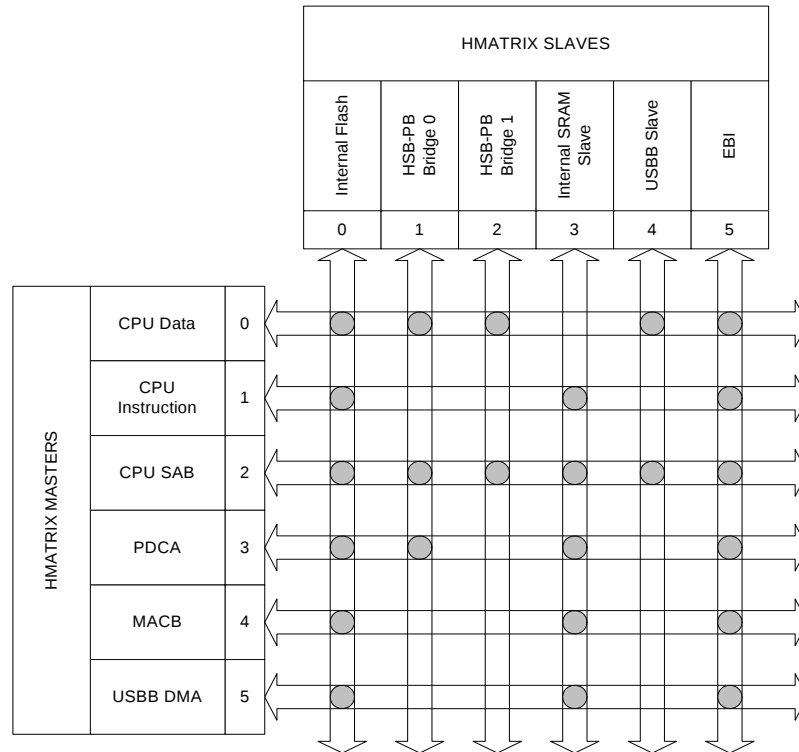


Table 10-9. GPIO Controller Function Multiplexing

	99	PX25	GPIO 79	EBI - ADDR[9]	EIM - SCAN[6]	
	101	PX26	GPIO 78	EBI - ADDR[8]	EIM - SCAN[7]	
	103	PX27	GPIO 77	EBI - ADDR[7]	SPI0 - MISO	
	105	PX28	GPIO 76	EBI - ADDR[6]	SPI0 - MOSI	
	107	PX29	GPIO 75	EBI - ADDR[5]	SPI0 - SCK	
	110	PX30	GPIO 74	EBI - ADDR[4]	SPI0 - NPCS[0]	
	112	PX31	GPIO 73	EBI - ADDR[3]	SPI0 - NPCS[1]	
	114	PX32	GPIO 72	EBI - ADDR[2]	SPI0 - NPCS[2]	
	118	PX33	GPIO 71	EBI - ADDR[1]	SPI0 - NPCS[3]	
	120	PX34	GPIO 70	EBI - ADDR[0]	SPI1 - MISO	
	135	PX35	GPIO 105	EBI - DATA[15]	SPI1 - MOSI	
	137	PX36	GPIO 104	EBI - DATA[14]	SPI1 - SCK	
	140	PX37	GPIO 103	EBI - DATA[13]	SPI1 - NPCS[0]	
	142	PX38	GPIO 102	EBI - DATA[12]	SPI1 - NPCS[1]	
	144	PX39	GPIO 101	EBI - DATA[11]	SPI1 - NPCS[2]	

10.8 Oscillator Pinout

The oscillators are not mapped to the normal A,B or C functions and their muxings are controlled by registers in the Power Manager (PM). Please refer to the power manager chapter for more information about this.

Table 10-10. Oscillator pinout

TQFP100 pin	VQFP144 pin	Pad	Oscillator pin
85	124	PC02	xin0
93	132	PC04	xin1
63	85	PC00	xin32
86	125	PC03	xout0
94	133	PC05	xout1
64	86	PC01	xout32

10.9 USART Configuration

Table 10-11. USART Supported Mode

	SPI	RS485	ISO7816	IrDA	Modem	Manchester Encoding
USART0	Yes	No	No	No	No	No
USART1	Yes	Yes	Yes	Yes	Yes	Yes
USART2	Yes	No	No	No	No	No
USART3	Yes	No	No	No	No	No

- Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
 - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
 - Communication at up to 115.2 Kbps
- Test Modes
 - Remote Loopback, Local Loopback, Automatic Echo
- SPI Mode
 - Master or Slave
 - Serial Clock Programmable Phase and Polarity
 - SPI Serial Clock (SCK) Frequency up to Internal Clock Frequency PBA/4
- Supports Connection of Two Peripheral DMA Controller Channels (PDC)
 - Offers Buffer Transfer without Processor Intervention

10.11.8 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.11.9 Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
 - Frequency Measurement
 - Event Counting
 - Interval Measurement
 - Pulse Generation
 - Delay Timing
 - Pulse Width Modulation
 - Up/down Capabilities
- Each channel is user-configurable and contains:
 - Three external clock inputs
 - Five internal clock inputs
 - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

10.11.10 Pulse Width Modulation Controller

- 7 channels, one 20-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
 - A Modulo n counter providing eleven clocks
 - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
 - Independent Enable Disable Commands
 - Independent Clock
 - Independent Period and Duty Cycle, with Double Bufferization
 - Programmable selection of the output waveform polarity
 - Programmable center or left aligned output waveform

12.3 Regulator characteristics

Table 12-2. Electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{VDDIN}	Supply voltage (input)		3	3.3	3.6	V
V_{VDDOUT}	Supply voltage (output)		1.81	1.85	1.89	V
I_{OUT}	Maximum DC output current with $V_{VDDIN} = 3.3V$				100	mA
	Maximum DC output current with $V_{VDDIN} = 2.7V$				90	mA
I_{SCR}	Static Current of internal regulator	Low Power mode (stop, deep stop or static) at $T_A = 25^\circ C$		10		μA

Table 12-3. Decoupling requirements

Symbol	Parameter	Condition	Typ.	Techno.	Units
C_{IN1}	Input Regulator Capacitor 1		1	NPO	nF
C_{IN2}	Input Regulator Capacitor 2		4.7	X7R	μF
C_{OUT1}	Output Regulator Capacitor 1		470	NPO	pF
C_{OUT2}	Output Regulator Capacitor 2		2.2	X7R	μF

12.4 Analog characteristics

Table 12-4. Electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{ADVREF}	Analog voltage reference (input)		2.6		3.6	V

Table 12-5. Decoupling requirements

Symbol	Parameter	Condition	Typ.	Techno.	Units
C_{VREF1}	Voltage reference Capacitor 1		10	-	nF
C_{VREF2}	Voltage reference Capacitor 2		1	-	μF

12.4.1 BOD

Table 12-6. BODLEVEL Values

BODLEVEL Value	Typ.	Typ.	Typ.	Units.
00 0000b	1.40	1.47	1.55	V
01 0111b	1.45	1.52	1.6	V
01 1111b	1.55	1.6	1.65	V
10 0111b	1.65	1.69	1.75	V

The values in [Table 12-6](#) describes the values of the BODLEVEL in the flash FGPFRR register.

12.7.2 Main Oscillators Characteristics

Table 12-15. Main Oscillator Characteristics

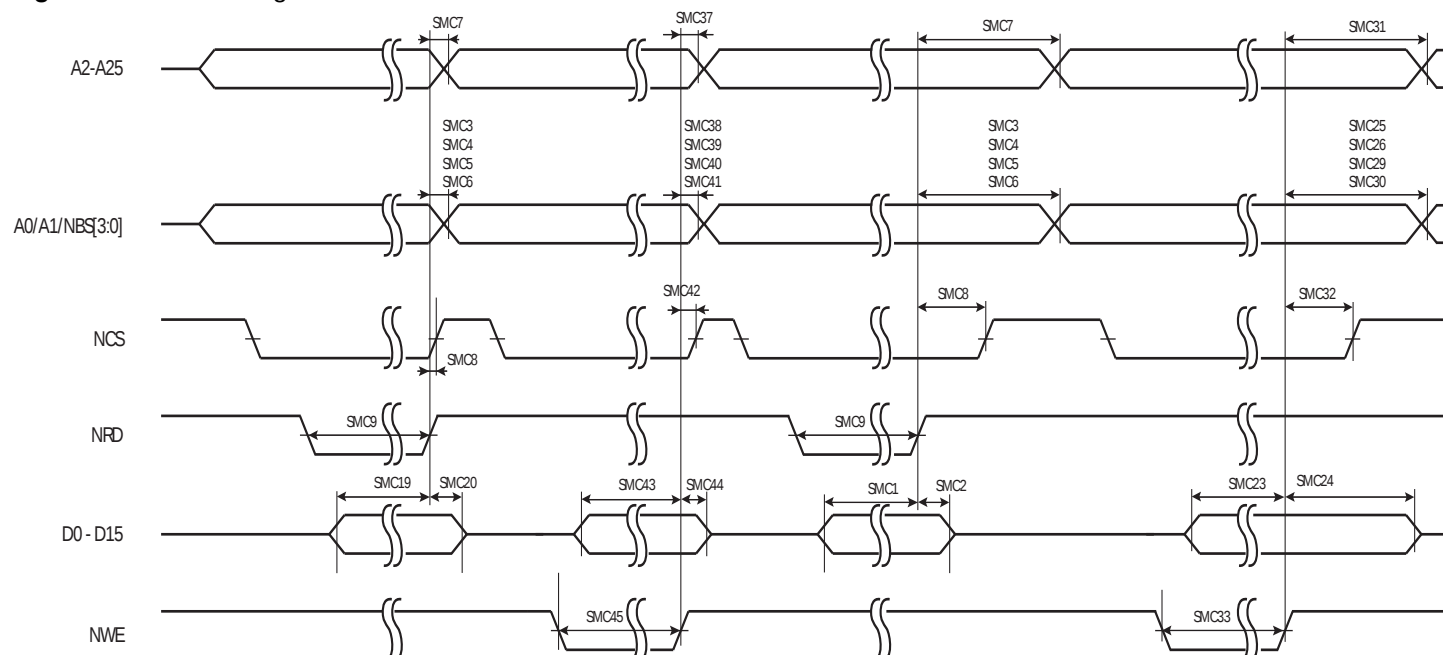
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency		0.45		16	MHz
C_{L1}, C_{L2}	Internal Load Capacitance ($C_{L1} = C_{L2}$)			12		pF
	Duty Cycle		40	50	60	%
t_{ST}	Startup Time				TBD	ms
$1/(t_{CPXIN})$	XIN Clock Frequency	External clock			50	MHz
		Crystal	0.45		16	MHz
t_{CHXIN}	XIN Clock High Half-period		$0.4 \times t_{CPXIN}$		$0.6 \times t_{CPXIN}$	
t_{CLXIN}	XIN Clock Low Half-period		$0.4 \times t_{CPXIN}$		$0.6 \times t_{CPXIN}$	
C_{IN}	XIN Input Capacitance			7		pF

12.7.3 PLL Characteristics

Table 12-16. Phase Lock Loop Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{OUT}	Output Frequency		80		240	MHz
F_{IN}	Input Frequency		4		16	MHz
I_{PLL}	Current Consumption	active mode ($F_{out}=80\text{Mhz}$)		250		μA
		active mode ($F_{out}=240\text{Mhz}$)		600		μA

Figure 12-3. SMC Signals for NRD and NRW Controlled Accesses.



12.9.1 SDRAM Signals

These timings are given for 10 pF load on SDCK and 40 pF on other signals.

Table 12-27. SDRAM Clock Signal.

Symbol	Parameter	Max ⁽¹⁾	Units
$1/(t_{\text{CPSDCK}})$	SDRAM Controller Clock Frequency	$1/(t_{\text{cpCPU}})$	MHz

Note: 1. The maximum frequency of the SDRAMC interface is the same as the max frequency for the HSB.

Table 12-28. SDRAM Clock Signal.

Symbol	Parameter	Min	Units
SDRAMC ₁	SDCKE High before SDCK Rising Edge	7.4	ns
SDRAMC ₂	SDCKE Low after SDCK Rising Edge	3.2	
SDRAMC ₃	SDCKE Low before SDCK Rising Edge	7	
SDRAMC ₄	SDCKE High after SDCK Rising Edge	2.9	
SDRAMC ₅	SDCS Low before SDCK Rising Edge	7.5	
SDRAMC ₆	SDCS High after SDCK Rising Edge	1.6	
SDRAMC ₇	RAS Low before SDCK Rising Edge	7.2	
SDRAMC ₈	RAS High after SDCK Rising Edge	2.3	
SDRAMC ₉	SDA10 Change before SDCK Rising Edge	7.6	
SDRAMC ₁₀	SDA10 Change after SDCK Rising Edge	1.9	

Figure 12-4. SDRAMC Signals relative to SDCK.

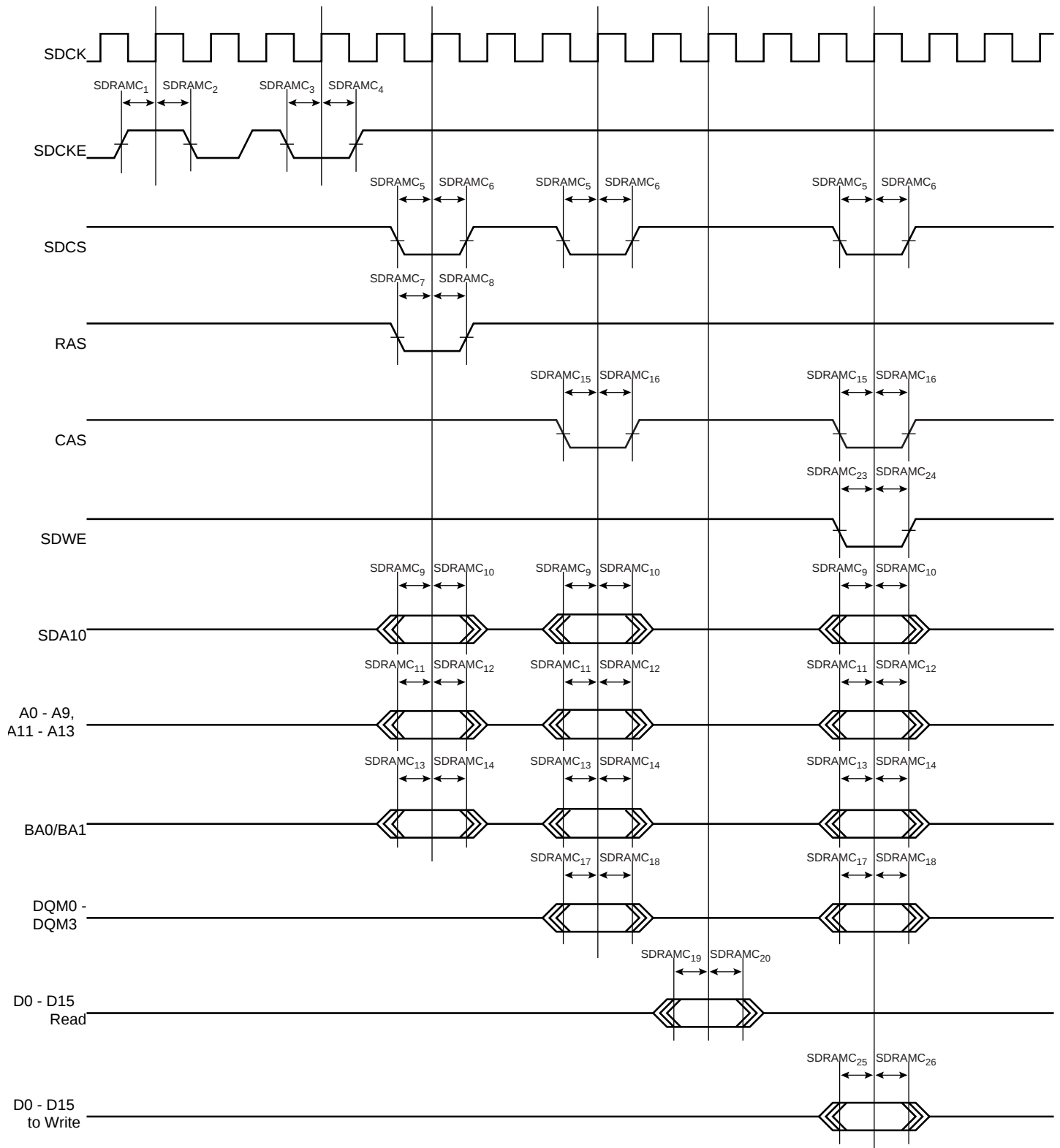


Figure 12-7. SPI Master mode with (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)

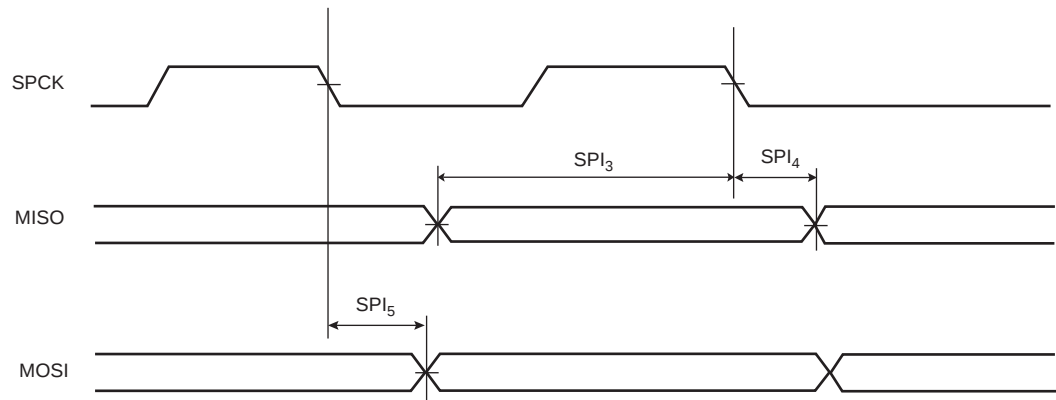


Figure 12-8. SPI Slave mode with (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)

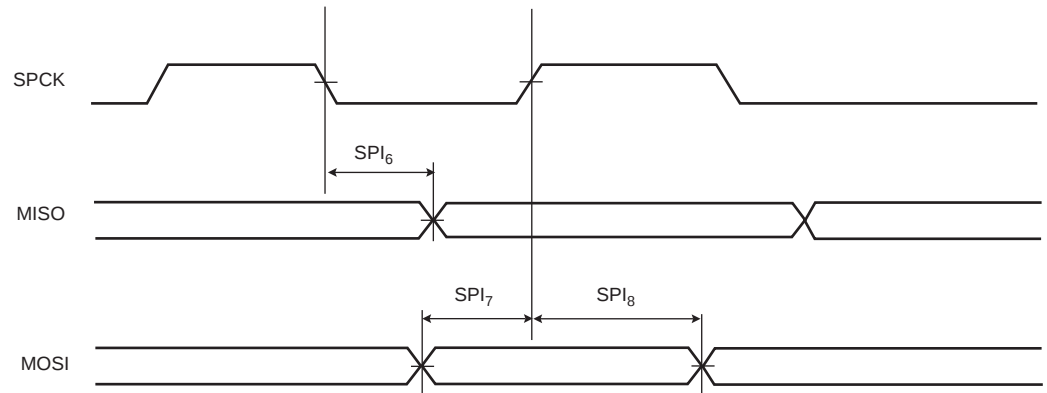
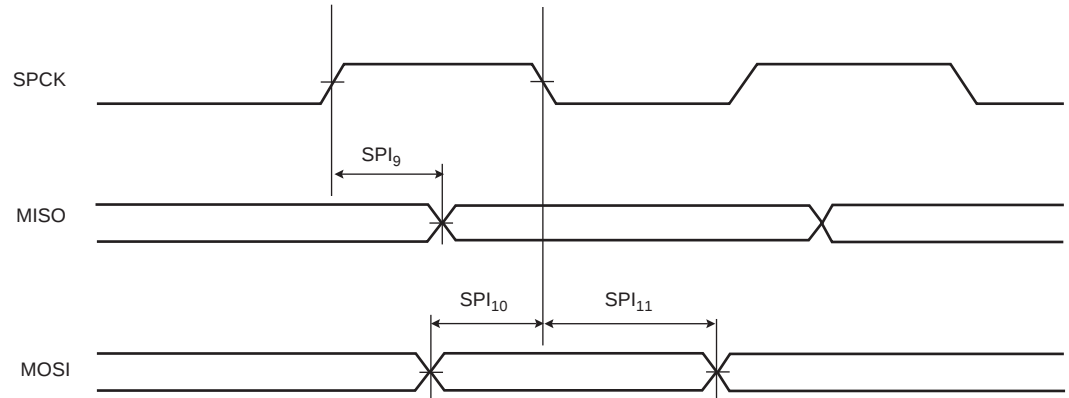


Figure 12-9. SPI Slave mode with (CPOL = NCPHA = 0) or (CPOL= NCPHA= 1)



13.3 Soldering Profile

Table 13-11 gives the recommended soldering profile from J-STD-20.

Table 13-11. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/sec
Preheat Temperature 175°C ±25°C	Min. 150 °C, Max. 200 °C
Time Maintained Above 217°C	60-150 sec
Time within 5-C of Actual Peak Temperature	30 sec
Peak Temperature Range	260 °C
Ramp-down Rate	6 °C/sec
Time 25-C to Peak Temperature	Max. 8 minutes

Note: It is recommended to apply a soldering temperature higher than 250°C.
A maximum of three reflow passes is allowed per component.

15.2 Rev. J

15.2.1 PWM

1. PWM channel interrupt enabling triggers an interrupt

When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

Fix/Workaround

When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

2. PWM counter restarts at 0x0001

The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.

Fix/Workaround

- The first period is 0x0000, 0x0001, ..., period
- Consecutive periods are 0x0001, 0x0002, ..., period

3. PWM update period to a 0 value does not work

It is impossible to update a period equal to 0 by the using the PWM update register (PWM_CUPD).

Fix/Workaround

Do not update the PWM_CUPD register with a value equal to 0.

15.2.2 ADC

1. Sleep Mode activation needs additional A to D conversion

If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

Fix/Workaround

Activate the sleep mode in the mode register and then perform an AD conversion.

15.2.3 SPI

1. SPI Slave / PDCA transfer: no TX UNDERRUN flag

There is no TX UNDERRUN flag available, therefore in SPI slave mode, there is no way to be informed of a character lost in transmission.

Fix/Workaround

For PDCA transfer: none.

2. SPI FDIV option does not work

Selecting clock signal using FDIV = 1 does not work as specified.

Fix/Workaround

Do not set FDIV = 1.

3. SPI Bad Serial Clock Generation on 2nd chip_select when SCBR = 1, CPOL=1 and NCPHA=0

When multiple CS are in use, if one of the baudrate equals to 1 and one of the others doesn't equal to 1, and CPOL=1 and CPHA=0, then an additional pulse will be generated on SCK.

Fix/workaround

When multiple CS are in use, if one of the baudrate equals 1, the other must also equal 1 if CPOL=1 and CPHA=0.

4. **SPI Glitch on RXREADY flag in slave mode when enabling the SPI or during the first transfer**

In slave mode, the SPI can generate a false RXREADY signal during enabling of the SPI or during the first transfer.

Fix/Workaround

1. Set slave mode, set required CPOL/CPHA.
2. Enable SPI.
3. Set the polarity CPOL of the line in the opposite value of the required one.
4. Set the polarity CPOL to the required one.
5. Read the RXHOLDING register.

Transfers can now begin and RXREADY will now behave as expected.

5. **SPI Disable does not work in Slave mode**

Fix/workaround

Read the last received data then perform a Software reset.

15.3.4 Power Manager

1. **If the BOD level is higher than VDDCORE, the part is constantly under reset**

If the BOD level is set to a value higher than VDDCORE and enabled by fuses, the part will be in constant reset.

Fix/Workaround

Apply an external voltage on VDDCORE that is higher than the BOD level and is lower than VDDCORE max and disable the BOD.

15.3.5 Flashc

1. **On AT32UC3A0512 and AT32UC3A1512, corrupted read in flash after FLASHC WP, EP, EA, WUP, EUP commands may happen**

- After a FLASHC Write Page (WP) or Erase Page (EP) command applied to a page in a given half of the flash (first or last 256 kB of flash), reading (data read or code fetch) the other half of the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

- After a FLASHC Erase All (EA) command, reading (data read or code fetch) the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

- After a FLASHC Write User Page (WUP) or Erase User Page (EUP) command, reading (data read or code fetch) the second half (last 256 kB) of the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

Fix/Workaround

Flashc WP, EP, EA, WUP, EUP commands: these commands must be issued from RAM or through the EBI. After these commands, read twice one flash page initialized to 00h in each half part of the flash.

15.3.6 PDCA

1. **Wrong PDCA behavior when using two PDCA channels with the same PID.**



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