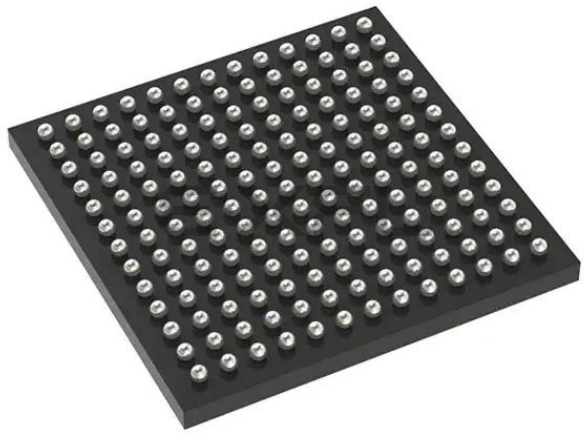

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	136
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-UFBGA
Supplier Device Package	169-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4a6agi6p

- Rich analog peripherals (independent supply)
  - 3 × 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 2 x 12-bit DAC output channels, low-power sample and hold
  - 2 x operational amplifiers with built-in PGA
  - 2 x ultra-low-power comparators
- 20 x communication interfaces
  - USB OTG 2.0 full-speed, LPM and BCD
  - 2 x SAIs (serial audio interface)
  - 4 x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 5 x U(S)ARTs (ISO 7816, LIN, IrDA, modem)
  - 1 x LPUART
  - 3 x SPIs (4 x SPIs with the Quad SPI)
  - 2 x CAN (2.0B Active) and SDMMC
  - SWPMI single wire protocol master I/F
  - IRTIM (Infrared interface)
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™

Table 1. Device summary

Reference	Part numbers
STM32L4A6xG	STM32L4A6AG, STM32L4A6QG, STM32L4A6RG, STM32L4A6VG, STM32L4A6ZG

Table 2. STM32L4A6xG family device features and peripheral counts (continued)

Peripheral	STM32L4A6AG	STM32L4A6ZG	STM32L4A6QG	STM32L4A6VG	STM32L4A6RG
LCD COM x SEG	Yes 8x40 or 4x44				
Random generator	Yes				
AES + HASH	Yes				
GPIOs(3) Wakeup pins Nb of I/Os down to 1.08 V	136 5 14	115 5 14	110 5 14	83 5 0	52 4 0
Capacitive sensing Number of channels	24	24	24	21	21
12-bit ADCs Number of channels	3 24	3 24	3 19	3 16	3 16
12-bit DAC channels	2				
Internal voltage reference buffer	Yes				
Analog comparator	2				
Operational amplifiers	2				
Max. CPU frequency	80 MHz				
Operating voltage (V_{DD})	1.71 to 3.6 V				
Operating voltage (V_{DD12})	1.05 to 1.32 V				
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 130 °C				
Packages	UFBGA169	LQFP144	UFBGA132	LQFP100 WLCSP100	LQFP64

1. For the LQFP100 and WLCSP100 packages, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. Only up to 13 data bits.
3. In case external SMPS package type is used, 2 GPIO's are replaced by VDD12 pins to connect the SMPS power supplies hence reducing the number of available GPIO's by 2.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

Table 6. STM32L4A6xG peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD DFSDM1 (analog watchdog, short circuit detection)	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y (1)
	ADCx DAC1 DFSDM1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

without having any impact on the timing of “injected” conversions

– “injected” conversions for precise timing and with high conversion priority

3.25 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.26 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.27 Advanced encryption standard hardware accelerator (AES)

The devices embed an AES hardware accelerator can be used to both encipher and decipher data using AES algorithm.

The AES peripheral supports:

- Encryption/Decryption using AES Rijndael Block Cipher algorithm
- NIST FIPS 197 compliant implementation of AES encryption/decryption algorithm
- 128-bit and 256-bit register for storing the encryption, decryption or derivation key (4x 32-bit registers)
- Electronic codebook (ECB), Cipher block chaining (CBC), Counter mode (CTR), Galois Counter Mode (GCM), Galois Message Authentication Code mode (GMAC) and Cipher Message Authentication Code mode (CMAC) supported.
- Key scheduler
- Key derivation for decryption
- 128-bit data block processing
- 128-bit, 256-bit key length
- 1x32-bit INPUT buffer and 1x32-bit OUTPUT buffer.
- Register access supporting 32-bit data width only.
- One 128-bit Register for the initialization vector when AES is configured in CBC mode or for the 32-bit counter initialization when CTR mode is selected, GCM mode or CMAC mode.
- Automatic data flow control with support of direct memory access (DMA) using 2 channels, one for incoming data, and one for outcoming data.
- Suspend a message if another message with a higher priority needs to be processed

Table 15. STM32L4A6xG pin definitions

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	-	-	-	-	C3	C3	PI11	I/O	FT	-	EVENTOUT	-
-	B9	C8	1	B2	B2	1	1	D3	D3	PE2	I/O	FT_l	-	TRACECK, TIM3_ETR, TSC_G7_IO1, LCD_SEG38, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
-	B10	B10	2	A1	A1	2	2	D2	D2	PE3	I/O	FT_l	-	TRACED0, TIM3_CH1, TSC_G7_IO2, LCD_SEG39, FMC_A19, SAI1_SD_B, EVENTOUT	-
-	C8	E7	3	B1	B1	3	3	D1	D1	PE4	I/O	FT	-	TRACED1, TIM3_CH2, DFSDM1_DATIN3, TSC_G7_IO3, DCMI_D4, FMC_A20, SAI1_FS_A, EVENTOUT	-
-	D8	E8	4	C2	C2	4	4	E4	E4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, DFSDM1_CKIN3, TSC_G7_IO4, DCMI_D6, FMC_A21, SAI1_SCK_A, EVENTOUT	-
-	E7	D8	5	D2	D2	5	5	E3	E3	PE6	I/O	FT	-	TRACED3, TIM3_CH4, DCMI_D7, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_TAMP3/WKUP3
1	C10	C10	6	E2	E2	6	6	E2	E2	VBAT	S	-	-	-	-
2	C9	C9	7	C1	C1	7	7	E1	E1	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1/RTC_TS/RTC_OUT/WKUP2
3	D10	D10	8	D1	D1	8	8	F1	F1	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN

Table 15. STM32L4A6xG pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
12	H9	H9	19	J1	J1	30	30	K2	K2	VSSA/VREF-	S	-	-	-	-
-	G8	-	20	-	-	31	31	-	-	VREF-	S	-	-	-	-
-	G7	H10	21	L1	L1	32	32	L1	L1	VREF+	S	-	-	-	VREFBUF_OUT
-	J10	J10	22	M1	M1	33	33	L2	L2	VDDA	S	-	-	-	-
13	-	-	-	-	-	-	-	-	-	VDDA/VREF+	-	-	-	-	-
14	G9	G8	23	L2	L2	34	34	K3	K3	PA0	I/O	FT_a	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, ADC12_IN5, RTC_TAMP2/WKUP1
-	-	-	-	M3	M3	-	-	M1	M1	OPAMP1_VINM	I	TT	-	-	-
15	H8	G7	24	M2	M2	35	35	N2	N2	PA1	I/O	FT_la	(3)	TIM2_CH2, TIM5_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, UART4_RX, LCD_SEG0, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, ADC12_IN6
16	H7	H8	25	K3	K3	36	36	N1	N1	PA2	I/O	FT_la	-	TIM2_CH3, TIM5_CH3, USART2_TX, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG1, SAI2_EXTCLK, TIM15_CH1, EVENTOUT	ADC12_IN7, WKUP4/LSCO

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_ DATIN0	USART3_RTS_ DE
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM1_CKIN0	-
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_ DE
	PB4	NJTRST	-	TIM3_CH1	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS
	PB5	-	LPTIM1_IN1	TIM3_CH2	CAN2_RX	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	I2C4_SCL	DFSDM1_ DATIN5	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	I2C4_SDA	DFSDM1_CKIN5	USART1_RX
	PB8	-	-	TIM4_CH3	-	I2C1_SCL	-	DFSDM1_ DATIN6	-
	PB9	-	IR_OUT	TIM4_CH4	-	I2C1_SDA	SPI2_NSS	DFSDM1_CKIN6	-
	PB10	-	TIM2_CH3	-	I2C4_SCL	I2C2_SCL	SPI2_SCK	DFSDM1_ DATIN7	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN_ COMP2	I2C2_SMBA	SPI2_NSS	DFSDM1_ DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM1_CKIN1	USART3_CTS
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2C2_SDA	SPI2_MISO	DFSDM1_ DATIN2	USART3_RTS_ DE
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	DFSDM1_CKIN2	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-
	PF1	-	-	-	-	I2C2_SCL	-	-	-
	PF2	-	-	-	-	I2C2_SMBA	-	-	-
	PF3	-	-	-	-	-	-	-	-
	PF4	-	-	-	-	-	-	-	-
	PF5	-	-	-	-	-	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	QUADSPI_CLK	-	-	-	-
	PF11	-	-	-	-	-	-	-	-
	PF12	-	-	-	-	-	-	-	-
	PF13	-	-	-	-	I2C4_SMBA	-	DFSDM1_ DATIN6	-
	PF14	-	-	-	-	I2C4_SCL	-	DFSDM1_CKIN6	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port G	PG0	-	-	-	-	-	-	-	-
	PG1	-	-	-	-	-	-	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	-	I2C3_SMBA	-	-	-
	PG7	-	-	-	-	I2C3_SCL	-	-	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	-	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	-	-	-	SPI3_MOSI	USART1_CTS
	PG12	-	LPTIM1_ETR	-	-	-	-	SPI3_NSS	USART1_RTS_ DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-

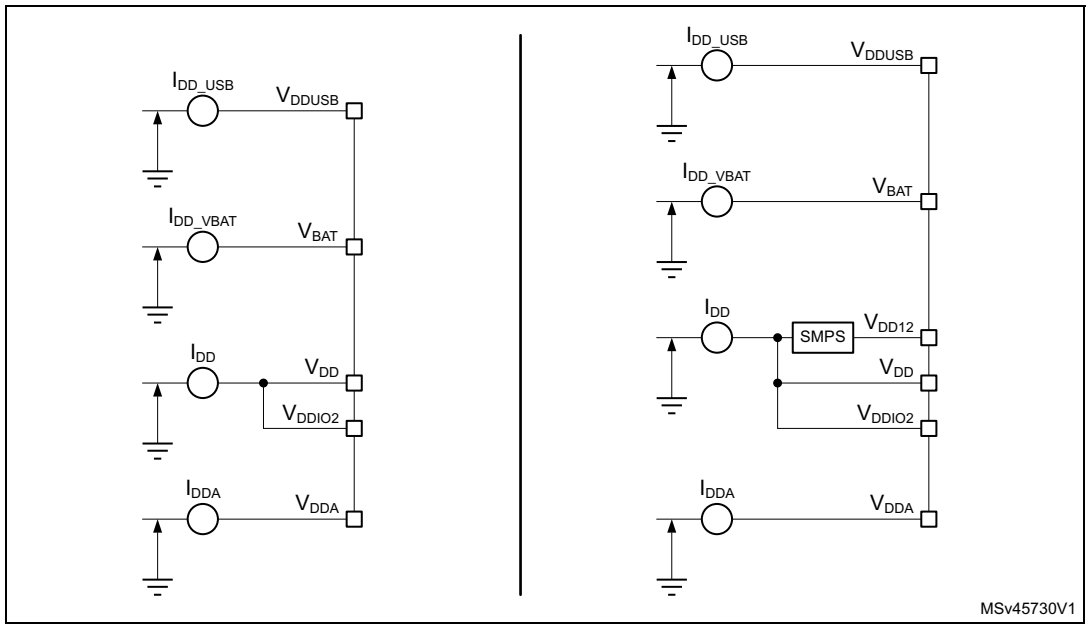
Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port I	PI0	-	-	DCMI_D13	-	-	-	-	EVENTOUT
	PI1	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PI2	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PI3	-	-	DCMI_D10	-	-	-	-	EVENTOUT
	PI4	-	-	DCMI_D5	-	-	-	-	EVENTOUT
	PI5	-	-	DCMI_VSYNC	-	-	-	-	EVENTOUT
	PI6	-	-	DCMI_D6	-	-	-	-	EVENTOUT
	PI7	-	-	DCMI_D7	-	-	-	-	EVENTOUT
	PI8	-	-	DCMI_D12	-	-	-	-	EVENTOUT
	PI9	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-	-	-	-	-	-	EVENTOUT
	PI11	-	-	-	-	-	-	-	EVENTOUT

1. Please refer to *Table 16* for AF0 to AF7.

6.1.7 Current consumption measurement

Figure 21. Current consumption measurement scheme with and without external SMPS power supply



The I_{DD_ALL} parameters given in *Table 26* to *Table 48* represent the total MCU consumption including the current supplying V_{DD}, V_{DDIO2}, V_{DDA}, V_{DDUSB} and V_{BAT}.

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics* and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 41. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.79	0.82	0.95	1.17	1.63	0.9	1.0	1.2	1.7	2.7	mA
				16 MHz	0.54	0.57	0.7	0.92	1.38	0.6	0.7	1.0	1.4	2.4	
				8 MHz	0.33	0.37	0.49	0.71	1.17	0.4	0.5	0.7	1.2	2.2	
				4 MHz	0.23	0.26	0.39	0.61	1.06	0.3	0.4	0.6	1.1	2.1	
				2 MHz	0.18	0.21	0.34	0.56	1.01	0.2	0.3	0.5	1.0	1.0	
				1 MHz	0.16	0.19	0.31	0.53	0.99	0.2	0.3	0.5	1.0	1.0	
				100 kHz	0.13	0.17	0.29	0.51	0.96	0.1	0.3	0.5	1.0	1.9	
			Range 1	80 MHz	2.57	2.62	2.76	3.01	3.53	2.8	2.9	3.2	3.8	4.9	
				72 MHz	2.34	2.38	2.53	2.78	3.29	2.6	2.7	3.0	3.5	4.6	
				64 MHz	2.1	2.15	2.29	2.54	3.05	2.3	2.4	2.7	3.3	4.4	
				48 MHz	1.58	1.63	1.78	2.03	2.54	1.8	1.9	2.2	2.7	3.8	
				32 MHz	1.11	1.15	1.3	1.54	2.05	1.2	1.4	1.7	2.2	3.3	
				24 MHz	0.87	0.91	1.06	1.3	1.81	1.0	1.1	1.4	1.9	3.0	
				16 MHz	0.63	0.67	0.82	1.06	1.56	0.7	0.8	1.1	1.6	2.7	
I_{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	103	140	270	506	985	130	247	500	990	2025	µA
				1 MHz	74.2	111	245	476	955	100	215	467	963	1999	
				400 kHz	60	89.8	224	457	937	79	194	444	941	1975	
				100 kHz	53.7	84.1	216	448	928	70	185	434	933	1967	

1. Guaranteed by characterization results, unless otherwise specified.

Table 45. Current consumption in Stop 1 mode (continued)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (wakeup from Stop1)	Supply current during wakeup from Stop 1	Wakeup clock MSI = 48 MHz, voltage Range 1. See (4).		3 V	0.99	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock MSI = 4 MHz, voltage Range 2. See (4).		3 V	1.1	-	-	-	-	-	-	-	-	-	
		Wakeup clock HSI16 = 16 MHz, voltage Range 1. See (4).		3 V	0.95	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Table 46. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions	TYP					MAX(1)					Unit
		V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 0)	Supply current in Stop 0 mode, RTC disabled	1.8 V	127	153	244	404	734	148	218	471	905	1795	µA
		2.4 V	129	155	247	407	737	151	221	474	910	1803	
		3 V	131	156	249	409	741	154	224	478	915	1813	
		3.6 V	133	158	251	412	744	157	228	482	921	1822(2)	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 47. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	no independent watchdog	1.8 V	108	299	1343	3822	10353	227	899	4159	13059	36572	nA
			2.4 V	118	348	1562	4447	12012	252	1009	4846	15026	41366	
			3 V	133	404	1777	5071	13589	318	1211	6082	17245	46714	
			3.6 V	171	501	2115	5898	15539	435	1508	7230	19850	52888(2)	
		with independent watchdog	1.8 V	296	-	-	-	-	-	-	-	-	-	
			2.4 V	349	-	-	-	-	-	-	-	-	-	
			3 V	411	-	-	-	-	-	-	-	-	-	
			3.6 V	506	-	-	-	-	-	-	-	-	-	
I_{DD_ALL} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	377	581	1700	4270	11100	763	1422	5182	13585	36564	nA
			2.4 V	461	700	2020	5030	12900	942	1704	5992	15473	41383	
			3 V	559	843	2390	5990	15500	1166	2032	6938	17889	46728	
			3.6 V	689	1050	2920	7130	18100	1454	2511	7754	20714	53018	
		RTC clocked by LSI, with independent watchdog	1.8 V	422	-	-	-	-	-	-	-	-	-	
			2.4 V	518	-	-	-	-	-	-	-	-	-	
			3 V	560	-	-	-	-	-	-	-	-	-	
			3.6 V	780	-	-	-	-	-	-	-	-	-	

Table 47. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSE bypassed at 32768Hz	1.8 V	308	504	1683	4193	10783	-	-	-	-	-	nA
			2.4 V	400	633	1963	4957	12583	-	-	-	-	-	
			3 V	508	779	2319	5925	15130	-	-	-	-	-	
			3.6 V	661	1009	2825	7027	17540	-	-	-	-	-	
		RTC clocked by LSE quartz (3) in low drive mode	1.8 V	426	624	1679	4244	10884	-	-	-	-	-	
			2.4 V	521	751	1985	4952	12619	-	-	-	-	-	
			3 V	643	914	2371	5931	15121	-	-	-	-	-	
			3.6 V	819	1162	2914	7019	17551	-	-	-	-	-	
I_{DD_ALL} (SRAM2)(4)	Supply current to be added in Standby mode when SRAM2 is retained	-	1.8 V	371	1111	4297	10153	22747	806	2640	10537	24695	54376	nA
			2.4 V	372	1112	4328	10154	22888	809	2661	10545	24767	54505	
			3 V	374	1116	4403	10429	23711	811	2683	10553	24840	54634	
			3.6 V	378	1149	4545	10702	24361	814	2704	10561	24913	54763	
I_{DD_ALL} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is MSI = 4 MHz. See (5).	3 V	1.4	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. The supply current in Standby with SRAM2 mode is: I_{DD_ALL}(Standby) + I_{DD_ALL}(SRAM2). The supply current in Standby with RTC with SRAM2 mode is: II_{DD_ALL}(Standby + RTC) + I_{DD_ALL}(SRAM2).
5. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Table 70. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}(4)	FT_xx input leakage current(3)(5)	$V_{IN} \le Max(V_{DDXXX})$(6)(7)	-	-	±100	nA
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(6)(7)	-	-	650	
		$Max(V_{DDXXX})+1$ V < $V_{IN} \le 5.5$ V(6)(7)	-	-	200	
	FT_lu, FT_u, PB2 and PC3 IO	$V_{IN} \le Max(V_{DDXXX})$ (6)(7)	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(6)(7)	-	-	2500(3)	
		$Max(V_{DDXXX})+1$ V < $V_{IN} \le 5.5$ V(6)(7)	-	-	250	
	TT_xx input leakage current	$V_{IN} \le Max(V_{DDXXX})$(6)	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN} < 3.6$ V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current (UFBGA132 only)	-	-	-	(8)	
R_{PU}	Weak pull-up equivalent resistor (9)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(9)	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to *Figure 30: I/O input characteristics*.
2. Guaranteed by test production.
3. Guaranteed by design.
4. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
5. All FT_xx GPIOs except FT_lu, FT_u, PB2 and PC3.
6. $Max(V_{DDXXX})$ is the maximum value of all the I/O supplies.
7. To sustain a voltage higher than Min(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Refer to I_{bias} in *Table 86: OPAMP characteristics* for the values of the OPAMP dedicated input leakage current.
9. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0.
4. Slow channels are: all ADC inputs except the fast channels.

Table 91. DFSDM characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)	$T_{CKIN}/2-0.5$	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	2	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	0	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0)	(CKOUT DIV+1) x $T_{DFSDMCLK}$	-	(2 x CKOUTDIV) x $T_{DFSDMCLK}$	

1. Data based on characterization results, not tested in production.

Figure 57. NAND controller waveforms for common memory write access

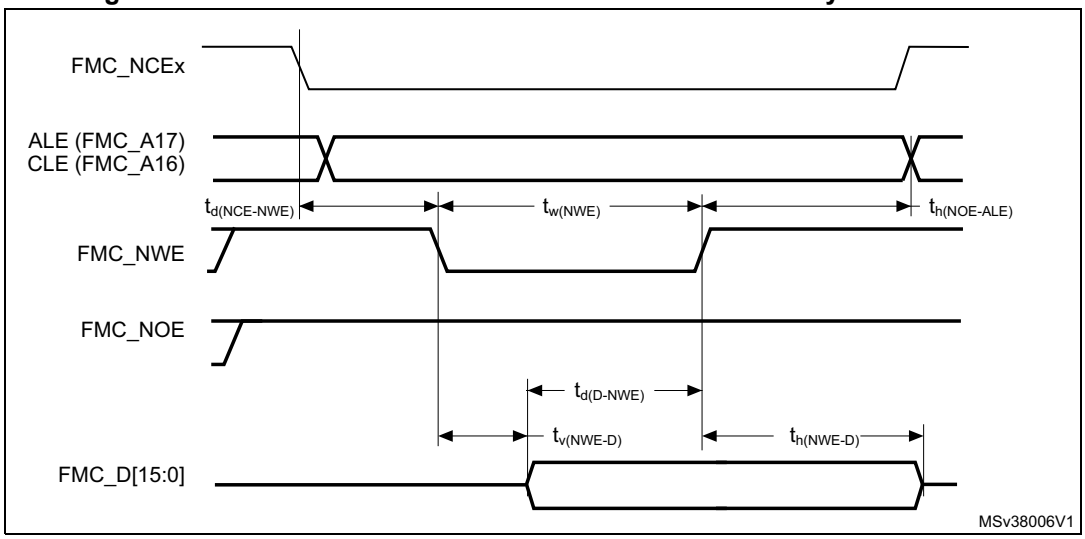


Table 117. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	12	-	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	-	$3T_{HCLK}$+1	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	$4T_{HCLK}$-2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 118. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	5	-	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{HCLK}$-1	-	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}$-1	-	
$T_{d(NCE\_NWE)}$	FMC_NCE valid before FMC_NWE low	-	$3T_{HCLK}$+1	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{HCLK}$-2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

6.3.30 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 119* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage