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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	110
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFBGA
Supplier Device Package	132-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4a6qgi6

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

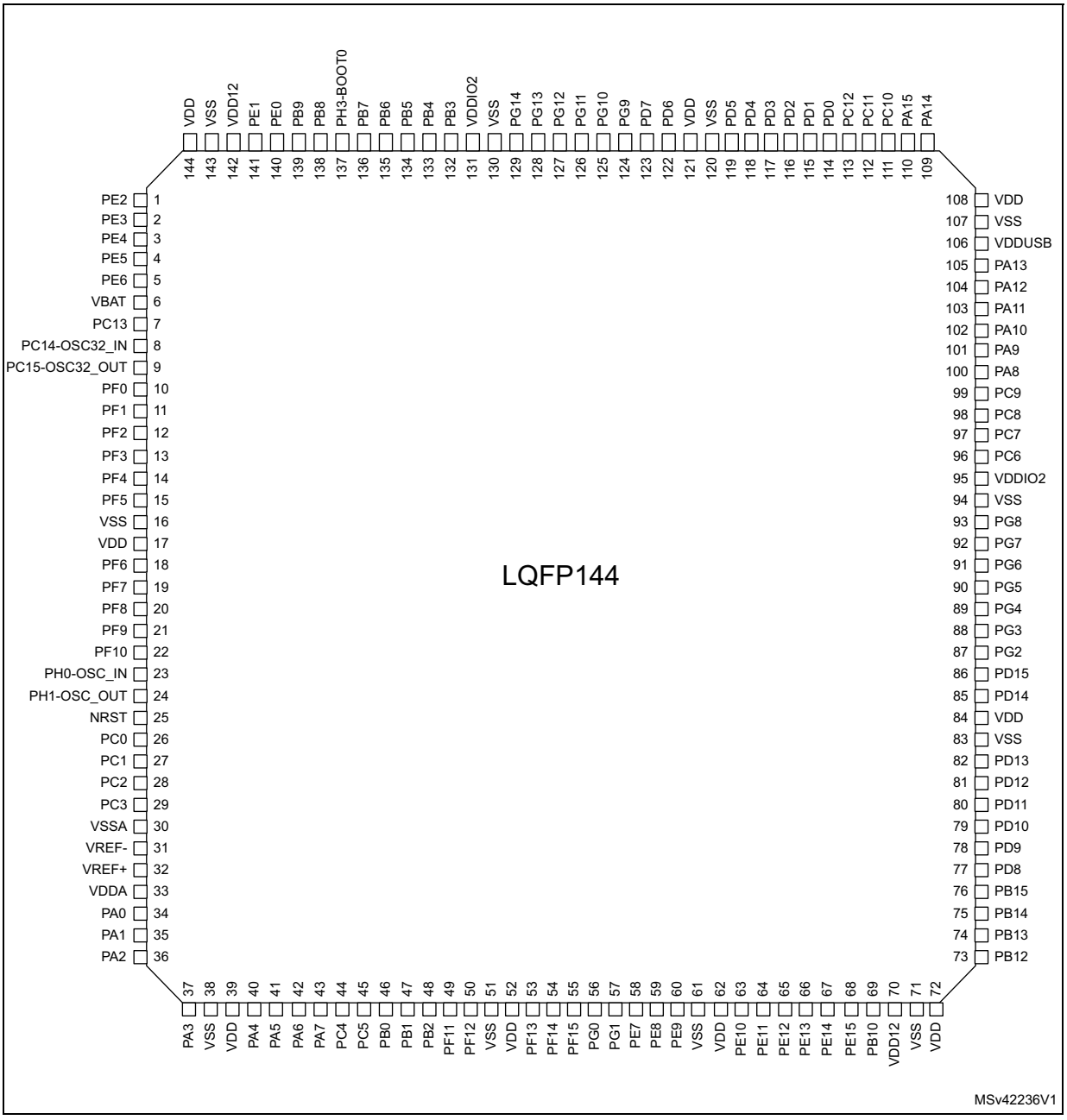
  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

Figure 10. STM32L4A6Zx, external SMPS device, LQFP144 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L4A6xG pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
30	J3	J3	48	L11	-	70	-	H8	H8	PB11	I/O	FT_fl	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG11, COMP2_OUT, EVENTOUT	-
-	-	K1	-	-	L11	-	70	-	M10	VDD12	S	-	-	-	-
-	-	-	-	-	-	-	-	K9	K9	PH4	I/O	FT_f	-	I2C2_SCL, EVENTOUT	-
-	-	-	-	-	-	-	-	L9	L9	PH5	I/O	FT_f	-	I2C2_SDA, DCMI_PIXCLK, EVENTOUT	-
-	-	-	-	-	-	-	-	N10	N10	PH8	I/O	FT_f	-	I2C3_SDA, DCMI_HSYNC, EVENTOUT	-
-	-	-	-	-	-	-	-	M9	M9	PH10	I/O	FT	-	TIM5_CH1, DCMI_D1, EVENTOUT	-
-	-	-	-	-	-	-	-	M10	-	PH11	I/O	FT	-	TIM5_CH2, DCMI_D2, EVENTOUT	-
-	-	-	-	-	-	-	-	M3	M3	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	N3	N3	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	M11	M11	VSS	S	-	-	-	-
31	K2	K2	49	F12	F12	71	71	L13	L13	VSS	S	-	-	-	-
32	K1	J2	50	G12	G12	72	72	L12	L12	VDD	S	-	-	-	-

Table 16. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	TIM5_CH2	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	DCMI_PIXCLK	SPI1_MISO	-	USART3_CTS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	SPI2_SCK	I2C1_SCL	DCMI_D0	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	I2C1_SDA	DCMI_D1	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS_ DE
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	I2C4_SMBA	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_ DE

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	QUADSPI_BK1_IO3	-	-	SAI1_SD_B	-	EVENTOUT
	PF7	-	-	QUADSPI_BK1_IO2	-	-	SAI1_MCLK_B	-	EVENTOUT
	PF8	-	-	QUADSPI_BK1_IO0	-	-	SAI1_SCK_B	-	EVENTOUT
	PF9	-	-	QUADSPI_BK1_IO1	-	-	SAI1_FS_B	TIM15_CH1	EVENTOUT
	PF10	-	-	DCMI_D11	-	-	-	TIM15_CH2	EVENTOUT
	PF11	-	-	DCMI_D12	-	-	-	-	EVENTOUT
	PF12	-	-	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	TSC_G8_IO1	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	TSC_G8_IO2	-	-	FMC_A9	-	-	EVENTOUT

Table 18. STM32L4A6xG memory map and peripheral register boundary addresses(1)

Bus	Boundary address	Size (bytes)	Peripheral
AHB4	0xA000 1000 - 0xA000 13FF	1 KB	QUADSPI
AHB3	0xA000 0400 - 0xA000 0FFF	3 KB	Reserved
	0xA000 0000 - 0xA000 03FF	1 KB	FMC
-	0x5006 0C00 - 0x5FFF FFFF	~260 MB	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5006 0400 - 0x5006 07FF	1 KB	HASH
	0x5006 0000 - 0x5006 03FF	1 KB	AES
	0x5005 0400 - 0x5005 FFFF	62 KB	Reserved
	0x5005 0000 - 0x5005 03FF	1 KB	DCMI
	0x5004 0400 - 0x5004 FFFF	62 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	OTG_FS
	0x4800 2400 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 2000 - 0x4800 23FF	1 KB	GPIOI
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 1800 - 0x4800 1BFF	1 KB	GPIOG
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 BC00 - 0x47FF FFFF	~127 MB	Reserved

Table 18. STM32L4A6xG memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB2	0x4001 0200 - 0x4001 03FF	1 KB	COMP
	0x4001 0030 - 0x4001 01FF		VREFBUF
	0x4001 0000 - 0x4001 002F		SYSCFG
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	I2C4
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC1
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	1 KB	Reserved
	0x4000 6800 - 0x4000 6BFF	1 KB	CAN2
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	CRS
	0x4000 5C00- 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4

Table 34. Typical current consumption in Run, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) and power supplied (by external SMPS (V_{DD12} = 1.05 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	f_{HCLK} = 26 MHz	Reduced code(2)	1.04	mA	40	µA/MHz
				Coremark	1.17		45	
				Dhrystone 2.1	1.22		47	
				Fibonacci	1.14		44	
				While(1)	0.96		37	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.05 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 35. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	3.1	mA	119	µA/MHz
				Coremark	2.85		110	
				Dhrystone 2.1	2.86		110	
				Fibonacci	2.63		101	
				While(1)	2.42		93.1	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	10	mA	125	µA/MHz
				Coremark	9.33		117	
				Dhrystone 2.1	9.4		118	
				Fibonacci	8.66		108	
				While(1)	8.61		108	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2 MHz all peripherals disable		Reduced code(1)	378	µA	189	µA/MHz
				Coremark	412		206	
				Dhrystone 2.1	418		209	
				Fibonacci	392		196	
				While(1)	266		133	

1. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 42. Current consumption in Sleep, Flash ON and power supplied by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions(1)		TYP					Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Sleep)	Supply current in sleep mode,	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	80 MHz	0.92	0.94	0.99	1.08	1.27	mA
			72 MHz	0.84	0.86	0.91	1.00	1.18	
			64 MHz	0.75	0.77	0.82	0.91	1.10	
			48 MHz	0.57	0.59	0.64	0.73	0.91	
			32 MHz	0.40	0.41	0.47	0.55	0.74	
			24 MHz	0.31	0.33	0.38	0.47	0.65	
			16 MHz	0.23	0.24	0.29	0.38	0.56	
			8 MHz	0.14	0.16	0.21	0.31	0.50	
			4 MHz	0.10	0.11	0.17	0.26	0.46	
			2 MHz	0.08	0.09	0.15	0.24	0.44	
			1 MHz	0.07	0.08	0.13	0.23	0.43	
			100 kHz	0.06	0.07	0.13	0.22	0.41	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V

Table 44. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI, LCD disabled	1.8 V	2.97	7.46	26.2	61.4	139	6.1	17.2	64.8	155.4	354	µA
			2.4 V	3.09	7.61	26.5	62.3	140	6.2	17.5	65.7	157.6	360	
			3 V	3.15	7.81	27	63.5	144	6.5	17.9	67.2	160.6	367	
			3.6 V	3.4	8.05	27.7	65.2	147	7.1	18.7	69.0	164.9	376	
		RTC clocked by LSI, LCD enabled(3)	1.8 V	2.98	7.31	25.5	60	135	5.5	16.8	65.1	155.8	355	
			2.4 V	3.10	7.46	25.8	60.7	137	5.8	17.1	66.3	158.2	360	
			3 V	3.23	7.63	26.4	62.1	141	6.2	17.5	67.6	161.4	367	
			3.6 V	3.47	7.95	27.1	63.6	144	6.58	18.3	69.5	165.5	376	
		RTC clocked by LSE bypassed at 32768Hz,LCD disabled	1.8 V	2.93	7.52	26.2	61.4	139	-	-	-	-	-	
			2.4 V	3.1	7.68	26.6	62.1	140	-	-	-	-	-	
			3 V	3.3	7.81	26.9	63.4	143	-	-	-	-	-	
			3.6 V	3.48	8.07	27.6	65.0	146	-	-	-	-	-	
		RTC clocked by LSE quartz(3) in low drive mode, LCD disabled	1.8 V	2.86	7.48	26.2	61.4	-	-	-	-	-	-	
			2.4 V	3.01	7.56	26.5	62.2	-	-	-	-	-	-	
			3 V	3.18	7.65	26.8	63.5	-	-	-	-	-	-	
			3.6 V	3.31	7.94	27.5	65.1	-	-	-	-	-	-	

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 56*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 56. HSE oscillator characteristics(1)

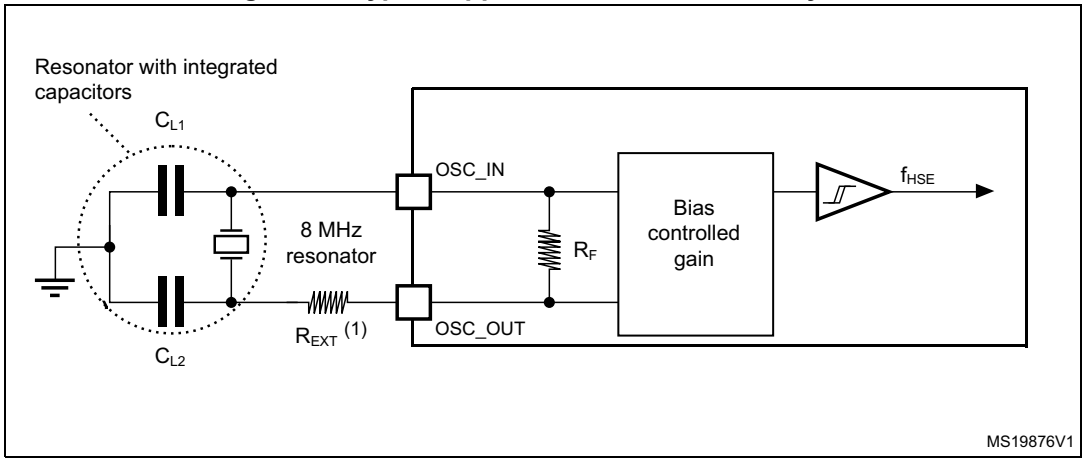
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 25*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 25. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

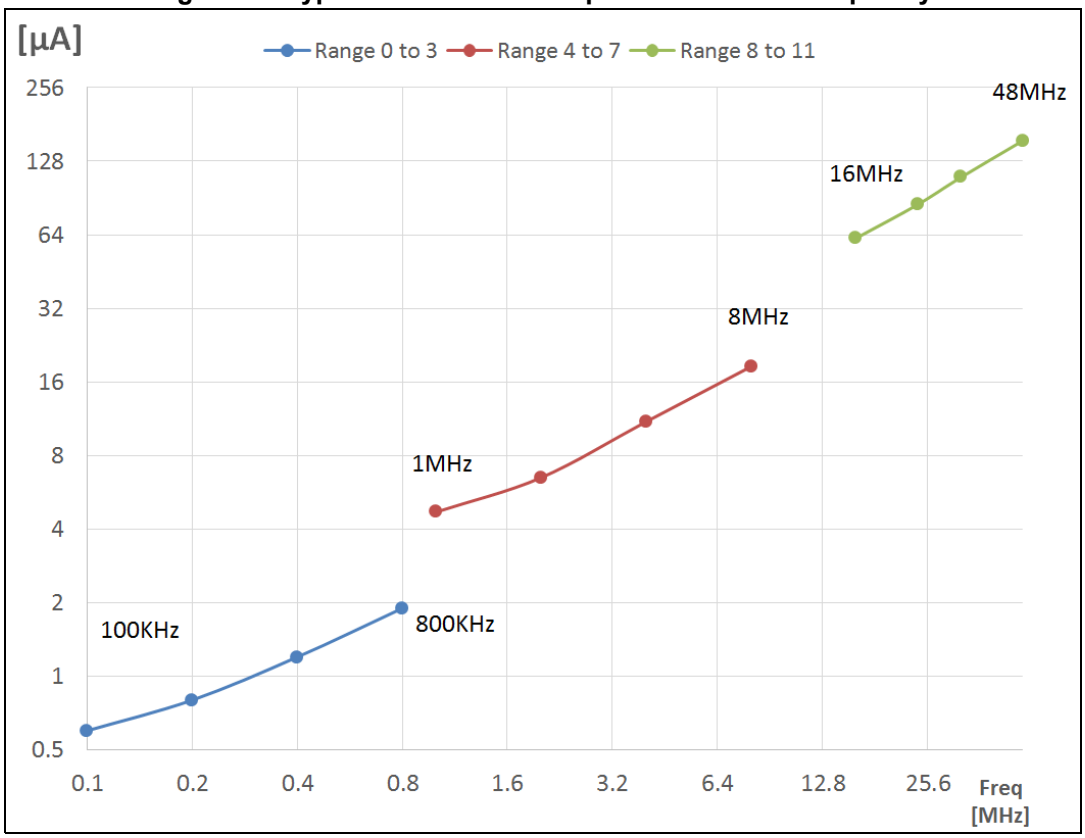
Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 57*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 57. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

Figure 28. Typical current consumption versus MSI frequency



High-speed internal 48 MHz (HSI48) RC oscillator

Table 60. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0V, T_A=30°C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	%
DuCy(HSI48)	Duty Cycle	-	45(2)	-	55(2)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA

6.3.19 Digital-to-Analog converter characteristics

Table 82. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF (no resistive load on DAC1_OUTx pin or internal connection)		1.71	-	3.6	V
		Other modes		1.80	-		
V_{REF+}	Positive reference voltage	DAC output buffer OFF (no resistive load on DAC1_OUTx pin or internal connection)		1.71	-	V_{DDA}	
		Other modes		1.80	-		
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC1_OUTx output	DAC output buffer ON		0.2	-	V_{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC1_OUTx reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

Table 83. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

Table 84. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

Table 98. QUADSPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 V < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1		-	-	40	MHz
		2 V < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1		-	-	48	
		1.71 V < V_{DD} < 3.6 V, C_{LOAD} = 15 pF Voltage Range 1		-	-	48	
		1.71 V < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2		-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK} = 48 MHz, presc= 1		$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$				$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	
$t_{sf(IN)}$;$t_{sr(IN)}$	Data input setup time	Voltage Range 1 and 2		3.5	-	-	
$t_{hf(IN)}$; $t_{hr(IN)}$	Data input hold time			6.5	-	-	
$t_{vr(OUT)}$	Data output valid time on rise edge	Voltage Range 1	DHHC = 0	-	4.5	5.5	
			DHHC = 1		$t_{(CK)}/2+1$	$t_{(CK)}/2+1.5$	
		Voltage Range 2			9.5	14	
$t_{vf(OUT)}$	Data output valid time on falling edge	Voltage Range 1	DHHC = 0	-	5	6	
			DHHC = 1		$t_{(CK)}/2+1$	$t_{(CK)}/2+1.5$	
		Voltage Range 2			15	18	
$t_{hr(OUT)}$	Data output hold time on rise edge	Voltage Range 1	DHHC = 0	4	-	-	
			DHHC = 1	$t_{(CK)}/2+0.5$	-	-	
		Voltage Range 2		8	-	-	
$t_{hf(OUT)}$	Data output hold time on falling edge	Voltage Range 1	DHHC = 0	3.5	-	-	
			DHHC = 1	$t_{(CK)}/2+0.5$	-	-	
		Voltage Range 2		13		-	

1. Guaranteed by characterization results.

Table 105. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK}$-1	$2T_{HCLK}$+1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}$-1	$2T_{HCLK}$+1	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	T_{HCLK}-1	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	T_{HCLK}-1	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+1	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 106. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{HCLK}$-1	$7T_{HCLK}$+1	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK}$-1	$5T_{HCLK}$+1	
$t_{w(NWAIT)}$	FMC_NWAIT low time	T_{HCLK}-0.5	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}$+1.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$+1	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

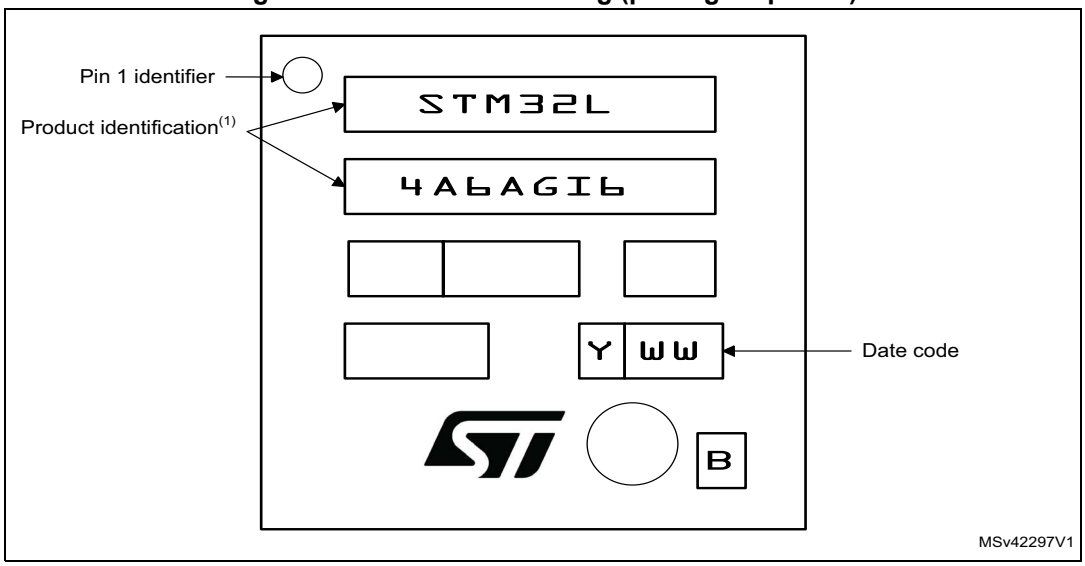
Note: 4 to 6 mils solder paste screen printing process.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 63. UFBGA169 marking (package top view)



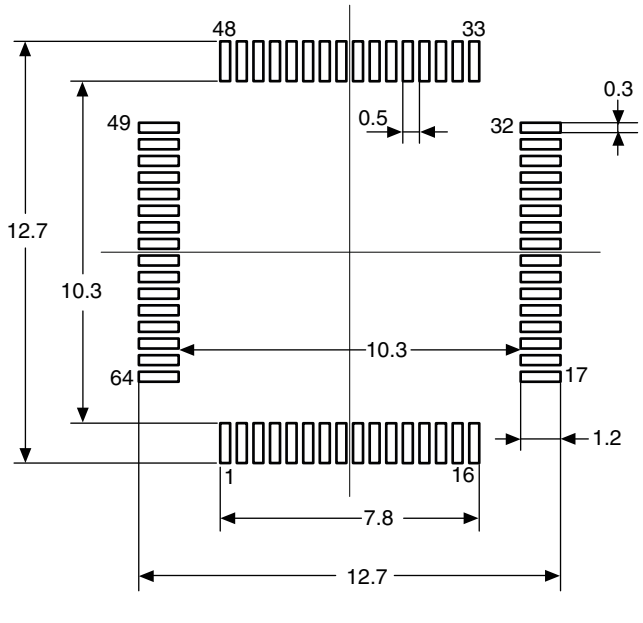
1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Table 131. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 81. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.