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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I <sup>2</sup> C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	83
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA, WLCSP
Supplier Device Package	100-WLCSP (4.62x4.14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4a6vgy6tr">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4a6vgy6tr</a>

## 3 Functional overview

### 3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32L4A6xG family is compatible with all Arm® tools and software.

*Figure 1* shows the general block diagram of the STM32L4A6xG family devices.

### 3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

### 3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application. Low frequency clocks (LSI, LSE) are available down to Stop 1 low power state.
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes down to Standby mode. LSE can also be output on LSCO in Shutdown mode. LSCO is not available in VBAT mode.

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 80 MHz.

### LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

## 3.42 Dual-flash Quad SPI memory interface (QUADSPI)

The Dual-flash Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory

Both throughput and capacity can be increased two-fold using dual-flash mode, where two Quad SPI flash memories are accessed simultaneously.

The Dual-flash Quad SPI interface supports:

- Three functional modes: indirect, status-polling, and memory-mapped
- Dual-flash mode, where 8 bits can be sent/received simultaneously by accessing two flash memories in parallel.
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error



Table 15. STM32L4A6xG pin definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	H3	G3	55	K9	K9	77	77	L11	L11	PD8	I/O	FT_I	-	USART3_TX, DCM1_HSYNC, LCD_SEG28, FMC_D13, EVENTOUT	-
-	G2	G2	56	K8	K8	78	78	L10	L10	PD9	I/O	FT_I	-	USART3_RX, DCM1_PIXCLK, LCD_SEG29, FMC_D14, SAI2_MCLK_A, EVENTOUT	-
-	G1	G1	57	J12	J12	79	79	J13	J13	PD10	I/O	FT_I	-	USART3_CK, TSC_G6_IO1, LCD_SEG30, FMC_D15, SAI2_SCK_A, EVENTOUT	-
-	-	-	58	J11	J11	80	80	K12	K12	PD11	I/O	FT_I	-	I2C4_SMBA, USART3_CTS, TSC_G6_IO2, LCD_SEG31, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	-
-	-	-	59	J10	J10	81	81	K11	K11	PD12	I/O	FT_fl	-	TIM4_CH1, I2C4_SCL, USART3_RTS_DE, TSC_G6_IO3, LCD_SEG32, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	-
-	-	-	60	H12	H12	82	82	K13	K13	PD13	I/O	FT_fl	-	TIM4_CH2, I2C4_SDA, TSC_G6_IO4, LCD_SEG33, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	-	-	83	83	H12	H12	VSS	S	-	-	-	-
-	F1	F1	-	-	-	84	84	H13	H13	VDD	S	-	-	-	-
-	G3	F3	61	H11	H11	85	85	K10	K10	PD14	I/O	FT_I	-	TIM4_CH3, LCD_SEG34, FMC_D0, EVENTOUT	-

Table 17. Alternate function AF8 to AF15<sup>(1)</sup> (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/FM C/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port B	PB0	-	-	QUADSPI_BK1_IO1	LCD_SEG5	COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_RT S_DE	-	QUADSPI_BK1_IO0	LCD_SEG6	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	-	LCD_VLCD	-	-	-	EVENTOUT
	PB3	-	-	OTG_FS_CRG_SYNC	LCD_SEG7	-	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS_ DE	TSC_G2_IO1	DCMI_D12	LCD_SEG8	-	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	DCMI_D10	LCD_SEG9	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	CAN2_TX	TSC_G2_IO3	DCMI_D5	-	TIM8_BKIN2_ COMP2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	DCMI_VSYNC	LCD_SEG21	FMC_NL	TIM8_BKIN_C OMP1	TIM17_CH1N	EVENTOUT
	PB8	-	CAN1_RX	DCMI_D6	LCD_SEG16	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	-	CAN1_TX	DCMI_D7	LCD_COM3	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	QUADSPI_CLK	LCD_SEG10	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	QUADSPI_BK1_NCS	LCD_SEG11	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RT S_DE	TSC_G1_IO1	CAN2_RX	LCD_SEG12	SWPMI1_IO	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CT S	TSC_G1_IO2	CAN2_TX	LCD_SEG13	SWPMI1_TX	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	LCD_SEG14	SWPMI1_RX	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	LCD_SEG15	SWPMI1_SUS PEND	SAI2_SD_A	TIM15_CH2	EVENTOUT

Table 17. Alternate function AF8 to AF15<sup>(1)</sup> (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/FM C/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT
	PH4	-	-	-	-	-	-	-	EVENTOUT
	PH5	-	-	DCMI_PIXCLK	-	-	-	-	EVENTOUT
	PH6	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PH7	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PH8	-	-	DCMI_HSYNC	-	-	-	-	EVENTOUT
	PH9	-	-	DCMI_D0	-	-	-	-	EVENTOUT
	PH10	-	-	DCMI_D1	-	-	-	-	EVENTOUT
	PH11	-	-	DCMI_D2	-	-	-	-	EVENTOUT
	PH12	-	-	DCMI_D3	-	-	-	-	EVENTOUT
	PH13	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	-	DCMI_D4	-	-	-	-	EVENTOUT
	PH15	-	-	DCMI_D11	-	-	-	-	EVENTOUT

Table 18. STM32L4A6xG memory map and peripheral register boundary addresses<sup>(1)</sup>

Bus	Boundary address	Size (bytes)	Peripheral
AHB4	0xA000 1000 - 0xA000 13FF	1 KB	QUADSPI
AHB3	0xA000 0400 - 0xA000 0FFF	3 KB	Reserved
	0xA000 0000 - 0xA000 03FF	1 KB	FMC
-	0x5006 0C00 - 0x5FFF FFFF	~260 MB	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5006 0400 - 0x5006 07FF	1 KB	HASH
	0x5006 0000 - 0x5006 03FF	1 KB	AES
	0x5005 0400 - 0x5005 FFFF	62 KB	Reserved
	0x5005 0000 - 0x5005 03FF	1 KB	DCMI
	0x5004 0400 - 0x5004 FFFF	62 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	OTG_FS
	0x4800 2400 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 2000 - 0x4800 23FF	1 KB	GPIOI
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 1800 - 0x4800 1BFF	1 KB	GPIOG
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 BC00 - 0x47FF FFFF	~127 MB	Reserved



Table 18. STM32L4A6xG memory map and peripheral register boundary addresses<sup>(1)</sup> (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB2	0x4001 0200 - 0x4001 03FF	1 KB	COMP
	0x4001 0030 - 0x4001 01FF		VREFBUF
	0x4001 0000 - 0x4001 002F		SYSCFG
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	I2C4
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC1
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	1 KB	Reserved
	0x4000 6800 - 0x4000 6BFF	1 KB	CAN2
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	CRS
	0x4000 5C00 - 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4

Table 24. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Unit
V <sub>PVD1</sub>	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	
V <sub>PVD2</sub>	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V <sub>PVD3</sub>	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V <sub>PVD4</sub>	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V <sub>PVD5</sub>	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V <sub>PVD6</sub>	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V <sub>hyst_BORH0</sub>	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
V <sub>hyst_BOR_PVD</sub>	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I <sub>DD</sub> (BOR_PVD) <sup>(2)</sup>	BOR <sup>(3)</sup> (except BOR0) and PVD consumption from V <sub>DD</sub>	-	-	1.1	1.6	μA
V <sub>PVM1</sub>	V <sub>DDUSB</sub> peripheral voltage monitoring	-	1.18	1.22	1.26	V
V <sub>PVM3</sub>	V <sub>DDA</sub> peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V <sub>PVM4</sub>	V <sub>DDA</sub> peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V <sub>hyst_PVM3</sub>	PVM3 hysteresis	-	-	10	-	mV
V <sub>hyst_PVM4</sub>	PVM4 hysteresis	-	-	10	-	mV
I <sub>DD</sub> (PVM1/PVM2) <sup>(2)</sup>	PVM1 and PVM2 consumption from V <sub>DD</sub>	-	-	0.2	-	μA
I <sub>DD</sub> (PVM3/PVM4) <sup>(2)</sup>	PVM3 and PVM4 consumption from V <sub>DD</sub>	-	-	2	-	μA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

2. Guaranteed by design.

3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

**Table 32. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)**

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
$I_{DD\_ALL}$ (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 $f_{HCLK} = 26$ MHz	Reduced code <sup>(1)</sup>	2.65	mA	102	$\mu A/MHz$
				Coremark	2.97		114	
				Dhrystone 2.1	3.1		119	
				Fibonacci	2.9		112	
				While(1)	2.43		93	
			Range 1 $f_{HCLK} = 80$ MHz	Reduced code <sup>(1)</sup>	9.44	mA	118	$\mu A/MHz$
				Coremark	10.6		133	
				Dhrystone 2.1	10.9		136	
				Fibonacci	10.3		129	
				While(1)	8.66		108	
$I_{DD\_ALL}$ (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI} = 2$ MHz all peripherals disable		Reduced code <sup>(1)</sup>	274	$\mu A$	137	$\mu A/MHz$
				Coremark	307		154	
				Dhrystone 2.1	308		154	
				Fibonacci	273		137	
				While(1)	258		129	

1. Reduced code used for characterization results provided in [Table 26](#), [Table 28](#), [Table 30](#).

**Table 33. Typical current consumption in Run, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) and power supplied (by external SMPS ( $V_{DD12} = 1.10$  V))**

Symbol	Parameter	Conditions <sup>(1)</sup>			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
$I_{DD\_ALL}$ (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	$f_{HCLK} = 26$ MHz	Reduced code <sup>(2)</sup>	1.14	mA	44	$\mu A/MHz$
				Coremark	1.28		49	
				Dhrystone 2.1	1.34		51	
				Fibonacci	1.25		48	
				While(1)	1.05		40	
			$f_{HCLK} = 80$ MHz	Reduced code <sup>(2)</sup>	3.39		42	
				Coremark	3.81		48	
				Dhrystone 2.1	3.92		49	
				Fibonacci	3.70		46	
				While(1)	3.11		39	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters:  
SMPS input = 3.3 V, SMPS efficiency = 85%,  $V_{DD12} = 1.10$  V

2. Reduced code used for characterization results provided in [Table 26](#), [Table 28](#), [Table 30](#).

Table 47. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX <sup>(1)</sup>					Unit
		-	V <sub>DD</sub>	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I <sub>DD_ALL</sub> (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	no independent watchdog	1.8 V	108	299	1343	3822	10353	227	899	4159	13059	36572	nA
			2.4 V	118	348	1562	4447	12012	252	1009	4846	15026	41366	
			3 V	133	404	1777	5071	13589	318	1211	6082	17245	46714	
			3.6 V	171	501	2115	5898	15539	435	1508	7230	19850	52888 <sup>(2)</sup>	
		with independent watchdog	1.8 V	296	-	-	-	-	-	-	-	-	-	
			2.4 V	349	-	-	-	-	-	-	-	-	-	
			3 V	411	-	-	-	-	-	-	-	-	-	
			3.6 V	506	-	-	-	-	-	-	-	-	-	
I <sub>DD_ALL</sub> (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	377	581	1700	4270	11100	763	1422	5182	13585	36564	nA
			2.4 V	461	700	2020	5030	12900	942	1704	5992	15473	41383	
			3 V	559	843	2390	5990	15500	1166	2032	6938	17889	46728	
			3.6 V	689	1050	2920	7130	18100	1454	2511	7754	20714	53018	
		RTC clocked by LSI, with independent watchdog	1.8 V	422	-	-	-	-	-	-	-	-	-	
			2.4 V	518	-	-	-	-	-	-	-	-	-	
			3 V	560	-	-	-	-	-	-	-	-	-	
			3.6 V	780	-	-	-	-	-	-	-	-	-	

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 50](#). The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in [Table 19: Voltage characteristics](#)
- The power consumption of the digital part of the on-chip peripherals is given in [Table 50](#). The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 50. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB2	All APB2 on	55.40	41.33	46.00	μA/MHz
ALL		234.98	195.83	235.70	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The GPIOx (x= A...I) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx\_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).
3. The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.
4. The AHB to APB2 Bridge is automatically active when at least one peripheral is ON on the APB2.

### 6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in [Table 51](#) are the latency between the event and the execution of the first user instruction.

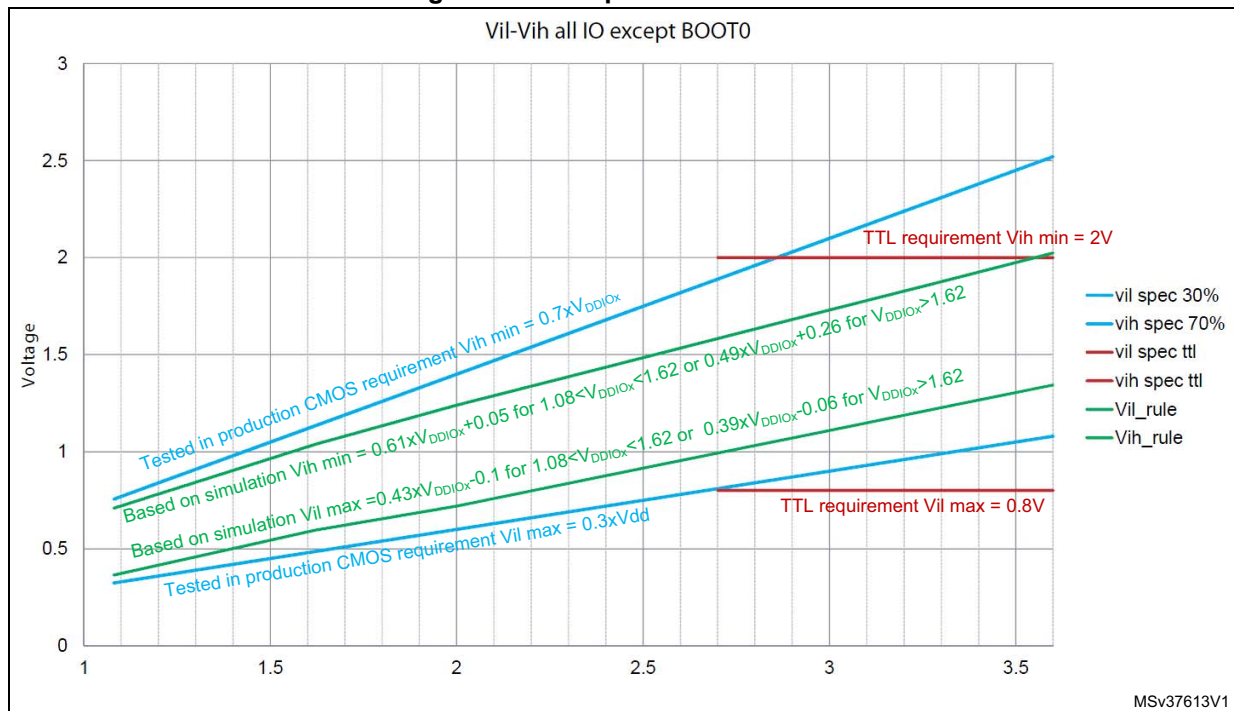
The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 51. Low-power mode wakeup timings<sup>(1)</sup>

Symbol	Parameter	Conditions		Typ	Max	Unit
t <sub>WUSLEEP</sub>	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
t <sub>WULPSLEEP</sub>	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		7	9	
t <sub>WUSTOP0</sub>	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	7.0	11.6	μs
			Wakeup clock HSI16 = 16 MHz	6.2	10.7	
		Range 2	Wakeup clock MSI = 24 MHz	7.3	11.7	
			Wakeup clock HSI16 = 16 MHz	6.2	10.7	
			Wakeup clock MSI = 4 MHz	7.6	13.2	
			Wakeup clock MSI = 4 MHz	7.6	13.2	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	2.5	2.9	
			Wakeup clock HSI16 = 16 MHz	2.7	2.9	
		Range 2	Wakeup clock MSI = 24 MHz	3.2	3.6	
			Wakeup clock HSI16 = 16 MHz	2.7	2.9	
			Wakeup clock MSI = 4 MHz	5.7	13.2	
			Wakeup clock MSI = 4 MHz	5.7	13.2	

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 30](#) for standard I/Os, and in [Figure 30](#) for 5 V tolerant I/Os.

**Figure 30. I/O input characteristics**



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to  $\pm 8$  mA, and sink or source up to  $\pm 20$  mA (with a relaxed  $V_{OL}/V_{OH}$ ).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on  $V_{DDIOX}$ , plus the maximum consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VDD}$  (see [Table 19: Voltage characteristics](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$ , plus the maximum consumption of the MCU sunk on  $V_{SS}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VSS}$  (see [Table 19: Voltage characteristics](#)).

Table 78. ADC accuracy - limited test conditions 1<sup>(1)</sup>(2)(3)

Sym- bol	Parameter	Conditions <sup>(4)</sup>		Min	Typ	Max	Unit
ET	Total unadjusted error	Single ended	Fast channel (max speed)	-	4	5	LSB
			Slow channel (max speed)	-	4	5	
		Differential	Fast channel (max speed)	-	3.5	4.5	
			Slow channel (max speed)	-	3.5	4.5	
EO	Offset error	Single ended	Fast channel (max speed)	-	1	2.5	
			Slow channel (max speed)	-	1	2.5	
		Differential	Fast channel (max speed)	-	1.5	2.5	
			Slow channel (max speed)	-	1.5	2.5	
EG	Gain error	Single ended	Fast channel (max speed)	-	2.5	4.5	
			Slow channel (max speed)	-	2.5	4.5	
		Differential	Fast channel (max speed)	-	2.5	3.5	
			Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error	Single ended	Fast channel (max speed)	-	1	1.5	
			Slow channel (max speed)	-	1	1.5	
		Differential	Fast channel (max speed)	-	1	1.2	
			Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error	Single ended	Fast channel (max speed)	-	1.5	2.5	
			Slow channel (max speed)	-	1.5	2.5	
		Differential	Fast channel (max speed)	-	1	2	
			Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits	Single ended	Fast channel (max speed)	10.4	10.5	-	bits
			Slow channel (max speed)	10.4	10.5	-	
		Differential	Fast channel (max speed)	10.8	10.9	-	
			Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio	Single ended	Fast channel (max speed)	64.4	65	-	dB
			Slow channel (max speed)	64.4	65	-	
		Differential	Fast channel (max speed)	66.8	67.4	-	
			Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio	Single ended	Fast channel (max speed)	65	66	-	
			Slow channel (max speed)	65	66	-	
		Differential	Fast channel (max speed)	67	68	-	
			Slow channel (max speed)	67	68	-	



## 6.3.20 Voltage reference buffer characteristics

Table 84. VREFBUF characteristics<sup>(1)</sup>

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DDA}$	Analog supply voltage	Normal mode	$V_{RS} = 0$	2.4	-	3.6	V
			$V_{RS} = 1$	2.8	-	3.6	
		Degraded mode <sup>(2)</sup>	$V_{RS} = 0$	1.65	-	2.4	
			$V_{RS} = 1$	1.65	-	2.8	
$V_{REFBUF\_OUT}$	Voltage reference output	Normal mode	$V_{RS} = 0$	2.046 <sup>(3)</sup>	2.048	2.049 <sup>(3)</sup>	V
			$V_{RS} = 1$	2.498 <sup>(3)</sup>	2.5	2.502 <sup>(3)</sup>	
		Degraded mode <sup>(2)</sup>	$V_{RS} = 0$	$V_{DDA} - 150 \text{ mV}$	-	$V_{DDA}$	
			$V_{RS} = 1$	$V_{DDA} - 150 \text{ mV}$	-	$V_{DDA}$	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent Serial Resistor of Cloud	-	-	-	-	2	Ω
$I_{load}$	Static load current	-	-	-	-	4	mA
$I_{line\_reg}$	Line regulation	$2.8 \text{ V} \leq V_{DDA} \leq 3.6 \text{ V}$	$I_{load} = 500 \text{ µA}$	-	200	1000	ppm/V
			$I_{load} = 4 \text{ mA}$	-	100	500	
$I_{load\_reg}$	Load regulation	$500 \text{ µA} \leq I_{load} \leq 4 \text{ mA}$	Normal mode	-	50	500	ppm/mA
$T_{Coeff}$	Temperature coefficient	$-40 \text{ °C} < T_J < +125 \text{ °C}$		-	-	$T_{coeff\_vrefint} + 50$	ppm/ °C
		$0 \text{ °C} < T_J < +50 \text{ °C}$		-	-	$T_{coeff\_vrefint} + 50$	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
$t_{START}$	Start-up time	$CL = 0.5 \text{ µF}^{(4)}$		-	300	350	µs
		$CL = 1.1 \text{ µF}^{(4)}$		-	500	650	
		$CL = 1.5 \text{ µF}^{(4)}$		-	650	800	
$I_{INRUSH}$	Control of maximum DC current drive on VREFBUF_OUT during start-up phase <sup>(5)</sup>	-	-	-	8	-	mA

Table 98. QUADSPI characteristics in DDR mode<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{CK}$ $1/t_{(CK)}$	Quad SPI clock frequency	$1.71\text{ V} < V_{DD} < 3.6\text{ V}$ , $C_{LOAD} = 20\text{ pF}$ Voltage Range 1	-	-	40	MHz
		$2\text{ V} < V_{DD} < 3.6\text{ V}$ , $C_{LOAD} = 20\text{ pF}$ Voltage Range 1	-	-	48	
		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$ , $C_{LOAD} = 15\text{ pF}$ Voltage Range 1	-	-	48	
		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$ $C_{LOAD} = 20\text{ pF}$ Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	$f_{AHBCLK} = 48\text{ MHz}$ , presc= 1	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$			$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	
$t_{sf(IN)}; t_{sr(IN)}$	Data input setup time	Voltage Range 1 and 2	3.5	-	-	
$t_{hf(IN)}; t_{hr(IN)}$	Data input hold time		6.5	-	-	
$t_{vr(OUT)}$	Data output valid time on rise edge	Voltage Range 1	-	DHHC = 0	4.5	5.5
				DHHC = 1	$t_{(CK)}/2+1$	$t_{(CK)}/2+1.5$
		Voltage Range 2			9.5	14
$t_{vf(OUT)}$	Data output valid time on falling edge	Voltage Range 1	-	DHHC = 0	5	6
				DHHC = 1	$t_{(CK)}/2+1$	$t_{(CK)}/2+1.5$
		Voltage Range 2			15	18
$t_{hr(OUT)}$	Data output hold time on rise edge	Voltage Range 1	DHHC = 0	4	-	-
			DHHC = 1	$t_{(CK)}/2+0.5$	-	-
		Voltage Range 2		8	-	-
$t_{hf(OUT)}$	Data output hold time on falling edge	Voltage Range 1	DHHC = 0	3.5	-	-
			DHHC = 1	$t_{(CK)}/2+0.5$	-	-
		Voltage Range 2		13	-	-

1. Guaranteed by characterization results.

Figure 39. Quad SPI timing diagram - SDR mode

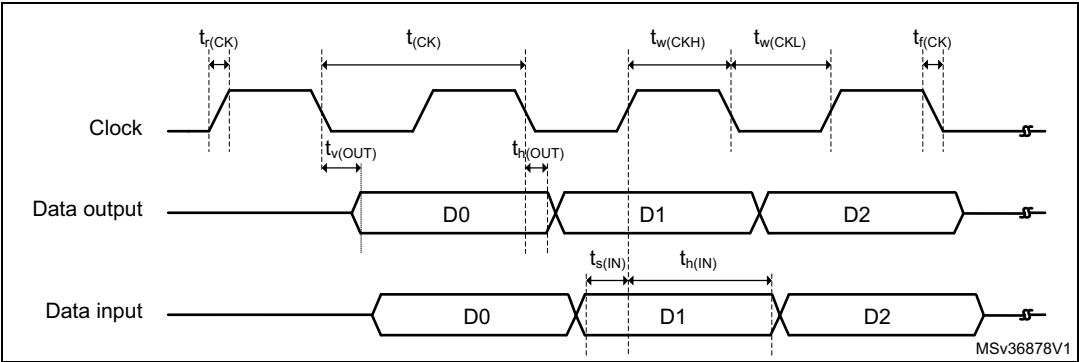
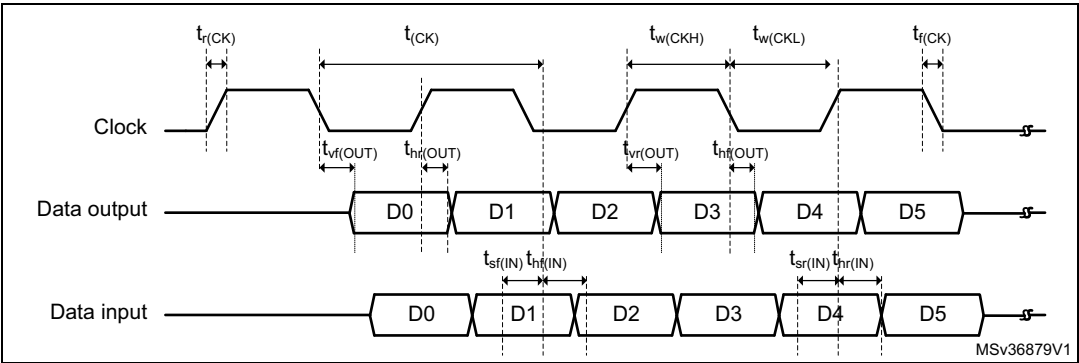


Figure 40. Quad SPI timing diagram - DDR mode



**Table 105. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK}-1$	$2T_{HCLK}+1$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}-1$	$2T_{HCLK}+1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK}-1$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	$T_{HCLK}-1$	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK}+1$	

1. CL = 30 pF.

2. Guaranteed by characterization results.

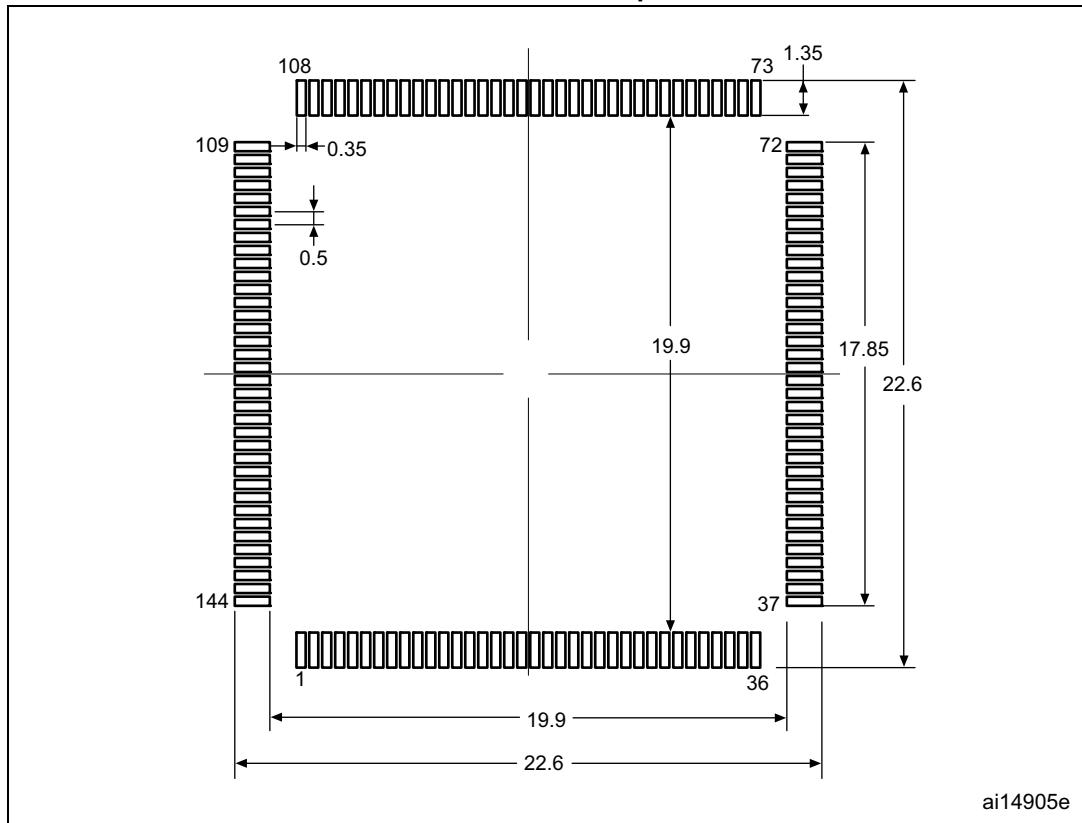
**Table 106. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{HCLK}-1$	$7T_{HCLK}+1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK}-1$	$5T_{HCLK}+1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{HCLK}-0.5$	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}+1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$	-	

1. CL = 30 pF.

2. Guaranteed by characterization results.

**Figure 66. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint**



1. Dimensions are expressed in millimeters.