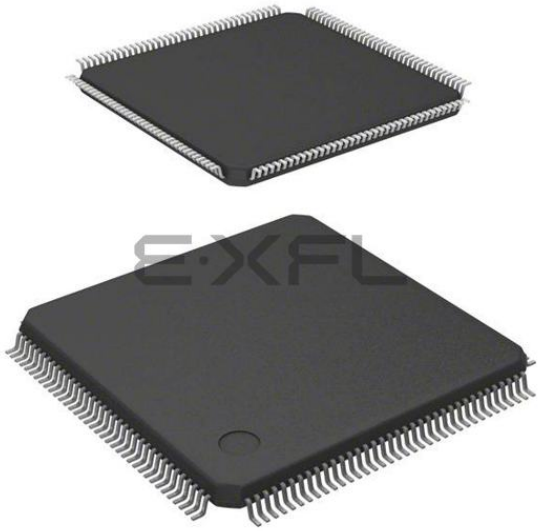

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	115
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4a6zgt6p

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Table 5. Functionalities depending on the working mode[1]

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (1 MB)	O[2]	O[2]	O[2]	O[2]	-	-	-	-	-	-	-	-	-
SRAM1 (256 KB)	Y	Y[3]	Y	Y[3]	Y	-	Y	-	-	-	-	-	-
SRAM2 (64 KB)	Y	Y[3]	Y	Y[3]	Y	-	Y	-	O[4]	-	-	-	-
FSMC	O	O	O	O	-	-	-	-	-	-	-	-	-
Quad SPI	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup Registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brown-out reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral Voltage Monitor (PVMx; x=1,2,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
DMA2D	O	O	O	O	-	-	-	-	-	-	-	-	-
High Speed Internal (HSI16)	O	O	O	O	[5]	-	[5]	-	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-	-	-	-
High Speed External (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low Speed Internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low Speed External (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi-Speed Internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock Security System (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock Security System on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O

3.20 Comparators (COMP)

The STM32L4A6xG devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.21 Operational amplifier (OPAMP)

The STM32L4A6xG embeds two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.22 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

3.33 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

Figure 11. STM32L4A6Qx UFBGA132 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3-BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5	PG14	PG13	PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSS		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO2		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	PB11	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

MSv38035V3

1. The above figure shows the package top view.

Figure 12. STM32L4A6Qx, external SMPS device, UFBGA132 ballout

	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3-BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5	VDD12	PG13	PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSS		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO2		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	VDD12	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

MS46960V1

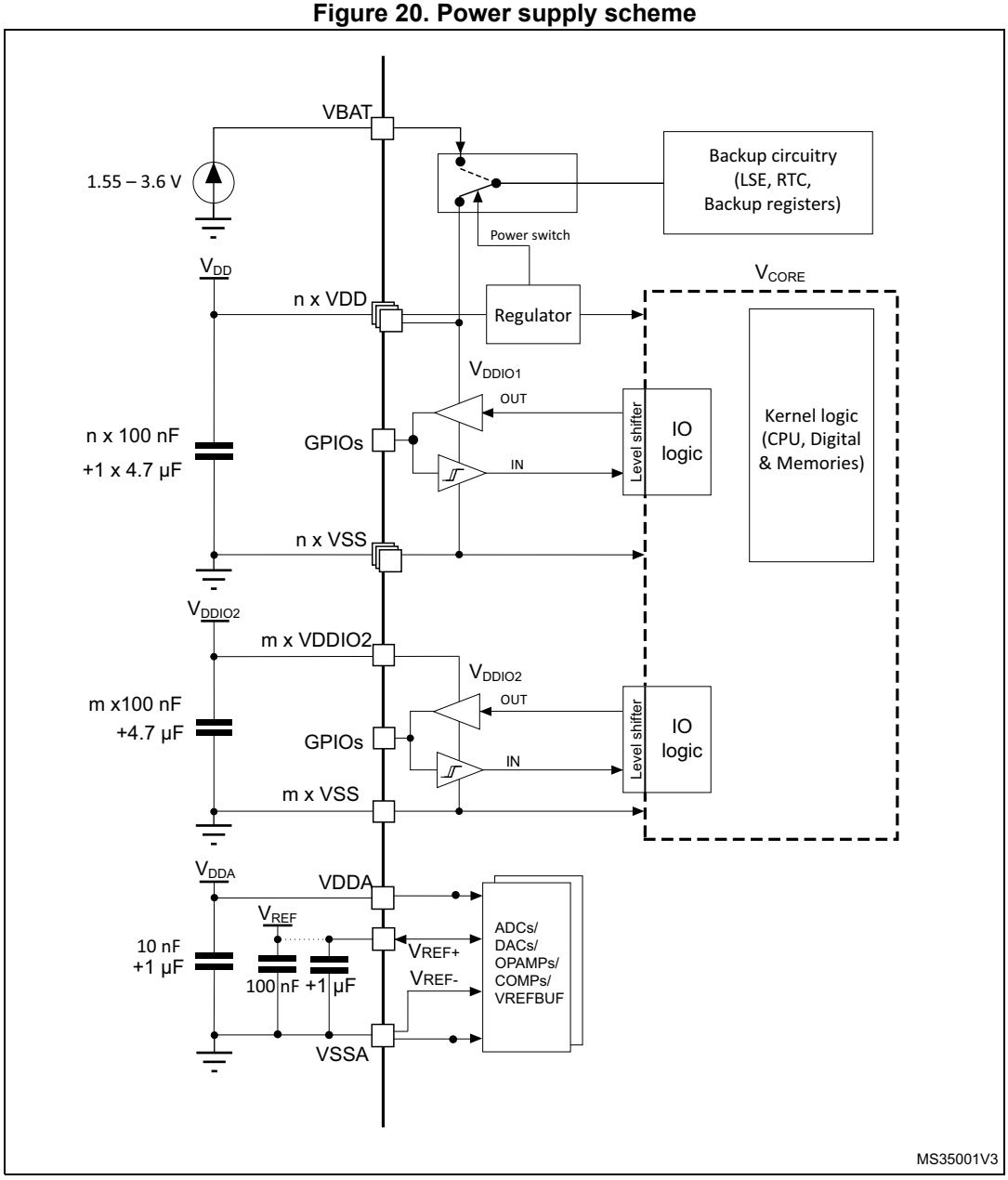
1. The above figure shows the package top view.

Table 16. Alternate function AF0 to AF7[(1)]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	TIM5_CH2	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	DCMI_PIXCLK	SPI1_MISO	-	USART3_CTS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	SPI2_SCK	I2C1_SCL	DCMI_D0	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	I2C1_SDA	DCMI_D1	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS_ DE
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	I2C4_SMBA	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_ DE

6.1.6 Power supply scheme

Figure 20. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 27. Current consumption in Run modes, code with data processing running from Flash, (ART enable Cache ON Prefetch OFF) and power supplied (by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions[1]		TYP					Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	80 MHz	3.39	3.42	3.48	3.57	3.74	mA
			72 MHz	3.06	3.09	3.15	3.24	3.43	
			64 MHz	2.74	2.76	2.81	2.91	3.10	
			48 MHz	2.06	2.08	2.14	2.23	2.42	
			32 MHz	1.39	1.41	1.46	1.56	1.74	
			24 MHz	1.06	1.07	1.13	1.22	1.40	
			16 MHz	0.72	0.74	0.79	0.88	1.06	
			8 MHz	0.39	0.41	0.46	0.56	0.75	
			4 MHz	0.22	0.24	0.29	0.39	0.58	
			2 MHz	0.14	0.16	0.21	0.30	0.50	
			1 MHz	0.10	0.11	0.16	0.26	0.46	
			100 kHz	0.06	0.07	0.13	0.22	0.42	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V

Table 28. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable

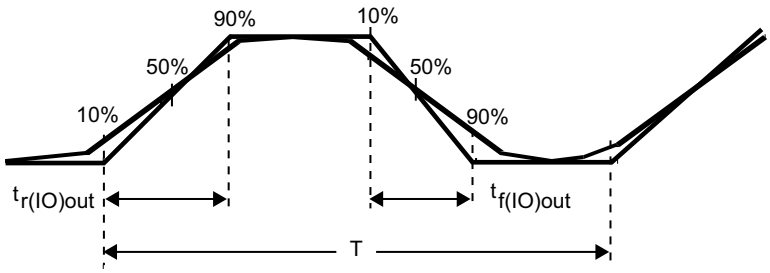
Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.1	3.14	3.28	3.51	3.98	3.5	3.6	3.8	4.3	5.3	mA
				16 MHz	2.19	2.23	2.36	2.59	3.05	2.5	2.6	2.8	3.3	4.3	
				8 MHz	1.22	1.26	1.39	1.61	2.07	1.4	1.5	1.7	2.2	3.2	
				4 MHz	0.69	0.73	0.85	1.08	1.53	0.8	0.9	1.1	1.6	2.6	
				2 MHz	0.41	0.44	0.57	0.79	1.24	0.5	0.6	0.8	1.3	2.3	
				1 MHz	0.27	0.3	0.43	0.65	1.1	0.3	0.4	0.6	1.1	2.1	
				100 kHz	0.14	0.18	0.3	0.52	0.97	0.2	0.3	0.5	1.0	2.0	
			Range 1	80 MHz	10	10.1	10.3	10.5	11.1	11.1	11.2	11.6	12.2	13.31	
				72 MHz	9.02	9.1	9.29	9.59	10.1	10	10.1	10.5	11.0	12.2	
				64 MHz	8.94	9.02	9.2	9.48	10	9.9	10.1	10.4	11.0	12.1	
				48 MHz	7.51	7.59	7.77	8.05	8.59	8.4	8.6	8.9	9.5	10.6	
				32 MHz	5.38	5.45	5.62	5.88	6.41	6.0	6.2	6.5	7.0	8.2	
				24 MHz	4.07	4.12	4.28	4.54	5.06	4.5	4.7	5.0	5.5	6.6	
				16 MHz	2.86	2.92	3.07	3.33	3.84	3.2	3.3	3.6	4.2	5.3	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	378	412	549	782	1260	436	538	761	1287	2317	µA
				1 MHz	213	246	381	618	1100	255	367	609.	1105	2138	
				400 kHz	101	144	277	514	989	141	256	507	995	2033	
				100 kHz	62	95.8	228	463	939	85	201	454	947	1982	

1. Guaranteed by characterization results, unless otherwise specified.

Table 45. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	LCD disabled	1.8 V	11.2	30.7	107	243	523	25.4	79.6	287	651	1395	µA
				2.4 V	11.3	30.8	108	244	526	25.5	79.8	288	655	1403	
				3 V	11.6	31	108	245	530	25.9	80.5	290	659	1413	
				3.6 V	11.9	31.5	109	248	536	28.6	81.4	293	665	1428	
		-	LCD enabled(2) clocked by LSI	1.8 V	11.7	29.7	102	234	504	27.1	81.1	288.5	653	1397	
				2.4 V	11.7	29.9	102	234	506	27.2	81.0	289	656	1405	
				3 V	12.1	29.9	103	234	508	27.4	81.6	291	660	1415	
				3.6 V	12.2	30.1	103	235	510	28.8	82.4	294	667	1429	
I_{DD_ALL} (Stop 1 with RTC)	Supply current in stop 1 mode, RTC enabled	RTC clocked by LSI	LCD disabled	1.8 V	11.9	31.1	108	244	524	26.6	80.5	288	652	1396	µA
				2.4 V	12.1	31.4	109	245	528	26.7	80.9	289	656	1404	
				3 V	12.4	31.7	109	246	531	27.7	81.6	291	660	1415	
				3.6 V	12.6	32.3	110	249	537	28.9	82.8	295	667	1429	
			LCD enabled(2)	1.8 V	11.7	30.1	104	235	510	26.7	80.6	288	653	1397	
				2.4 V	11.8	30.2	104	238	511	26.7	81.1	290	657	1406	
				3 V	11.8	30.5	104	238	515	28.3	81.8	2912	661	1416	
				3.6 V	12.3	31	105	239	519	30.9	83.0	295	668	1430	
		RTC clocked by LSE bypassed at 32768 Hz	LCD disabled	1.8 V	11.6	31.3	108	244	524	-	-	-	-	-	
				2.4 V	11.8	31.6	109	245	527	-	-	-	-	-	
				3 V	12.3	31.9	109	246	531	-	-	-	-	-	
				3.6 V	12.7	32.5	111	249	537	-	-	-	-	-	
		RTC clocked by LSE quartz(3) in low drive mode	LCD disabled	1.8 V	11.5	31.1	108	244	-	-	-	-	-	-	
				2.4 V	11.5	31.4	109	246	-	-	-	-	-	-	
				3 V	12	31.7	109	247	-	-	-	-	-	-	
				3.6 V	12.4	32.3	110	250	-	-	-	-	-	-	

Figure 31. I/O AC characteristics definition(1)



Maximum frequency is achieved if ($t_r + t_f$ (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 72: I/O AC characteristics*.

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 73. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3xV_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7xV_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Table 82. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W_to_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC1_OUTx for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001 DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 50 pF, RL ≥ 5 kΩ CL ≤ 10 pF		1 1.4	-	-	µs
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DAC1_OUTx reaches final value ±1LSB)	DAC1_OUTx pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC1_OUTx pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC1_OUTx pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	

Table 96. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V Voltage Range 1	-	13	15.5	ns
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range 1	-	13	26.5	
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range 2	-	13	30	
-		Slave mode 1.08 V < V_{DDIO2} < 1.32 V(3)	-	26	60	
$t_{v(MO)}$		Master mode	-	4.5	6	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	7	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.
3. SPI mapped on Port G.

Figure 36. SPI timing diagram - slave mode and CPHA = 0

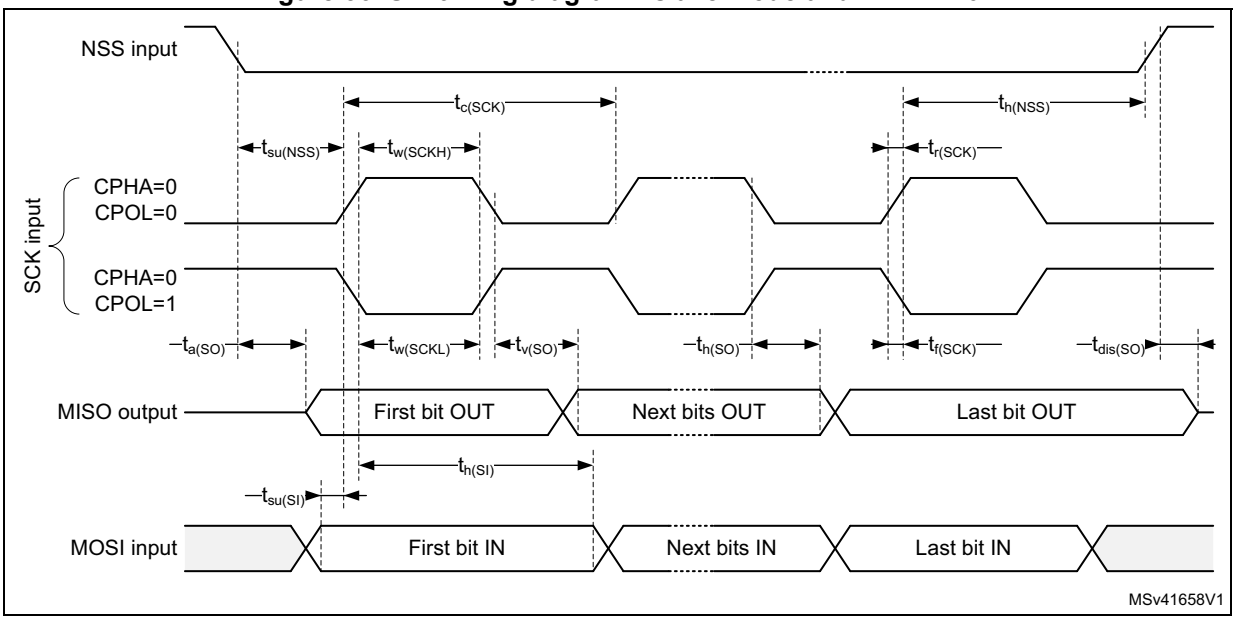


Figure 39. Quad SPI timing diagram - SDR mode

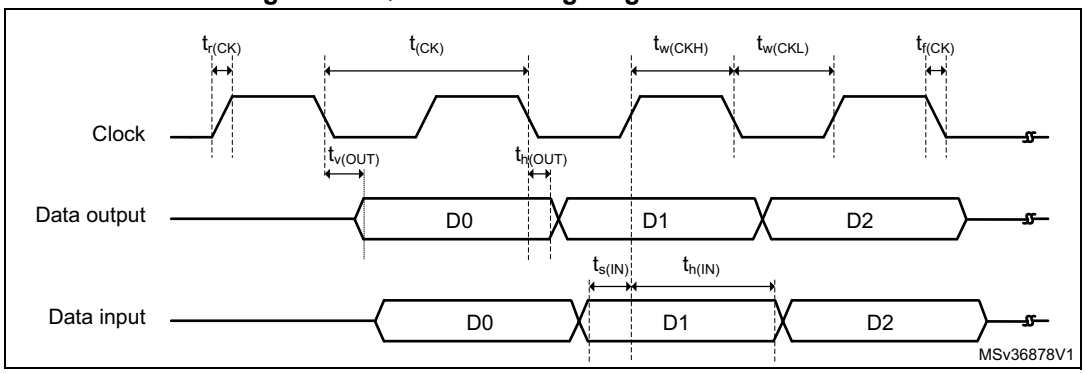


Figure 40. Quad SPI timing diagram - DDR mode

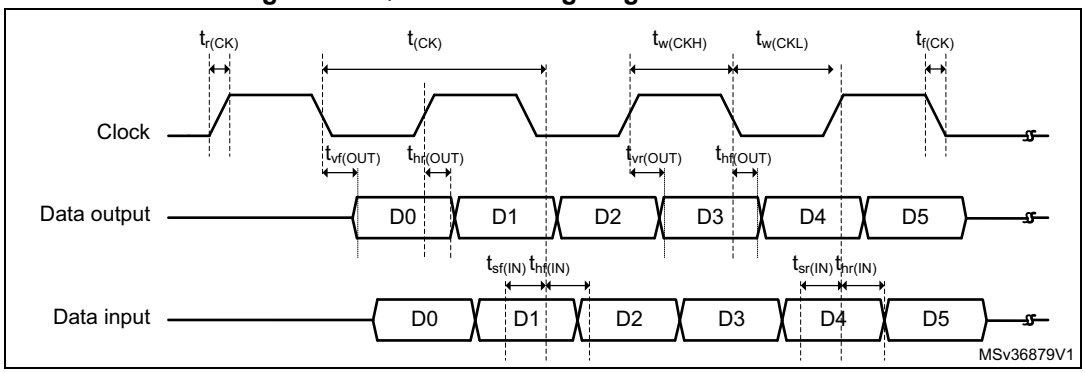


Figure 54. NAND controller waveforms for read access

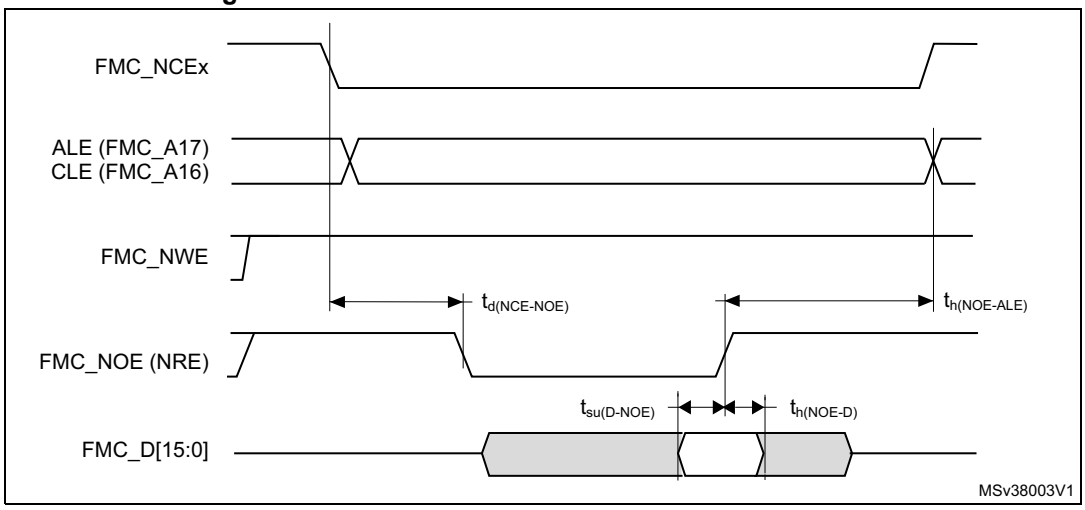


Figure 55. NAND controller waveforms for write access

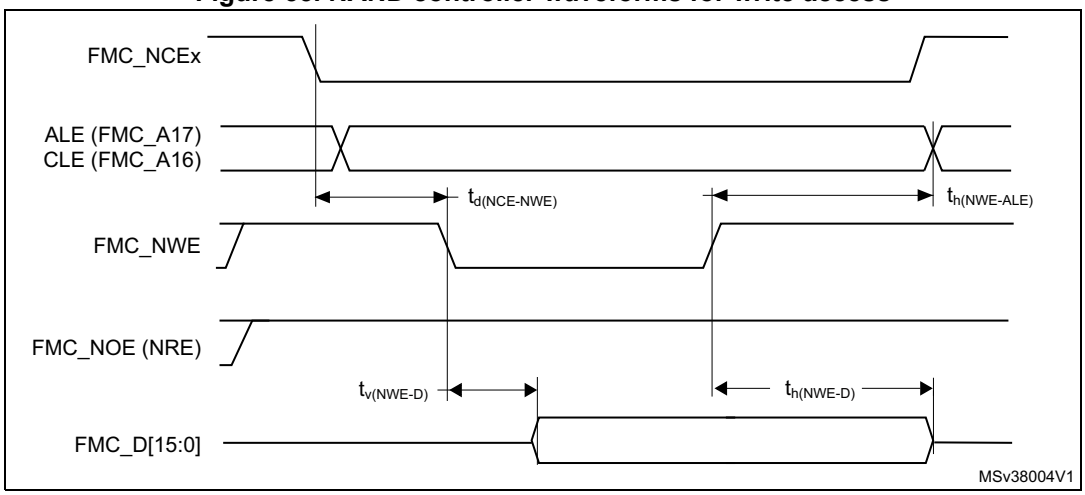


Figure 56. NAND controller waveforms for common memory read access

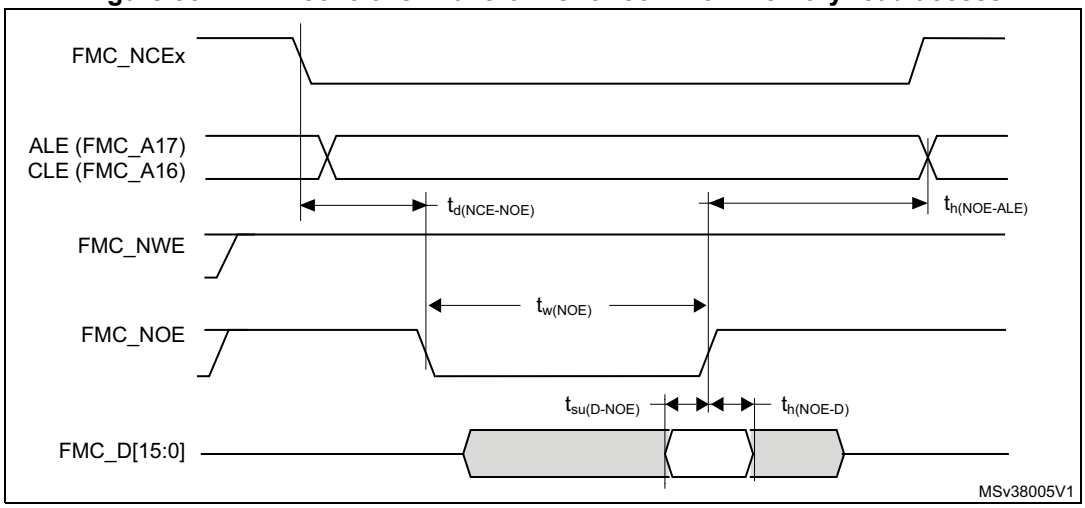


Figure 57. NAND controller waveforms for common memory write access

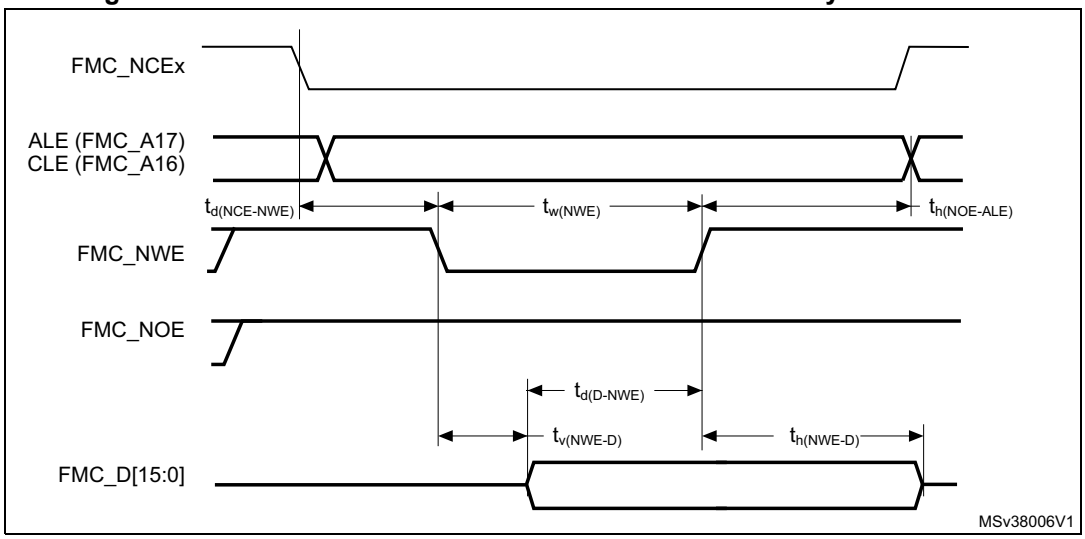


Table 117. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	12	-	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	-	$3T_{HCLK}$+1	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	$4T_{HCLK}$-2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 118. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	5	-	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{HCLK}$-1	-	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}$-1	-	
$T_{d(NCE_NWE)}$	FMC_NCE valid before FMC_NWE low	-	$3T_{HCLK}$+1	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{HCLK}$-2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

6.3.30 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 119* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage

Figure 60. SD default mode

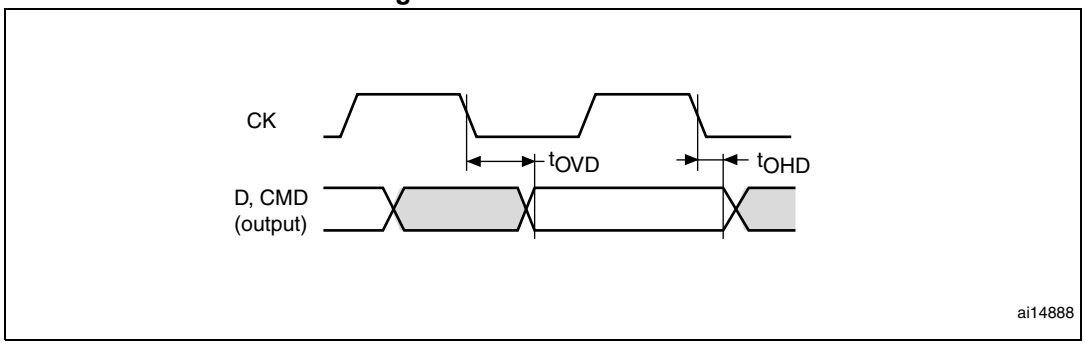


Table 121. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode		0		50	MHz
-	SDIO_CK/fPCLK2 frequency ratio		-	-	4/3	-
$t_{W(CKL)}$	Clock low time	fpp =50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50 MHz	8	10	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50 MHz	2.5	-	-	ns
t_{IH}	Input hold time HS	fpp =50 MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50 MHz	-	12	13	ns
t_{OH}	Output hold time HS	fpp =50 MHz	10	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
tISUD	Input setup time SD	fpp =25 MHz	3.5	-	-	ns
tIHD	Input hold time SD	fpp =25 MHz	3	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
tOVD	Output valid default time SD	fpp =25 MHz	-	3	5	ns
tOHD	Output hold default time SD	fpp =25 MHz	0	-	-	

1. Guaranteed by characterization results.

Table 122. SD / MMC dynamic characteristics, V_{DD}=1.71 V to 1.9 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns

Table 123. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-
F	0.450	0.500	0.550	0.0177	0.0197	0.0217
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 62. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint

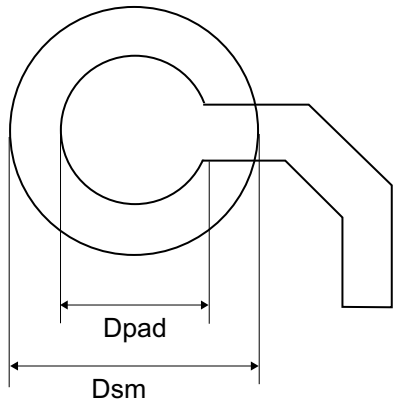


Table 124. UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

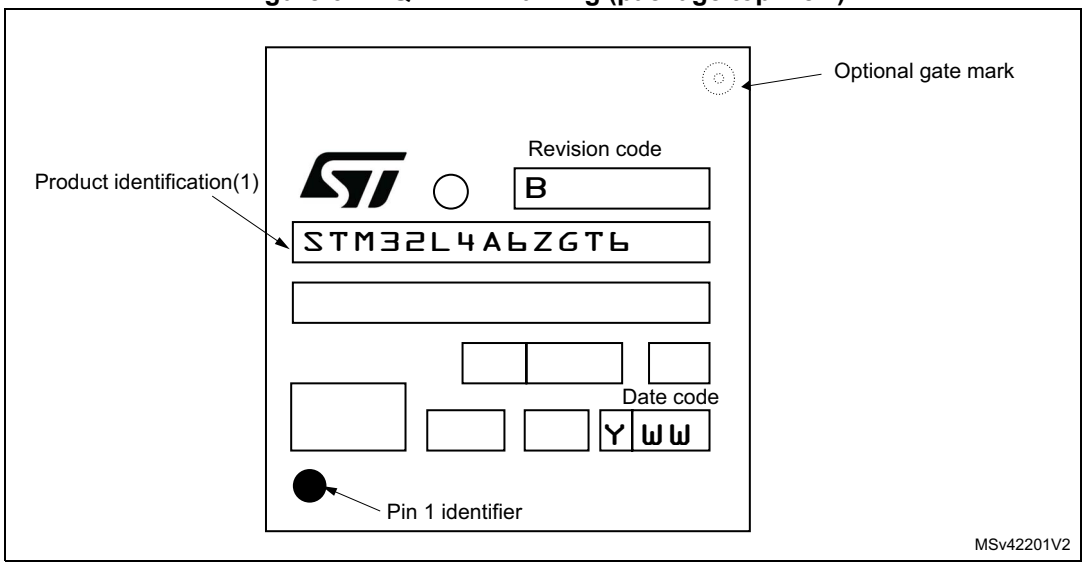
Note: Non-solder mask defined (NSMD) pads are recommended.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 67. LQFP144 marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.