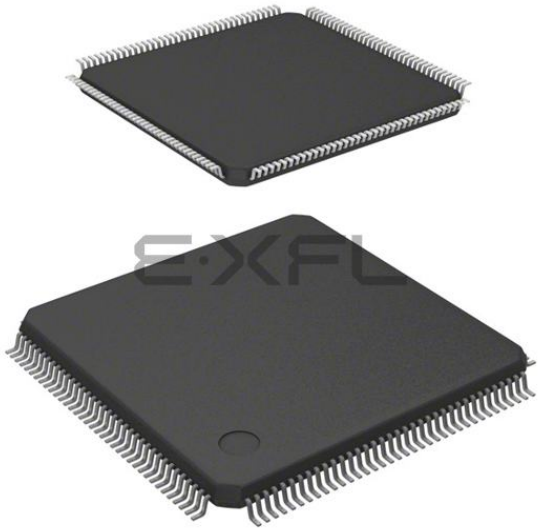

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Not For New Designs
Type	Fixed Point
Interface	I²C, SCI, SSI
Clock Rate	120MHz
Non-Volatile Memory	-
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/e-tda7590

Contents

List of tables

2.2 Pin function

Table 2. Pin function

N°	Name	Type	Description
1	SRD1/TI02	I/O	Serial receive data. Serial input data for receiver. Timer 2 input/output.
2	STD1	I/O	Serial transmit data. Serial output data from transmitter.
3	SC02	I/O	Serial control 2.Transmitter frame sync only in asynchronous mode, transmitter and receiver frame sync in synchronous mode.
4	SC01	I/O	Serial control 1. Receive frame sync in asynchronous mode, output from transmitter 2 or serial flag 1 in synchronous mode.
5	DE_N	I/O	Test data output (input/output). Debug request input and acknowledge output.
6	NMI_N	I	Non-maskable interrupt/ PINIT. Used to enable the PLL during RESET and as a non-maskable interrupt at all other times.
7	SRD0	I/O	Serial receive data. Serial input data for receiver.
8	IOVDD	I	IO power supply.
9	IOVSS	I	IO ground.
10	STD0	I/O	Serial Transmit Data. Serial output data from transmitter.
11	SC10/SCL	I/O	ESSI1 serial control 0. Receive clock in asynchronous mode, output from transmitter or serial flag in synchronous mode. I^2C SCL serial clock line.
12	SC00	I/O	Serial control 0. Receive clock in asynchronous mode, output from transmitter 1 or serial flag 0 in synchronous mode.
13	RXD	I/O	SCI receive data. Receives byte-oriented serial data.
14	TXD	I/O	SCI read enable. Transmits serial data from SCI transmit shift register.
15	SCLK	I/O	SCI serial clock. Input or output clock from which data is transferred in synchronous mode and from which the transmit and/or receive baud rate is derived in asynchronous mode.
16	SCK1/TI01	I/O	Serial clock. Serial bit clock for transmitter only in asynchronous mode, serial bit clock for both receiver and transmitter in synchronous mode. Timer 1 input/output.
17	SCK0	I/O	Serial clock. Serial bit clock for transmitter only in asynchronous mode, serial bit clock for both receiver and transmitter in synchronous mode.
18	RESETN	I	System reset. A low level applied to RESET_N input initializes the IC.
19	SCANEN	I	SCAN enable. When active with TESTEN also active, controls the shifting of the internal scan chains.
20	TESTEN	I	Test enable. When active, puts the chip into test mode and muxes the XTI clock to all flip-flops. When SCANEN is also active, the scan chain shifting is enabled.
21	COREVSS	I	Core ground.
22	COREVDD	I	Core power supply.
23	TIO0	I/O	Timer 0 input/output.
24	VSSSUB	I	Analog substrate isolation.

Table 2. Pin function (continued)

N°	Name	Type	Description
52	HAD[6]	I/O	Host 8-bit data line 6. Host data bus and/or address lines when in multiplexed mode.
53	HAD[5]	I/O	Host 8-bit data line 5. Host data bus and/or address lines when in multiplexed mode.
54	HAD[4]	I/O	Host 8-bit data line 4. Host data bus and/or address lines when in multiplexed mode.
55	COREVDD	I	Core power supply.
56	COREVSS	I	Core ground.
57	HAD[3]	I/O	Host 8-bit data line 3. Host data bus and/or address lines when in multiplexed mode.
58	HAD[2]	I/O	Host 8-bit data line 2. Host data bus and/or address lines when in multiplexed mode.
59	HAD[1]	I/O	Host 8-bit data line 1. Host data bus and/or address lines when in multiplexed mode.
60	HAD[0]	I/O	Host 8-bit data line 0. Host data bus and/or address lines when in multiplexed mode.
61	AA[3]	O	Address attributes line 3.Port A address attributes/chip select pins with programmable polarity.
62	AA[2]	O	Address attributes line 2.Port A address attributes/chip select pins with programmable polarity.
63	BR_N	O	Bus request. Asserted when port A requires bus mastership to perform off-chip accesses.
64	BB_N	I/O	Bus busy. Asserted by port A when bus_busy_in_n is negated and BG_N is asserted.
65	IOVDD	I	IO power supply.
66	IOVSS	I	IO ground.
67	WEN_N	O	Write enable.
68	OEN_N	O	Output enable.
69	AA[1]	O	Address attributes line 1.Port A address attributes/chip select pins with programmable polarity.
70	AA[0]	O	Address attributes line 0.Port A address attributes/chip select pins with programmable polarity.
71	BG_N	I	Bus grant. When asserted, Port A becomes the bus master elect. Bus mastership is attained when bus busy is negated by the current bus master.
72	AB[0]	O	Address bus line 0. Port A external address bus.
73	AB[1]	O	Address bus line 1. Port A external address bus.
74	IOVDD	I	IO power supply.
75	IOVSS	I	IO ground.
76	AB[2]	O	Address bus line 2. Port A external address bus.

Table 2. Pin function (continued)

N°	Name	Type	Description
77	AB[3]	O	Address bus line 3. Port A external address bus.
78	AB[4]	O	Address bus line 4. Port A external address bus.
79	AB[5]	O	Address bus line 5. Port A external address bus.
80	IOVDD	I	IO power supply.
81	IOVSS	I	IO ground.
82	AB[6]	O	Address bus line 6. Port A external address bus.
83	AB[7]	O	Address bus line 7. Port A external address bus.
84	AB[8]	O	Address bus line 8. Port A external address bus.
85	AB[9]	O	Address bus line 9. Port A external address bus.
86	COREVDD	I	Core power supply.
87	COREVSS	I	Core ground.
88	AB[10]	O	Address bus line 10. Port A external address bus.
89	AB[11]	O	Address bus line 11. Port A external address bus.
90	IOVDD	I	IO power supply.
91	IOVSS	I	IO ground.
92	AB[12]	O	Address bus line 12. Port A external address bus.
93	AB[13]	O	Address bus line 13. Port A external address bus.
94	AB[14]	O	Address bus line 14. Port A external address bus.
95	AB[15]	O	Address bus line 15. Port A external address bus.
96	AB[16]	O	Address bus line 16. Port A external address bus.
97	AB[17]	O	Address bus line 17. Port A external address bus.
98	AB[18]	O	Address bus line 18. Port A external address bus.
99	AB[19]	O	Address bus line 19. Port A external address bus.
100	DB[0]	I/O	Address bus 0. Port A external data bus.
101	DB[1]	I/O	Address bus 1. Port A external data bus.
102	DB[2]	I/O	Address bus 2. Port A external data bus.
103	COREVDD	I	Core power supply.
104	COREVSS	I	Core ground.
105	DB[3]	I/O	Data bus line 3. Port A external data bus.
106	DB[4]	I/O	Data bus line 4. Port A external data bus.
107	DB[5]	I/O	Data bus line 5. Port A external data bus.
108	DB[6]	I/O	Data bus line 6. Port A external data bus.
109	DB[7]	I/O	Data bus line 7. Port A external data bus.
110	DB[8]	I/O	Data bus line 8. Port A external data bus.
111	IOVDD	I	IO Power Supply.

Table 2. Pin function (continued)

N°	Name	Type	Description
143	SC12	I/O	Serial control 2.Transmitter frame sync only in asynchronous mode, transmitter and receiver frame sync in synchronous mode.
144	SC11/SDA	I/O	Serial control 1. Receive frame sync in asynchronous mode, output from transmitter 2 or serial flag 1 in synchronous mode. I^2C SDA. Serial data line.

2.3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\text{-}j\text{-}pins}$	Thermal resistance junction to pins	32	°C/W

Table 4. Key parameters (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DR	Dynamic range		89		dB
ICL	Interchannel isolation		-100		dB
DAC differential					
Vpp	Maximum input range at ADC1			2.8	V
THD/S	Total harmonics distortion to signal		-58		dB
(THD+N)/S	(THD + Noise) to signal		-57		dB
DR	Dynamic range		90		dB
ICL	Interchannel Isolation		-85		dB

3.1.1 CODEC (ADC/DAC) test description

Reported typical values (table 3. - ADC and DAC sections) have been measured at Lab level during product evaluation phase. General definitions and procedures are separately defined in following dedicated paragraphs.

Total harmonic distortion with noise to signal (THD+N)/S

THD+N is defined as the ratio of the total power of the second power and higher harmonic with noise components to the power of the fundamental for that signal. For THD+N measurement, choose the DSP analyzer in digital analyzer with THD ratio as measurement option. Measure the THD+N value at -3 dB amplitude of the input signal. First measure the THD+N value at 1Vrms which is 0 dB reference and then measure the value at -3 dB reference.

Dynamic range (DR)

DR is defined as the level of THD+N measured when the input sine wave amplitude is so small that no harmonics apart from the fundamental tone are present in the output signal. This way THD+N becomes practically the ratio between the whole signal and noise floor, being a different way to express SNR. As a convention, at which no harmonics should be present in the output signal, it is fixed at -40dB of the full scale amplitude.

Crosstalk or interchannel isolation

A disturbance, caused by electromagnetic interference, along a circuit or a cable pair. An electric signal disrupts another signal in an adjacent circuit and can cause it to become confused and cross over each other. Crosstalk is measured by applying a signal -3dB amplitude of input signal at one channel (A) and no signal at an other channel (B), measuring the effect on this channel (B) because of the channel (A).

Total harmonic distortion to signal (THD)/S

THD is defined as the ratio of the sum of only those components of the output signal which are harmonic of system input, after having removed the fundamental tone corresponding to the pure sine wave as input and the input signal.This measurement is done by using the Harmonic analyzer which can isolate up to 15th harmonic components on the acquired signal and report the sum of all of them, centering the fundamental tone on the frequency provided by the input signal generator. These measurements are performed at -3dB reference amplitude of input signal.

4 Electrical specification

4.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
PLL_VDD	3.3V PLL power supply voltage	-0.5 to 4	V
CODEC_VDD	3.3V CODEC analog power supply	-0.5 to 4	V
IOVDD	3.3V IO power supply	-0.5 to 4	V
CORE_VDD	1.8V CORE power supply	-0.5 to 2.2	V
IO_MAX	Input or output voltage	-0.5 to (IOVDD +0.5)	V

4.2 Electrical characteristics for I/O pins

Table 6. Recommended DC operating conditions

Symbol	Parameter	Value	Unit
IOVDD	IO power supply voltage	3 to 3.6(1)	V
T_j	Operating junction temperature	-40 to 105	°C

1. All the specification are valid only within these recommended operating conditions.

Table 7. General interface electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Iil	Low level input current without pull-up device				1	µA
Iih	High level input current without pull-down device				1	µA
Ioz	Tri-state output leakage without pull up/down device				1	µA
IozFT	Five Volt tolerant tri-state output leakage without pull up/down device				1	µA
I latch-up	I/O latch-up current	V < 0V, V < Vdd	200			mA
Vesd	Electrostatic protection (HBM)	leakage < 1mA	2000			V
Vil	Low level input voltage(1))				0.8	V
Vih	High level input voltage(1)		2			V
Vhyst	Schmitt trigger hysteresis(1)		0.4			V
Vol	Low level output voltage (1) (2) (3)	Iol = XmA			0.15	V
Voh	High level output voltage (1) (2) (3)	Ioh = -XmA	IOVDD - 0.15			V

1. TTL specifications only apply to the supply voltage range Vdd = 3.15V to 3.6V.
2. Takes into account 200mV voltage drop in both supply lines.
3. X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

5 24 bit DSP core

The DSP core is a general purpose 24-bit DSP. The main feature of the DSP core are listed below:

- 120 MHz operating frequency (120 MIPS)
- Fully pipelined 24 x 24 bit parallel multiplier-accumulator
- Saturation/limiting logic
- 56-bit parallel barrel shifter
- Linear, reverse carry and modulo addressing modes
- 24-bit address buses for program, X and Y data spaces and DMA
- Memory-expandible hardware stack
- Nested zero-overhead DO loops
- Fast interrupts
- Powerful JTAG emulation port
- Software wait and stop low power standby modes
- Program address tracing support
- Two 24-bit data moves in parallel with arithmetic operations
- External interrupts including non-maskable interrupt
- Interrupts may be independently masked and prioritized
- Bit-manipulation instructions can access any register or memory location
- On board support for DMA controller

6 Memories

128 K x 24-bit RAM divided into 4 areas, program RAM(PRAM), X data RAM(XRAM), Y data RAM(YRAM) and flexible allocation RAM(FLEX) as follows:

- 16 kB PRAM
- 40 kB FLEX RAM. FLEX RAM is accessed through the expansion port by the DSP core.
- External access to the FLEX RAM is also supported.
- 72 kB RAM is allocated as XRAM and YRAM. Four configurations are supported:
  - 4 kB XRAM and 68 kB YRAM
  - 8 kB XRAM and 64 kB YRAM
  - 16 kB XRAM and 56 kB YRAM
  - 24 kB XRAM and 48 kB YRAM

The key features of the host interface are:

- 8 bit parallel port "Full-duplex" dedicated host register bank
- Dedicated Mozart™ core DSP register core bank.
- Register banks map directly into Mozart X memory space
- 3 transfer modes:
  - host command
  - Host to Mozart core DSP
  - Mozart core DSP to host
- Access protocols:
  - Software polled
  - Interrupt
  - DMA access by the Mozart core DSP core
- 2+ wait states clock cycles per transfer
- Supported instructions:
  - Data transfer between Mozart core and external host using Mozart MOVE instruction
  - Simple I/O service routine with bit addressing instructions
  - IO service using fast interrupts with MOVEP instructions.

7.5 ESSI

The ESSI peripheral enables serial-port communication between the DSP core and external devices including Codecs, DSP, microprocessors. The ESSI is capable of driving 12 programmable external pins which can be configured as GPIO ports C and D or ESSI pins.

The key features of the ESSI are:

- Independent receiver and transmitter
- Synchronous or asynchronous channel modes synchronous. Receiver and transmitter use same clock/sync asynchronous. Receiver and transmitter may use separate clock/sync up to one transmitter enabled in asynchronous channel mode.
- Up to three transmitters enabled in synchronous channel mode.
- Normal mode. One word per period.
- Network mode. Up to 32 words per period.

7.6 EOC

The Salieri extended on-chip memory interface provides access to 40 kB of on-chip memory. The Mozart core will treat this memory as if it were external. Access by off-chip expansion bus masters is permitted. All accesses to the extended on-chip RAM are controlled by the extended on-chip memory control register. This register determines which combinations of the Address attribute pins should be interpreted as accesses to the 40 kB of RAM.

7.7 Timers and watchdog block

The timers and watchdog block consists of a common 21-bit prescaler and three independent and identical general-purpose 24-bit timer/event counters, each with its own register set.

Each timer has the following capabilities:

- Uses internal or external clocking.
- Interrupts the Mozart after a specified number of events (clocks).
- Signals an external device after counting internal events.
- Triggers DMA transfers after a specified number of events (clocks) occurs.
- Connects to the external world through designated pins TIO[0-2] for timers 0-2.

When TIO is configured as an

- Input: timer functions as an external event counter. Timer measures external pulse width/signal period.
- Output: timer functions as a:
  - Timer
  - Watchdog timer
  - Pulse-width modulator.

7.8 PLL

The PLL generates the following clocks:

- DCLK: DSP core clock
- DACLK: ADC and DAC clock
- LRCLK: left/right clock for the SAI and the CODEC
- SCLK: shift serial clock for the SAI and the CODEC

7.9 CODEC cell

The main features of the CODEC cell are listed below:

- 20 bits stereo DAC, and 18 bits ADC
- I^2S format
- Oversampling ratio: 512
- Sampling rates of 8 kHz to 48 kHz

The analog interface is in the form of differential signals for each channel. The interface on the digital side has the form of an SAI interface and can interface directly to an SAI channel and then to the DSP core.

DCLK can be supplied either by the internal PLL or by external, to allow synchronization with external anal digital sources.

```
;---------------------------------------------------------------------
;            EQUATES for Expansion Port
;---------------------------------------------------------------------
EXP_BCR      EQU     $FFFFFB        ; Bus Control Register address
EXP_AAR0     EQU     $FFFFF9        ; Address Attribte Register (AAR0) address
EXP_AAR1     EQU     $FFFFF8        ; Address Attribte Register (AAR1) address
EXP_AAR2     EQU     $FFFFF7        ; Address Attribte Register (AAR2) address
EXP_AAR3     EQU     $FFFFF6        ; Address Attribte Register (AAR3) address
EXT_RAM_STARTEQU     $C00000

;---------------------------------------------------------------------
;            EQUATES for Extended Memory
;---------------------------------------------------------------------
EOC_ADR      EQU     $FFFFCA

;*************************************************************************
;***************************** Initialisation Values  ********************
;*************************************************************************

;-------------------------------------------------------------------------
;           CODEC Intitialisation values
;-------------------------------------------------------------------------
; --- INIT_CCR ------------------------------------------------------------
; settings fro the CODEC Control Register
;                       321098765432109876543210
INIT_CODEC_CSR  EQU    %000000001110011011011011  ; $00E6DB  DACgain = 0dB - ADCgain = +0dBdB
;                                          011 --- GADCL[0:2]
;                                       011 ------ GADCR[0:2]
;                                    011 --------- GDACL[0:2]
;                                 011 ------------ GDACR[0:2]
;                                0 --------------- MUTEDAC (1=Mute)
;                               1 ---------------- PDNDAC (1=pwrdwn)
;                              1 ----------------- PDNADC (1=pwrdwn)
;                             1 ------------------ NRST (0=reset)

;-------------------------------------------------------------------------
;           SAI Intitialisation values
;-------------------------------------------------------------------------

;--- INIT_RCS ------------------------------------------------------------
; settings for the Receiver Control/Status Register
;                       321098765432109876543210
INIT_SAI_RCS    EQU    %000000000001000101001001   ; $000149
;                                           1 --- R0EN (0:Disbaled; 1:Enabled)
;                                          0 ---- R1EN (0:Disbaled; 1:Enabled)
;                                         0 ----- R2EN (0:Disbaled; 1:Enabled)
;                                        1 ------ RMME (1:Master mode; 0:Slave mode)
;                                       0 ------- Reserved
;                                    10 -------- RWL[0:1] (00:16; 01:24; 10:32)
;                                   0 ---------- RDIR (0:MSB 1st; 1:LSB 1st)
;                                  1 ----------- RLRS (0:LRCKR=0-LW; 1:LRCKR=0-RW)
;                                 0 ------------ RCKP (0:-ve ; 1:+ve)
;                                0 ------------- RREL (0:trans-1st; 1:I2S)
;                               0 -------------- RDWJ
;                              1 --------------- RXIE (0:Disabled; 1:Enabled)
;                             0 ---------------- Reserved
;                            0 ----------------- ROFL
```

```
;                              0 ------------------ RDR
;                             0 ------------------- ROFCL

;--- INIT_TCS ----------------------------------------------------------------
; settings for the Transmitter Control/Status Register
;                       3210987654321098765432l0
INIT_SAI_TCS    EQU    %000000000001010101001001   ; $000549 - non incrociato
;                                            1 --- T0EN (0:Disbaled; 1:Enabled)
;                                           0 ---- T1EN (0:Disbaled; 1:Enabled)
;                                          0 ----- T2EN (0:Disbaled; 1:Enabled)
;                                         1 ------ TMME (1:Master mode; 0:Slave mode)
;                                        0 ------- reserved
;                                      10 -------- TWL[0:1] (00:16; 01:24; 10:32)
;                                     0 ---------- TDIR (0:MSB 1st; 1:LSB 1st)
;                                    1 ----------- TLRS (0:LRCKR=0-LW; 1:LRCKR=0-RW)
;                                   0 ------------ TCKP (0:-ve ; 1:+ve)
;                                  1 ------------- TREL (0:trans-1st; 1:I2S)
;                                 0 -------------- TDWE
;                                1 --------------- TXIE (0:Disabled; 1:Enabled)
;                               0 ---------------- Reserved
;                              0 ----------------- TUFL
;                             0 ------------------ TDE
;                            0 ------------------- TUFCL

;-----------------------------------------------------------------------------
;           PLL Intitialisation values
;-----------------------------------------------------------------------------
    IF 1    ; Settings per sci 115200
;--- PLL_CSR -----------------------------------------------------------------
; settings for the PLL control register
;                       3210987654321098765432l0
; settings for the PLL control register
;                       3210987654321098765432l0
;INIT_PLL_CSR    EQU    $0E0C00
INIT_PLL_CSR    EQU    %000011100000110000000000   ; $0E0C00
;                                       00000 --- IDF =0 (actual = IDF+1=1)
;                                      0 -------- RESERVED
;                                     0 --------- LOCK (read only; 0:out of lock)
;                                    0 ---------- OUTLOCK (read only; 0:in lock)
;                                 0001100 ------ MF =12 (actual = MF + 1 = 13)
;                                0 ------------- PLLIE (0:intr disable)
;                               0 -------------- PWRDN (1:power down mode)
;                              1 --------------- DITEN (0:disable)
;                             1 ---------------- FRACTN (0:disable)
;                            1 ----------------- PEN (1:PLL enable)

;--- FRACT -------------------------------------------------------------------
; settings for the Fractional N part of the PLL
;                       3210987654321098765432l0
;INIT_PLL_FCR    EQU    $0034bd
INIT_PLL_FCR    EQU    %000000000011010010111101   ; $0034bd

;                                01110000101001 --- FRACT = 13501



;--- CLKCTL ------------------------------------------------------------------
```

```
INIT_TCPR2   EQU      $000000

;--- TPLR ---------------------------------------------------------------------
; settings for the clock control register
;                      32109876543210987654321O
;INIT_TPLR   EQU      %00100000000000011111100111            ; $2003E7 source TIO0 / divider = 999+1
INIT_TPLR    EQU      %00000000000000011111100111            ; $0003E7 source internal / prescaler 999
;                        x------------------------>           ; Reserved. Write to zero for future compatibility.
;                         01---------------------->  PS[1-0]  ; Prescaler Source [00 internal / 01 external TIO0 /
;                                                              ;              10  external TIO0 / 11  external TIO0]
;                           00000000010000000000->  PL[20-0] ; Prescaler Preload Value200400


;------------------------------------------------------------------------------
;           Interrupt Initialisation Values
;------------------------------------------------------------------------------
; settings for the Interrupt priority register - Core
;                      32109876543210987654321O
INIT_IPR_C      EQU    %000000000000000000000000   ; $000000

; settings for the Interrupt priority register - peripherals
;                      32109876543210987654321O
INIT_IPR_P      EQU    %000000000011111001000100   ; $29C4 glitch sull'uscita del dac
;                                           00---- HI
;                                         11------ ESSI0
;                                       00-------- ESSI1
;                                     11---------- SCI
;                                   11------------ TIMER
;                                 11 ------------- SAI
;                               11 --------------- CODEC
;                             00 ----------------- PLL
;                           00 ------------------- Unknow
;                         00 --------------------- I2C
;                       00 ----------------------- SPI
;                     00 ------------------------- EMI


;------------------------------------------------------------------------------
;           Expansion Port Intitialisation values
;------------------------------------------------------------------------------
;--- INIT_AAR0 ----------------------------------------------------------------
; settings for the Address Attribute Register1
;                      32109876543210987654321O
INIT_AAR0       EQU    %110000000000010000010000 ; C00410
;                                          00 --- BAT  (00: Synchronous SRAM; 01: SRAM; 10: DRAM; 11: Reserved)
;                                           0 ----- BAAP (0:AA1 active low; 1: AA1 active high)
;                                          0 ------ BPEN (0: P space disabled; 1: P space enabled)
;                                         1 ------- BXEN (0: X data space disabled; 1: X data space enabled)
;                                        0 -------- BYEN (0: Y data space disabled; 1: Y data space enabled)
;                                       0 --------- BAM  (0: 8 LSB of address will appear on A0-A7;
;                                                            1: 8 LSB of address will appear on A16-A23)
;                                     0 ---------- BPAC (0: packing disabled; 1: packing enabled)
;                                   0100 ---------- BNC  (Number of bits to compare; 1111, 1110, 1101 reserved)
;                      110000000000 --------------- BAC  (Address to compare; BNC most significant)
;--- INIT_BCR -----------------------------------------------------------------
```

```
; settings for the Bus Control Register
;                       321098765432109876543210
INIT_BCR        EQU    %001100000010010000100001 ; 306E10
;INIT_BCR        EQU    %000001111111110011100111 ; 30FE07
;                                        00111 --- BA0W (Area 0 wait states)
;                                    00000 -------- BA1W (Area 1 wait states)
;                                  111 ------------- BA2W (Area 2 wait states)
;                              111 ---------------- BA3W (Area 3 wait states)
;                           00000 ------------------- BDFW (Default area wait states)
;                          0 ------------------------ BBS  (0: ; 1: DSP is bus master READ ONLY)
;                         0 ------------------------- BLH  (0: ; 1: BLN always asserted)
;                        0 -------------------------- BRH  (0: ; 1: BRN always asserted)



;*******************************************************************************



; definitions addded by Paul Cassidy for salieri testbench
TRIGGER_TUBE   EQU   $12002
M_BCR          EQU   $FFFFFB       ; Bus Control Register
M_AAR0         EQU   $FFFFF9       ; Address Attribute 0
M_AAR1         EQU   $FFFFF8       ; Address Attribute 1
M_AAR2         EQU   $FFFFF7       ; Address Attribute 2
M_AAR3         EQU   $FFFFF6       ; Address Attribute 3

;*******************************************************************************
;************************* Main Prog Starts Here ******************************
;*******************************************************************************
startp
    org p:$0
    jmp start

sci_int
    org p:SCI_REC            ; Interrupt SCI receive
    jsr INT_SCIR
    org p:SCI_TRANS          ; Interrupt SCI transmit
    jsr INT_SCIT
    org p:SCI_REC_E          ; Interrupt SCI framing error
    jsr INT_SCIE

sai_int
    org p:SAI_RDR
    jsr INT_RDR
    org p:SAI_TDE
    jsr INT_TDE
    org p:SAI_ROF
    jsr INT_ROF
    org p:SAI_TUF
    jsr INT_TUF

essi_int
    org p:essi0_rdf
    jsr Comp_0
    nop
    org p:essi0_roe
```

```
    movep x:M_SSISR0,a0
    movep x:M_RX0,y:(r0)+
    org p:essi0_rls
    nop
    nop
    org p:essi0_tde
    jsr clr_tde0
    nop
    org p:essi0_tue
    jsr clr_tue0
    nop
    org p:essi0_tls
    nop
    nop

timer_int
        org p:Timer0_tcf
        jsr INT_TMR0_tcf
        org p:Timer0_tof
        jsr INT_TMR0_tof
        org p:Timer1_tcf
        jsr INT_TMR1_tcf
        org p:Timer1_tof
        jsr INT_TMR1_tof
        org p:Timer2_tcf
        jsr INT_TMR2_tcf
        org p:Timer2_tof
        jsr INT_TMR2_tof

        org x:0
states  dsm ntaps

        org y:0
coef    dc  .1,.3,-.1,.2

    org p:$100
start
        ; setup external memory for sync with testbench
;------------------------------------------------------------------------
;   Initialise Core
;------------------------------------------------------------------------

    clr     a
    clr     b
    move    #$0,r0
    move    #$fff,m0
    ori     #$3,mr                  ; mask interrupts
    movep   #INIT_IPR_C,x:IPR_C     ; set CORE interrupt priorities
    movep   #INIT_IPR_P,x:IPR_P     ; set PERIPHERAL interrupt priorities


;------------------------------------------------------------------------
;   Initialise PLL
;------------------------------------------------------------------------
init_pll
    movep   #INIT_PLL_CSR,x:PLL_CSR         ; enable the pll.
    jclr    #LOCK,x:<<PLL_CSR,*             ; wait for lock.
```

```
    movep   #INIT_PLL_FCR,x:PLL_FCR         ; set fract value.
    bset    #FRACEN,x:<<PLL_CSR             ; enable fractional-n operation.
    movep   #INIT_PLL_CLKCTL,x:PLL_CLKCTL   ; setup the clock generation.

    IF 1
;---------------------------------------------------------------------
;   Initialise CODEC
;---------------------------------------------------------------------
init_codec
    movep   #INIT_CODEC_CSR,x:CODEC_CSR     ; initialise CODEC control/status reg

;---------------------------------------------------------------------
;   Initialise SAI
;---------------------------------------------------------------------
; The receiver and transmitter control/status register are configured the same for simplicity only.
; Master mode , 24-bit word-size , MSB first , Low word clock = left word , Neg bit-clk polarity ,
; Non i2s format ,  (For 32-bit words) First bit x 8 , Interrupts enabled.
init_sai
    movep   #INIT_SAI_TCS,y:SAI_TCS         ; initialise transmit control/status reg
    movep   #INIT_SAI_RCS,y:SAI_RCS         ; initialise receiver control/status reg

;---------------------------------------------------------------------
; Enable gpios for HI
;---------------------------------------------------------------------
    bset  #GPIO0_DIR,x:GPIOCTRL     ; Setup HI pin for GPIO mode
    bset  #GPIO0_DIR,x:GPIODIR      ; Setup GPIO as output
    bset  #GPIO1_DIR,x:GPIOCTRL     ; Setup HI pin for GPIO mode
    bset  #GPIO1_DIR,x:GPIODIR      ; Setup GPIO as output
    ENDIF

;---------------------------------------------------------------------
; Initialize ESSI0
;---------------------------------------------------------------------
    IF 1
init_essi
    movep #$181801,x:M_CRA0 ; cra0_addr, 24'b010110000001100000011110
                            ; The divider control is set to 1 (2 words per frame)
                            ; for Normal mode, bits are left aligned to bit 23.  Word
                            ; length is set to 24 bits.PM = 1 -> Fcore/4.

    movep #$fc113e,x:M_CRB0 ; crb0_addr, 24'b111111000001010100111110
                            ; The receive exception and transmit exception interrupts
                            ; are enabled as are receive last slot and transmit last
                            ; slot. It is set in the synchronous normal mode. Data and
                            ; frame sync are clocked out on the rising edge of the clock.
                            ; Frame sync polarity is positive and occurs together with the
                            ; the first bit of data from the first slot.  MSB is shifted
                            ; first. SC2 o/p SC1 o/p SC0 o/p
Enable_pins
;---------------------------------------------------------------------
    move  #$01c000,x0       ;
    movep x:M_CRB0,b1       ;
    or    x0,b1             ;  // Enable TX2/TX1/TX0 (ESSI 0)
    movep #$00003f,x:M_PCRC ; // ALL Pins are ESSI.
                            ; check that all pins are enabled
    rep   #$05
    nop
```

```
    movep b1,x:M_CRB0

    ENDIF

    IF 1
;---------------------------------------------------------------------
; Enable gpios for TIMER
;---------------------------------------------------------------------

init_gpio
;    movep    #$000000,x:<<PCRC              ; ESSI0 port as GPIO
;    movep    #$0000ff,x:<<PRRC              ; ESSI0 port as OUT
    Movep    #$000000,x:<<PCRD              ; ESSI1 port as GPIO
    Movep    #$000000,x:<<PRRD              ; ESSI1 port as TIMER(INPUT)

;---------------------------------------------------------------------
;   Initialise Timer
;---------------------------------------------------------------------

init_timer
    bclr #0,x:M_TCSR0                              ; Disable Timer0
    bclr #0,x:M_TCSR1                              ; Disable Timer1
    bclr #0,x:M_TCSR2                              ; Disable Timer2

    movep #INIT_TCSR0,x:<<M_TCSR0                  ; Timer0 enable at mode 0 + reload
    movep #INIT_TPLR,x:<<M_TPLR                    ; Initial value of the timer counter
    movep #INIT_TLR0,x:<<M_TLR0                    ; Initial value of the timer counter
    movep #INIT_TCPR0,x:<<M_TCPR0                  ; Number of CLK/2 cycles until a trigger is generated

    movep #INIT_TCSR1,x:<<M_TCSR1                  ; Timer1 enable at mode 0 + reload
    movep #INIT_TPLR,x:<<M_TPLR                    ; Initial value of the timer counter
    movep #INIT_TLR1,x:<<M_TLR1                    ; Initial value of the timer counter
    movep #INIT_TCPR1,x:<<M_TCPR1                  ; Number of CLK/2 cycles until a trigger is generated

    movep #INIT_TCSR2,x:<<M_TCSR2                  ; Timer2 enable at mode 0 + reload
    movep #INIT_TPLR,x:<<M_TPLR                    ; Initial value of the timer counter
    movep #INIT_TLR2,x:<<M_TLR2                    ; Initial value of the timer counter
    movep #INIT_TCPR2,x:<<M_TCPR2                  ; Number of CLK/2 cycles until a trigger is generated

;---------------------------------------------------------------------
;   Initialise Expansion Port and Flex Memory
;---------------------------------------------------------------------
init_expport
     movep    #INIT_AAR0,x:EXP_AAR0         ; initialise AAR0 control/status reg
     movep    #INIT_BCR,x:EXP_BCR           ; initialise BCR reg

    ENDIF

;---------------------------------------------------------------------
;   Initialise SCI
;---------------------------------------------------------------------
    IF 1
init_sci
        movep   #$E,x:SCCR_ADR
        movep   #$7,x:PCRE_ADR
        movep   #$11b02,x:SCR_ADR
```

```
    ENDIF

;---------------------------------------------------------------------
; Enable interrupts
;---------------------------------------------------------------------

    Andi #$fc,mr            ; set DSP interrupt priority level to 0
                            ; Sets the Interrupt Mask bits in the SR
                            ; to [00]  (No exceptions masked)

    IF 1
    Bset #0,x:M_TCSR0       ; Enable Timer0
    Bset #0,x:M_TCSR1       ; Enable Timer1
    Bset #0,x:M_TCSR2       ; Enable Timer2
    ENDIF

    move    #states,r3
    move    #ntaps-1,m3
    move    #coef,r4
    move    #ntaps-1,m4

;---------------------------------------------------------------------
; Processor Loop
;---------------------------------------------------------------------

  IF 0
LOOP
;    bset    #12,x:SCR_ADR                          ; start SCI transmit
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
jmp LOOP
  ENDIF

  IF 1
LOOP
;    bset    #12,x:SCR_ADR                          ; start SCI transmit
    mac     x0,y0,a     x:(r3)+,x0      y:(r4)+,y0  ; generates variations on mean value of DAC
    move    #$AAAAAA,x0
    move    x0,x:$CAAAAA                           ; send data to expansion port
    move    x0,x:GPIODAT                           ; move PORTB pins

    bset    #12,x:SCR_ADR                          ; start SCI transmit
    mac     x0,y0,a     x:(r3)+,x0      y:(r4)+,y0  ; generates variations on mean value of DAC
    move    #$555555,x0
    move    x0,x:$C55555                           ; send data to expansion port
    move    x0,x:GPIODAT                           ; move PORTB pins
```