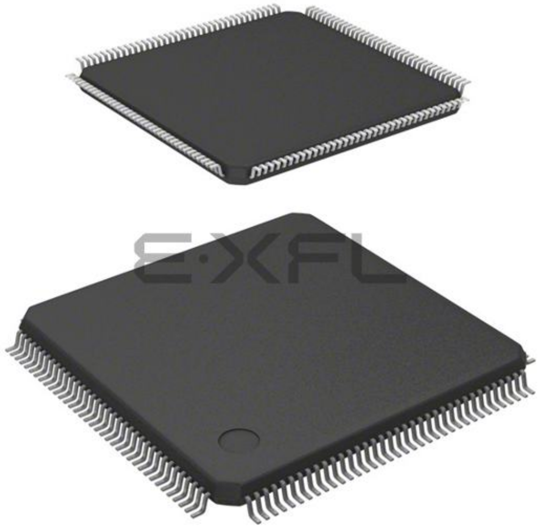

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Not For New Designs
Type	Fixed Point
Interface	I²C, SCI, SSI
Clock Rate	120MHz
Non-Volatile Memory	-
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/e-tda7590tr

Contents

List of tables

2.2 Pin function

Table 2. Pin function

N°	Name	Type	Description
1	SRD1/TI02	I/O	Serial receive data. Serial input data for receiver. Timer 2 input/output.
2	STD1	I/O	Serial transmit data. Serial output data from transmitter.
3	SC02	I/O	Serial control 2.Transmitter frame sync only in asynchronous mode, transmitter and receiver frame sync in synchronous mode.
4	SC01	I/O	Serial control 1. Receive frame sync in asynchronous mode, output from transmitter 2 or serial flag 1 in synchronous mode.
5	DE_N	I/O	Test data output (input/output). Debug request input and acknowledge output.
6	NMI_N	I	Non-maskable interrupt/ PINIT. Used to enable the PLL during RESET and as a non-maskable interrupt at all other times.
7	SRD0	I/O	Serial receive data. Serial input data for receiver.
8	IOVDD	I	IO power supply.
9	IOVSS	I	IO ground.
10	STD0	I/O	Serial Transmit Data. Serial output data from transmitter.
11	SC10/SCL	I/O	ESSI1 serial control 0. Receive clock in asynchronous mode, output from transmitter or serial flag in synchronous mode. I^2C SCL serial clock line.
12	SC00	I/O	Serial control 0. Receive clock in asynchronous mode, output from transmitter 1 or serial flag 0 in synchronous mode.
13	RXD	I/O	SCI receive data. Receives byte-oriented serial data.
14	TXD	I/O	SCI read enable. Transmits serial data from SCI transmit shift register.
15	SCLK	I/O	SCI serial clock. Input or output clock from which data is transferred in synchronous mode and from which the transmit and/or receive baud rate is derived in asynchronous mode.
16	SCK1/TI01	I/O	Serial clock. Serial bit clock for transmitter only in asynchronous mode, serial bit clock for both receiver and transmitter in synchronous mode. Timer 1 input/output.
17	SCK0	I/O	Serial clock. Serial bit clock for transmitter only in asynchronous mode, serial bit clock for both receiver and transmitter in synchronous mode.
18	RESETN	I	System reset. A low level applied to RESET_N input initializes the IC.
19	SCANEN	I	SCAN enable. When active with TESTEN also active, controls the shifting of the internal scan chains.
20	TESTEN	I	Test enable. When active, puts the chip into test mode and muxes the XTI clock to all flip-flops. When SCANEN is also active, the scan chain shifting is enabled.
21	COREVSS	I	Core ground.
22	COREVDD	I	Core power supply.
23	TIO0	I/O	Timer 0 input/output.
24	VSSSUB	I	Analog substrate isolation.

Table 2. Pin function (continued)

N°	Name	Type	Description
52	HAD[6]	I/O	Host 8-bit data line 6. Host data bus and/or address lines when in multiplexed mode.
53	HAD[5]	I/O	Host 8-bit data line 5. Host data bus and/or address lines when in multiplexed mode.
54	HAD[4]	I/O	Host 8-bit data line 4. Host data bus and/or address lines when in multiplexed mode.
55	COREVDD	I	Core power supply.
56	COREVSS	I	Core ground.
57	HAD[3]	I/O	Host 8-bit data line 3. Host data bus and/or address lines when in multiplexed mode.
58	HAD[2]	I/O	Host 8-bit data line 2. Host data bus and/or address lines when in multiplexed mode.
59	HAD[1]	I/O	Host 8-bit data line 1. Host data bus and/or address lines when in multiplexed mode.
60	HAD[0]	I/O	Host 8-bit data line 0. Host data bus and/or address lines when in multiplexed mode.
61	AA[3]	O	Address attributes line 3.Port A address attributes/chip select pins with programmable polarity.
62	AA[2]	O	Address attributes line 2.Port A address attributes/chip select pins with programmable polarity.
63	BR_N	O	Bus request. Asserted when port A requires bus mastership to perform off-chip accesses.
64	BB_N	I/O	Bus busy. Asserted by port A when bus_busy_in_n is negated and BG_N is asserted.
65	IOVDD	I	IO power supply.
66	IOVSS	I	IO ground.
67	WEN_N	O	Write enable.
68	OEN_N	O	Output enable.
69	AA[1]	O	Address attributes line 1.Port A address attributes/chip select pins with programmable polarity.
70	AA[0]	O	Address attributes line 0.Port A address attributes/chip select pins with programmable polarity.
71	BG_N	I	Bus grant. When asserted, Port A becomes the bus master elect. Bus mastership is attained when bus busy is negated by the current bus master.
72	AB[0]	O	Address bus line 0. Port A external address bus.
73	AB[1]	O	Address bus line 1. Port A external address bus.
74	IOVDD	I	IO power supply.
75	IOVSS	I	IO ground.
76	AB[2]	O	Address bus line 2. Port A external address bus.

Table 2. Pin function (continued)

N°	Name	Type	Description
77	AB[3]	O	Address bus line 3. Port A external address bus.
78	AB[4]	O	Address bus line 4. Port A external address bus.
79	AB[5]	O	Address bus line 5. Port A external address bus.
80	IOVDD	I	IO power supply.
81	IOVSS	I	IO ground.
82	AB[6]	O	Address bus line 6. Port A external address bus.
83	AB[7]	O	Address bus line 7. Port A external address bus.
84	AB[8]	O	Address bus line 8. Port A external address bus.
85	AB[9]	O	Address bus line 9. Port A external address bus.
86	COREVDD	I	Core power supply.
87	COREVSS	I	Core ground.
88	AB[10]	O	Address bus line 10. Port A external address bus.
89	AB[11]	O	Address bus line 11. Port A external address bus.
90	IOVDD	I	IO power supply.
91	IOVSS	I	IO ground.
92	AB[12]	O	Address bus line 12. Port A external address bus.
93	AB[13]	O	Address bus line 13. Port A external address bus.
94	AB[14]	O	Address bus line 14. Port A external address bus.
95	AB[15]	O	Address bus line 15. Port A external address bus.
96	AB[16]	O	Address bus line 16. Port A external address bus.
97	AB[17]	O	Address bus line 17. Port A external address bus.
98	AB[18]	O	Address bus line 18. Port A external address bus.
99	AB[19]	O	Address bus line 19. Port A external address bus.
100	DB[0]	I/O	Address bus 0. Port A external data bus.
101	DB[1]	I/O	Address bus 1. Port A external data bus.
102	DB[2]	I/O	Address bus 2. Port A external data bus.
103	COREVDD	I	Core power supply.
104	COREVSS	I	Core ground.
105	DB[3]	I/O	Data bus line 3. Port A external data bus.
106	DB[4]	I/O	Data bus line 4. Port A external data bus.
107	DB[5]	I/O	Data bus line 5. Port A external data bus.
108	DB[6]	I/O	Data bus line 6. Port A external data bus.
109	DB[7]	I/O	Data bus line 7. Port A external data bus.
110	DB[8]	I/O	Data bus line 8. Port A external data bus.
111	IOVDD	I	IO Power Supply.

3 Key parameters

3.1 Power consumption

Power consumption depends on application running and DSP clock frequency.

Supply current values are measured and guaranteed at testing level by adopting the benchmarking program reported in Appendix 1.

Table 4. Key parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
General					
fosc	Crystal frequency			16	MHz
CORE_VDD	Operating voltage	1.62	1.8	1.98	V
CODEC_VDD	Operating voltage	3.0	3.3	3.6	V
IOVDD	Operating voltage	3.0	3.3	3.6	V
PLL_VDD	Operating voltage	3.0	3.3	3.6	V
IDD_1.8V	Supply current			150	mA
IDD_3.3V	Supply current			50	mA
Tamb	Operating temperature	-40		85	°C
DSP core					
fdsp	DSP clock frequency			120	MHz
ADC single ended					
Vpp	Maximum input range at ADC1			1.4	V
THD/S	Total harmonics distortion to signal		-71		dB
(THD+N)/S	(THD + Noise) to signal		-70		dB
DR	Dynamic range		75		dB
ICL	Interchannel Isolation		-100		dB
ADC differential					
Vpp	Maximum input range at ADC0M-ADC0P			2.8	V
THD/S	Total harmonics distortion to signal		-65		dB
(THD+N)/S	(THD + Noise) to signal		-65		dB
DR	Dynamic range		84		dB
ICL	Interchannel isolation		-100		dB
DAC single ended					
Vpp	Maximum input range at ADC1			1.4	V
THD/S	Total harmonics distortion to signal		-64		dB
(THD+N)	(THD + Noise) to signal		-60		dB

Table 4. Key parameters (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DR	Dynamic range		89		dB
ICL	Interchannel isolation		-100		dB
DAC differential					
Vpp	Maximum input range at ADC1			2.8	V
THD/S	Total harmonics distortion to signal		-58		dB
(THD+N)/S	(THD + Noise) to signal		-57		dB
DR	Dynamic range		90		dB
ICL	Interchannel Isolation		-85		dB

3.1.1 CODEC (ADC/DAC) test description

Reported typical values (table 3. - ADC and DAC sections) have been measured at Lab level during product evaluation phase. General definitions and procedures are separately defined in following dedicated paragraphs.

Total harmonic distortion with noise to signal (THD+N)/S

THD+N is defined as the ratio of the total power of the second power and higher harmonic with noise components to the power of the fundamental for that signal. For THD+N measurement, choose the DSP analyzer in digital analyzer with THD ratio as measurement option. Measure the THD+N value at -3 dB amplitude of the input signal. First measure the THD+N value at 1Vrms which is 0 dB reference and then measure the value at -3 dB reference.

Dynamic range (DR)

DR is defined as the level of THD+N measured when the input sine wave amplitude is so small that no harmonics apart from the fundamental tone are present in the output signal. This way THD+N becomes practically the ratio between the whole signal and noise floor, being a different way to express SNR. As a convention, at which no harmonics should be present in the output signal, it is fixed at -40dB of the full scale amplitude.

Crosstalk or interchannel isolation

A disturbance, caused by electromagnetic interference, along a circuit or a cable pair. An electric signal disrupts another signal in an adjacent circuit and can cause it to become confused and cross over each other. Crosstalk is measured by applying a signal -3dB amplitude of input signal at one channel (A) and no signal at an other channel (B), measuring the effect on this channel (B) because of the channel (A).

Total harmonic distortion to signal (THD)/S

THD is defined as the ratio of the sum of only those components of the output signal which are harmonic of system input, after having removed the fundamental tone corresponding to the pure sine wave as input and the input signal.This measurement is done by using the Harmonic analyzer which can isolate up to 15th harmonic components on the acquired signal and report the sum of all of them, centering the fundamental tone on the frequency provided by the input signal generator. These measurements are performed at -3dB reference amplitude of input signal.

4 Electrical specification

4.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
PLL_VDD	3.3V PLL power supply voltage	-0.5 to 4	V
CODEC_VDD	3.3V CODEC analog power supply	-0.5 to 4	V
IOVDD	3.3V IO power supply	-0.5 to 4	V
CORE_VDD	1.8V CORE power supply	-0.5 to 2.2	V
IO_MAX	Input or output voltage	-0.5 to (IOVDD +0.5)	V

4.2 Electrical characteristics for I/O pins

Table 6. Recommended DC operating conditions

Symbol	Parameter	Value	Unit
IOVDD	IO power supply voltage	3 to 3.6[(1)]	V
T_j	Operating junction temperature	-40 to 105	°C

1. All the specification are valid only within these recommended operating conditions.

Table 7. General interface electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Iil	Low level input current without pull-up device				1	µA
Iih	High level input current without pull-down device				1	µA
Ioz	Tri-state output leakage without pull up/down device				1	µA
IozFT	Five Volt tolerant tri-state output leakage without pull up/down device				1	µA
I latch-up	I/O latch-up current	V < 0V, V < Vdd	200			mA
Vesd	Electrostatic protection (HBM)	leakage < 1mA	2000			V
Vil	Low level input voltage[(1)])				0.8	V
Vih	High level input voltage[(1)]		2			V
Vhyst	Schmitt trigger hysteresis[(1)]		0.4			V
Vol	Low level output voltage [(1) (2) (3)]	Iol = XmA			0.15	V
Voh	High level output voltage [(1) (2) (3)]	Ioh = -XmA	IOVDD - 0.15			V

1. TTL specifications only apply to the supply voltage range Vdd = 3.15V to 3.6V.
2. Takes into account 200mV voltage drop in both supply lines.
3. X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

5 24 bit DSP core

The DSP core is a general purpose 24-bit DSP. The main feature of the DSP core are listed below:

- 120 MHz operating frequency (120 MIPS)
- Fully pipelined 24 x 24 bit parallel multiplier-accumulator
- Saturation/limiting logic
- 56-bit parallel barrel shifter
- Linear, reverse carry and modulo addressing modes
- 24-bit address buses for program, X and Y data spaces and DMA
- Memory-expandible hardware stack
- Nested zero-overhead DO loops
- Fast interrupts
- Powerful JTAG emulation port
- Software wait and stop low power standby modes
- Program address tracing support
- Two 24-bit data moves in parallel with arithmetic operations
- External interrupts including non-maskable interrupt
- Interrupts may be independently masked and prioritized
- Bit-manipulation instructions can access any register or memory location
- On board support for DMA controller

6 Memories

128 K x 24-bit RAM divided into 4 areas, program RAM(PRAM), X data RAM(XRAM), Y data RAM(YRAM) and flexible allocation RAM(FLEX) as follows:

- 16 kB PRAM
- 40 kB FLEX RAM. FLEX RAM is accessed through the expansion port by the DSP core.
- External access to the FLEX RAM is also supported.
- 72 kB RAM is allocated as XRAM and YRAM. Four configurations are supported:
  - 4 kB XRAM and 68 kB YRAM
  - 8 kB XRAM and 64 kB YRAM
  - 16 kB XRAM and 56 kB YRAM
  - 24 kB XRAM and 48 kB YRAM

The key features of the host interface are:

- 8 bit parallel port "Full-duplex" dedicated host register bank
- Dedicated Mozart™ core DSP register core bank.
- Register banks map directly into Mozart X memory space
- 3 transfer modes:
  - host command
  - Host to Mozart core DSP
  - Mozart core DSP to host
- Access protocols:
  - Software polled
  - Interrupt
  - DMA access by the Mozart core DSP core
- 2+ wait states clock cycles per transfer
- Supported instructions:
  - Data transfer between Mozart core and external host using Mozart MOVE instruction
  - Simple I/O service routine with bit addressing instructions
  - IO service using fast interrupts with MOVEP instructions.

7.5 ESSI

The ESSI peripheral enables serial-port communication between the DSP core and external devices including Codecs, DSP, microprocessors. The ESSI is capable of driving 12 programmable external pins which can be configured as GPIO ports C and D or ESSI pins.

The key features of the ESSI are:

- Independent receiver and transmitter
- Synchronous or asynchronous channel modes synchronous. Receiver and transmitter use same clock/sync asynchronous. Receiver and transmitter may use separate clock/sync up to one transmitter enabled in asynchronous channel mode.
- Up to three transmitters enabled in synchronous channel mode.
- Normal mode. One word per period.
- Network mode. Up to 32 words per period.

7.6 EOC

The Salieri extended on-chip memory interface provides access to 40 kB of on-chip memory. The Mozart core will treat this memory as if it were external. Access by off-chip expansion bus masters is permitted. All accesses to the extended on-chip RAM are controlled by the extended on-chip memory control register. This register determines which combinations of the Address attribute pins should be interpreted as accesses to the 40 kB of RAM.

7.7 Timers and watchdog block

The timers and watchdog block consists of a common 21-bit prescaler and three independent and identical general-purpose 24-bit timer/event counters, each with its own register set.

Each timer has the following capabilities:

- Uses internal or external clocking.
- Interrupts the Mozart after a specified number of events (clocks).
- Signals an external device after counting internal events.
- Triggers DMA transfers after a specified number of events (clocks) occurs.
- Connects to the external world through designated pins TIO[0-2] for timers 0-2.

When TIO is configured as an

- Input: timer functions as an external event counter. Timer measures external pulse width/signal period.
- Output: timer functions as a:
  – Timer
  – Watchdog timer
  – Pulse-width modulator.

7.8 PLL

The PLL generates the following clocks:

- DCLK: DSP core clock
- DACLK: ADC and DAC clock
- LRCLK: left/right clock for the SAI and the CODEC
- SCLK: shift serial clock for the SAI and the CODEC

7.9 CODEC cell

The main features of the CODEC cell are listed below:

- 20 bits stereo DAC, and 18 bits ADC
- I^2S format
- Oversampling ratio: 512
- Sampling rates of 8 kHz to 48 kHz

The analog interface is in the form of differential signals for each channel. The interface on the digital side has the form of an SAI interface and can interface directly to an SAI channel and then to the DSP core.

DCLK can be supplied either by the internal PLL or by external, to allow synchronization with external anal digital sources.

```
;;; Bit Definitions for M_TCS
TUFCL       EQU     16              ; Transmitter Data Overflow Clear
TDE         EQU     15              ; Transmitter Data Ready
TUFL        EQU     14              ; Transmitter Data Overflow
;Reserved
TXIE        EQU     12              ; Transmitter Interrupt Enable
TDWE        EQU     11              ; Transmitter Data Word Justification
TREL        EQU     10              ; Transmitter Relative Timing
TCKP        EQU     9               ; Transmitter Clock Polarity
TLRS        EQU     8               ; Transmitter Left Right Selection
TDIR        EQU     7               ; Transmitter Data Shift Direction
TWL1        EQU     6               ; Transmitter Word Length Control 1
TWL0        EQU     5               ; Transmitter Word Length Control 0
;Reserved
TMME        EQU     3               ; Transmitter Master Mode Enable
T2EN        EQU     2               ; Transmitter 2 enable
T1EN        EQU     1               ; Transmitter 1 enable
T0EN        EQU     0               ; Transmitter 0 enable


;------------------------------------------------------------------------
;           EQUATES for CODEC
;------------------------------------------------------------------------
CODEC_CSR   EQU     $FFFFCB         ; CODEC Control Register Address

;;; Bit Definitions for CODEC
GADCL_0     EQU     0               ; ADC Left  Gain Bit 0
GADCL_1     EQU     1               ; ADC Left  Gain Bit 1
GADCL_2     EQU     2               ; ADC Left  Gain Bit 2
GADCR_0     EQU     3               ; ADC Right Gain Bit 0
GADCR_1     EQU     4               ; ADC Right Gain Bit 1
GADCR_2     EQU     5               ; ADC Right Gain Bit 2
GDACL_0     EQU     6               ; DAC Left  Gain Bit 0
GDACL_1     EQU     7               ; DAC Left  Gain Bit 1
GDACL_2     EQU     8               ; DAC Left  Gain Bit 2
GDACR_0     EQU     9               ; DAC Right Gain Bit 0
GDACR_1     EQU     10              ; DAC Right Gain Bit 1
GDACR_2     EQU     11              ; DAC Right Gain Bit 2
MUTEDAC     EQU     12              ; Mute DAC - Active Hi, Reset Val = 1
PDNDAC      EQU     13              ; Power down DAC - Active Hi, Reset Val = 0
PDNADC      EQU     14              ; Power down ADC - Active Hi, Reset Val = 0
N_RST       EQU     15              ; Asynchronoue Reset - Active Lo, Reset Val = 1

;------------------------------------------------------------------------
;           EQUATES for PLL
;------------------------------------------------------------------------
PLL_CSR     EQU     $FFFFD7         ; PLL Control/Status Register
PLL_FCR     EQU     $FFFFD6         ; PLL Fractional Register
PLL_CLKCTL  EQU     $FFFFD5         ; PLL Clock Control Register

;;; Bit Definitions for PLL_CSR
IDF0        EQU     0               ; Input Divide Factor 0
IDF1        EQU     1               ; Input Divide Factor 1
IDF2        EQU     2               ; Input Divide Factor 2
IDF3        EQU     3               ; Input Divide Factor 3
IDF4        EQU     4               ; Input Divide Factor 4
; Reserved
```

```
LOCK        EQU   6           ; PLL Lock Indication bit
OUTLOCK     EQU   7           ; PLL Lost Lock bit
MF0         EQU   8           ; Multiplication bit 0
MF1         EQU   9           ; Multiplication bit 1
MF2         EQU   10          ; Multiplication bit 2
MF3         EQU   11          ; Multiplication bit 3
MF4         EQU   12          ; Multiplication bit 4
MF5         EQU   13          ; Multiplication bit 5
MF6         EQU   14          ; Multiplication bit 6
PLLIE       EQU   15          ; PLL interrupt enable
PWRDN       EQU   16          ; PLL power down
DITEN       EQU   17          ; Dither Enable
FRACEN      EQU   18          ; PLL Fractional-N function enable
PEN         EQU   19          ; PLL Enable

;;; Bit Definitions for PLL_CLKCNTL
DSPDF0      EQU   0           ; DSP clock divider factor 0
DSPDF1      EQU   1           ; DSP clock divider factor 1
DSPDF2      EQU   2           ; DSP clock divider factor 2
DSPDF3      EQU   3           ; DSP clock divider factor 3
; Reserved
DCKSRC      EQU   6           ; DSP clock source  0->XTI/(DSPDF3:0 + 1)
                              ;                   1->VCO/(DSPDF3:0 + 1)
DACLKEN     EQU   7           ; Enable bit for oversampling clock
MFSDF0      EQU   8           ; Oversampling multiple bit 0
MFSDF1      EQU   9           ; Oversampling multiple bit 1
MFSDF2      EQU   10          ; Oversampling multiple bit 2
MFSDF3      EQU   11          ; Oversampling multiple bit 3
MFSDF4      EQU   12          ; Oversampling multiple bit 4
MFSDF5      EQU   13          ; Oversampling multiple bit 5
MFSDF6      EQU   14          ; Oversampling multiple bit 6
SEL0        EQU   15          ; Sampling multiple select bit 0
SEL1        EQU   16          ; Sampling multiple select bit 1
SEL2        EQU   17          ; Sampling multiple select bit 2
DSP_XTI     EQU   18          ; DSP_XTI =0 -> Use VCO/DSPDF      for DCLK
                              ; DSP_XTI =1 -> Use XTI            for DCLK
DAC_SEL     EQU   19          ; Selects between VCO and ext_dac_clk
XTLD        EQU   20          ; Disables the external crystal when set

;-----------------------------------------------------------------------
;           EQUATES for I/O Port Programming
;-----------------------------------------------------------------------
;           Register Addresses
HDR         EQU   $FFFFC9     ; PS- Host port GPIO data Register
HDDR        EQU   $FFFFC8     ; PS- Host port GPIO direction Register
PCRC        EQU   $FFFFBF     ; Port C Control Register
PRRC        EQU   $FFFFBE     ; Port C Direction Register
PDRC        EQU   $FFFFBD     ; Port C GPIO Data Register
PCRD        EQU   $FFFFAF     ; Port D Control register
PRRD        EQU   $FFFFAE     ; Port D Direction Data Register
PDRD        EQU   $FFFFAD     ; Port D GPIO Data Register
PCRE        EQU   $FFFF9F     ; Port E Control register
PRRE        EQU   $FFFF9E     ; Port E Direction Register
PDRE        EQU   $FFFF9D     ; Port E Data Register
OGDB        EQU   $FFFFFC     ; OnCE GDB Register
```

```
; settings for the clock control register
;                      321098765432109876543210
;INIT_PLL_CLKCTL EQU    $018cc1
INIT_PLL_CLKCTL EQU    %000000011000001011000001   ; $018cc1
;                                          0001 --- DSPDF =1 (actual = DSPDF+1=3)
;                                        00 ------- TESTSEL
;                                       1 --------- DCKSRC (0:XTI; 1:FVCO)
;                                      1 ---------- DACLKEN (1: enable CODEC clocks)
;                               0000010 ----------- MFSDF =2 (actual =MFSDF+1 = 3 )
;                            011 ----------------- SEL (000:128,001:256, 010:384, etc)
;                           0 -------------------- DSP_XTI (0:vco/DSPDF; 1:xti)
;                          0 --------------------- DAC_SEL (0:vco/MFSDF; 1:ext_dac_clk)
;                         0 ---------------------- XTLD (0:Enabled; 1:Disabled)

    ENDIF    ; Settings per sci 115200


;----------------------------------------------------------------------
;           Timer Intitialisation values
;----------------------------------------------------------------------
;--- TCSR0 -------------------------------------------------------------------
; settings for the Timer Control/Status Register
;                321098765432109876543210
INIT_TCSR0  EQU  %000000001000101000000100      ; $8A04    mode0 / trm=1 / tce=1 / pce=1/ dir=out
INIT_TCSR1  EQU  %000000001000101000000100      ; $8A04    mode0 / trm=1 / tce=1 / pce=1/ dir=out
INIT_TCSR2  EQU  %000000001000101000000100      ; $8A04    mode0 / trm=1 / tce=1 / pce=1/ dir=out
;                 xx ----------------------->[23-22]; unused
;                   0 ---------------------->[21]    TCF       ; Timer Compare Flag
;                    0 --------------------->[20]    TOF       ; Timer Overflow Flag
;                     xxxx ----------------->[19-16]           ; unused
;                         0 ---------------->[15]    PCE       ; Prescaler Clock Enable
;                          x --------------->[14]              ; unused
;                           0 -------------->[13]    DO        ; Data Output
;                            0 ------------->[12]    DI        ; Data Input
;                             1 ------------>[11]    DIR       ; Direction
;                              x ----------->[10]              ; unused
;                               1 ---------->[ 9]    TRM       ; Timer Reload Mode
;                                0 --------->[ 8]    INV       ; Inverter
;                                 0000 ----->[7-4]   Tc[3-0]   ; Timer Control =  Mode0
;                                     x ---->[ 3]              ; unused
;                                      1 --->[ 2]    TCIE      ; Timer Compare Interrupt Enable
;                                       0 -->[ 1]    TOIE      ; Timer Overflow Enable
;                                        0 ->[ 0]    TE        ; Timer Enable

;--- TLR0 -------------------------------------------------------------------
; settings for the Timer Load Register
INIT_TLR0    EQU      $000000
INIT_TLR1    EQU      $000000
INIT_TLR2    EQU      $000000

;--- TCPR0 -------------------------------------------------------------------
; settings for the Timer Compare Register
;INIT_TCPR0  EQU      $000002
;INIT_TCPR1  EQU      $000004
;INIT_TCPR2  EQU      $000008
INIT_TCPR0   EQU      $000000
INIT_TCPR1   EQU      $000000
```

```
; settings for the Bus Control Register
;                       321098765432109876543210
INIT_BCR        EQU    %001100000010010000100001 ; 306E10
;INIT_BCR        EQU    %000001111111110011100111 ; 30FE07
;                                         00111 --- BA0W (Area 0 wait states)
;                                    00000 -------- BA1W (Area 1 wait states)
;                                 111 ------------- BA2W (Area 2 wait states)
;                              111 ---------------- BA3W (Area 3 wait states)
;                         00000 ------------------- BDFW (Default area wait states)
;                        0 ------------------------ BBS  (0: ; 1: DSP is bus master READ ONLY)
;                       0 ------------------------- BLH  (0: ; 1: BLN always asserted)
;                      0 -------------------------- BRH  (0: ; 1: BRN always asserted)



;********************************************************************************



; definitions addded by Paul Cassidy for salieri testbench
TRIGGER_TUBE   EQU   $12002
M_BCR          EQU   $FFFFFB       ; Bus Control Register
M_AAR0         EQU   $FFFFF9       ; Address Attribute 0
M_AAR1         EQU   $FFFFF8       ; Address Attribute 1
M_AAR2         EQU   $FFFFF7       ; Address Attribute 2
M_AAR3         EQU   $FFFFF6       ; Address Attribute 3

;********************************************************************************
;************************** Main Prog Starts Here ******************************
;********************************************************************************
startp
    org p:$0
    jmp start

sci_int
    org p:SCI_REC           ; Interrupt SCI receive
    jsr INT_SCIR
    org p:SCI_TRANS         ; Interrupt SCI transmit
    jsr INT_SCIT
    org p:SCI_REC_E         ; Interrupt SCI framing error
    jsr INT_SCIE

sai_int
    org p:SAI_RDR
    jsr INT_RDR
    org p:SAI_TDE
    jsr INT_TDE
    org p:SAI_ROF
    jsr INT_ROF
    org p:SAI_TUF
    jsr INT_TUF

essi_int
    org p:essi0_rdf
    jsr Comp_0
    nop
    org p:essi0_roe
```

```
    movep x:M_SSISR0,a0
    movep x:M_RX0,y:(r0)+
    org p:essi0_rls
    nop
    nop
    org p:essi0_tde
    jsr clr_tde0
    nop
    org p:essi0_tue
    jsr clr_tue0
    nop
    org p:essi0_tls
    nop
    nop

timer_int
        org p:Timer0_tcf
        jsr INT_TMR0_tcf
        org p:Timer0_tof
        jsr INT_TMR0_tof
        org p:Timer1_tcf
        jsr INT_TMR1_tcf
        org p:Timer1_tof
        jsr INT_TMR1_tof
        org p:Timer2_tcf
        jsr INT_TMR2_tcf
        org p:Timer2_tof
        jsr INT_TMR2_tof

        org x:0
states  dsm ntaps

        org y:0
coef    dc  .1,.3,-.1,.2

    org p:$100
start
        ; setup external memory for sync with testbench
;-------------------------------------------------------------------------
;   Initialise Core
;-------------------------------------------------------------------------

    clr     a
    clr     b
    move    #$0,r0
    move    #$fff,m0
    ori     #$3,mr                  ; mask interrupts
    movep   #INIT_IPR_C,x:IPR_C     ; set CORE interrupt priorities
    movep   #INIT_IPR_P,x:IPR_P     ; set PERIPHERAL interrupt priorities


;-------------------------------------------------------------------------
;   Initialise PLL
;-------------------------------------------------------------------------
init_pll
    movep   #INIT_PLL_CSR,x:PLL_CSR         ; enable the pll.
    jclr    #LOCK,x:<<PLL_CSR,*             ; wait for lock.
```

```
    bset    #12,x:SCR_ADR                         ; start SCI transmit
    mac     x0,y0,a      x:(r3)+,x0      y:(r4)+,y0   ; generates variations on mean value of DAC
    move    #$AAAAAA,x0
    move    x0,x:$CAAAAA                          ; send data to expansion port
    move    x0,x:GPIODAT                          ; move PORTB pins

       bset    #12,x:SCR_ADR                      ; start SCI transmit
    mac     x0,y0,a      x:(r3)+,x0      y:(r4)+,y0   ; generates variations on mean value of DAC
    move    #$555555,x0
    move    x0,x:$C55555                          ; send data to expansion port
    move    x0,x:GPIODAT                          ; move PORTB pins

jmp LOOP

  ENDIF



;------------------------------------------------------------------------
;   Interrupt Service Routines
;------------------------------------------------------------------------

;SAI
;------------------------------------------------------------------------
INT_TDE                             ; The transmitter data empty flag is cleared as soon
                                    ; as the last move is performed
    Movep a,y:<<SAI_TX0             ; Load LEFT transmit data register for channel 0
    nop
    nop
    movep b,y:<<SAI_TX0             ; Load RIGHT transmit data register for channel 0
    rti


INT_RDR                             ; The receiver data ready flag is cleared as soon
                                    ; as the last move is performed
    movep   y:<<SAI_RX0,a           ; Move Channel 0 received LEFT data to x-memory.
    move    a,x:(r0)
    nop
    nop
    movep   y:<<SAI_RX0,b           ; Move channel 0 received RIGHT data to y-memory.
    move    b,y:(r0)+
    rti


INT_ROF
    bset    #16,y:SAI_RCS
    bclr    #16,y:SAI_RCS
    rti


INT_TUF
    bset    #16,y:SAI_TCS
    bclr    #16,y:SAI_RCS
    rti


;TIMER
```

```
;---------------------------------------------------------------------
INT_TMR0_tcf
;     bchg    #0,x:PDRC              ; toggle pin12 Fout=(XTI/2)/((TPLR+1)*(TCPR+1)*2)
    bchg    #13,x:M_TCSR0            ; toggle TIO0 Fout=(XTI/2)/((TPLR+1)*(TCPR+1)*2)
    nop
    rti

INT_TMR0_tof
    nop
    nop
    rti

INT_TMR1_tcf
;    bchg    #1,x:PDRC               ; toggle pin4 Fout=Fin/((TPLR+1)*(TCPR+1)*2)
    bchg    #13,x:M_TCSR1            ; toggle TIO1 Fout=(XTI/2)/((TPLR+1)*(TCPR+1)*2)
    nop
    rti

INT_TMR1_tof
    nop
    nop
    rti

INT_TMR2_tcf
;    bchg    #2,x:PDRC               ; toggle pin3  Fout=Fin/((TPLR+1)*(TCPR+1)*2)
    bchg    #13,x:M_TCSR2            ; toggle TIO2 Fout=(XTI/2)/((TPLR+1)*(TCPR+1)*2)
    nop
    rti

INT_TMR2_tof
    nop
    nop
    rti

;ESSI
;---------------------------------------------------------------------
clr_tde0
    movep   r1,x:M_TX00
    move    (r1)+
    movep   r1,x:M_TX01
    move    (r1)+
    movep   r1,x:M_TX02
    move    (r1)+
    rti

clr_tue0
    movep   x:M_SSISR0,a0
    movep   r1,x:M_TX00
    move    (r1)+
    movep   r1,x:M_TX01
    move    (r1)+
    movep   r1,x:M_TX02
    move    (1)+
    rti

Comp_0
    rti
```