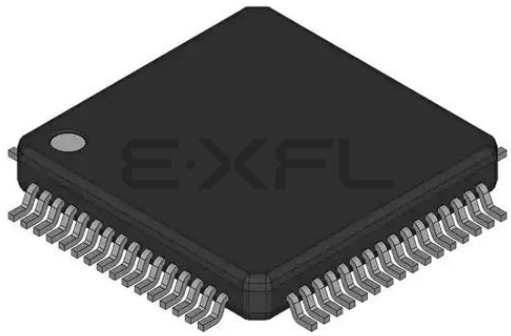

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z0h |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | CANbus, LINbus, SCI, SPI |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 45 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5602df1mlh3 |

Figure 2 shows the MPC5602D in the 100 LQFP package.

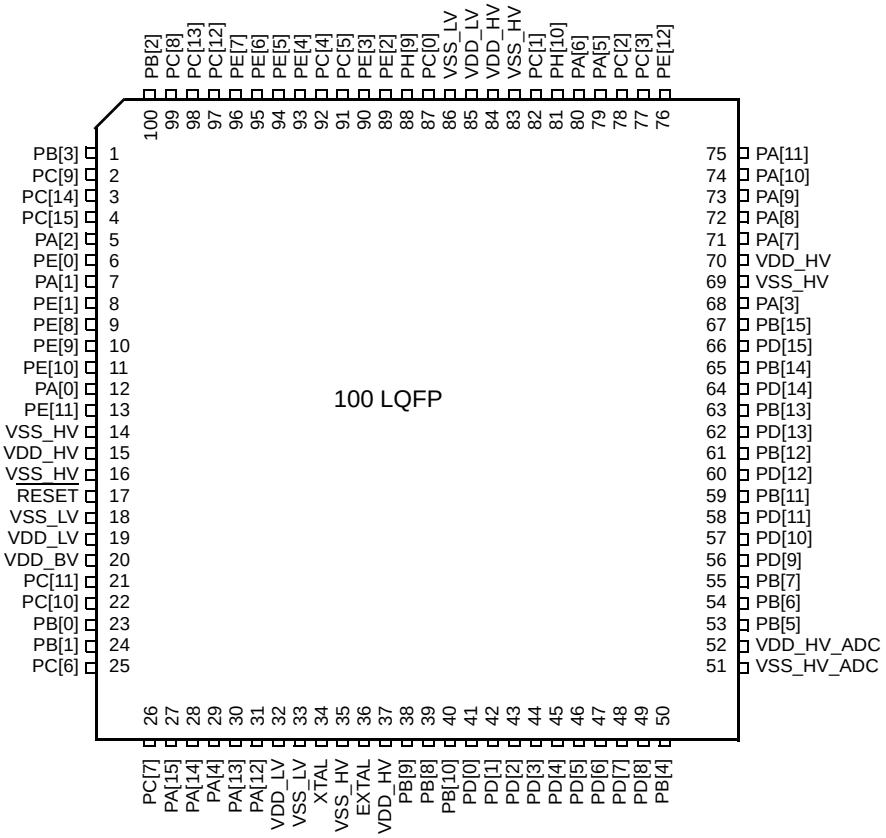


**Figure 2. 100 LQFP pin configuration (top view)**

**NOTE**

SRAM data retention is guaranteed with $V_{DD\_LV}$ not below 1.08 V.

# 4.6 Thermal characteristics

## 4.6.1 Package thermal characteristics

**Table 13. LQFP thermal characteristics[1]**

| Symbol | | C | Parameter | Conditions[2] | | Value | Unit |
|---|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | CC | D | Thermal resistance, junction-to-ambient natural convection[3] | Single-layer board —1s | LQFP64 | 72.1 | °C/W |
| | | | | | LQFP100 | 65.2 | |
| | | | | Four-layer board — 2s2p | LQFP64 | 57.3 | |
| | | | | | LQFP100 | 51.8 | |
| $R_{\theta JB}$ | CC | D | Thermal resistance, junction-to-board[4] | Four-layer board — 2s2p | LQFP64 | 44.1 | °C/W |
| | | | | | LQFP100 | 41.3 | |
| $R_{\theta JC}$ | CC | D | Thermal resistance, junction-to-case[5] | Single-layer board — 1s | LQFP64 | 26.5 | °C/W |
| | | | | | LQFP100 | 23.9 | |
| | | | | Four-layer board — 2s2p | LQFP64 | 26.2 | |
| | | | | | LQFP100 | 23.7 | |
| $\Psi_{JB}$ | CC | D | Junction-to-board thermal characterization parameter, natural convection | Single-layer board — 1s | LQFP64 | 41 | °C/W |
| | | | | | LQFP100 | 41.6 | |
| | | | | Four-layer board — 2s2p | LQFP64 | 43 | |
| | | | | | LQFP100 | 43.4 | |
| $\Psi_{JC}$ | CC | D | Junction-to-case thermal characterization parameter, natural convection | Single-layer board — 1s | LQFP64 | 11.5 | °C/W |
| | | | | | LQFP100 | 10.4 | |
| | | | | Four-layer board — 2s2p | LQFP64 | 11.1 | |
| | | | | | LQFP100 | 10.2 | |

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C

3 Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-7. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as $R_{thJA}$.

4 Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as $R_{thJB}$.

5 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as $R_{thJC}$.

## 4.6.2 Power considerations

The average chip-junction temperature, $T_J$, in degrees Celsius, may be calculated using Equation 1:

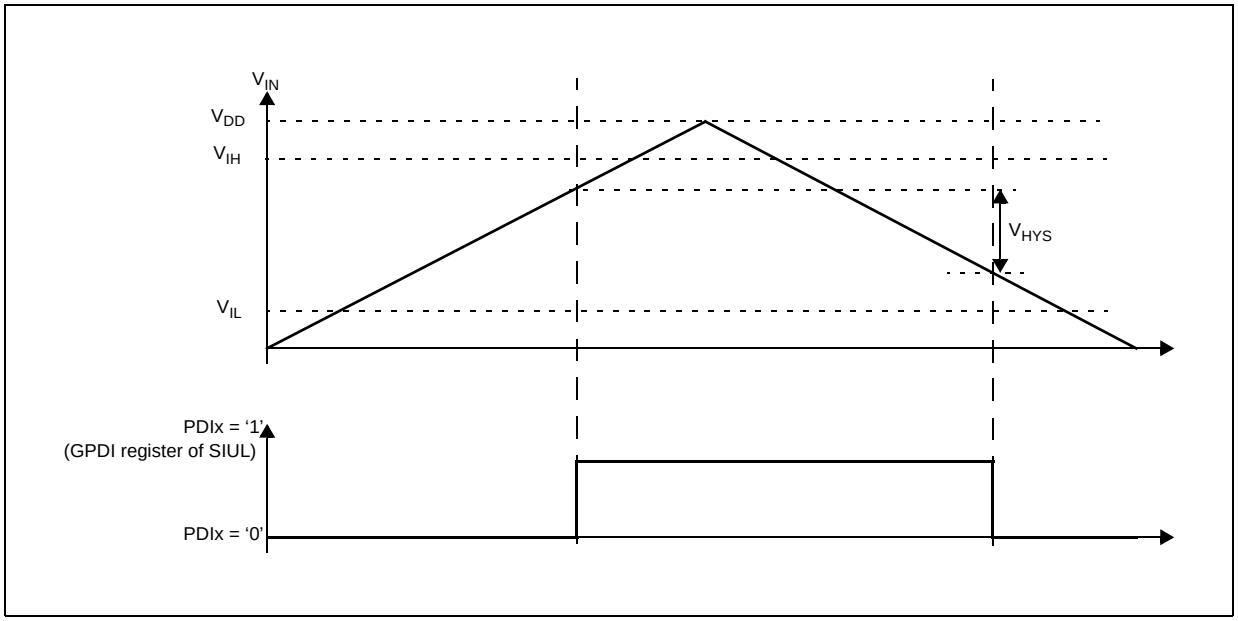


**Figure 4. Input DC electrical characteristics definition**

**Table 14. I/O input DC electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{IH}$ | SR | P | Input high level CMOS (Schmitt Trigger) | — | | $0.65V_{DD}$ | — | $V_{DD}+0.4$ | V |
| $V_{IL}$ | SR | P | Input low level CMOS (Schmitt Trigger) | — | | –0.4 | — | $0.35V_{DD}$ | V |
| $V_{HYS}$ | CC | C | Input hysteresis CMOS (Schmitt Trigger) | — | | $0.1V_{DD}$ | — | — | V |
| $I_{LKG}$ | CC | D | Digital input leakage | No injection on adjacent pin | $T_A$ = –40 °C | — | 2 | 200 | nA |
| | | D | | | $T_A$ = 25 °C | — | 2 | 200 | |
| | | D | | | $T_A$ = 85 °C | — | 5 | 300 | |
| | | D | | | $T_A$ = 105 °C | — | 12 | 500 | |
| | | P | | | $T_A$ = 125 °C | — | 70 | 1000 | |
| $W_{FI}$[2] | SR | P | Digital input filtered pulse | — | | — | — | 40 | ns |
| $W_{NFI}$(2) | SR | P | Digital input not filtered pulse | — | | 1000 | — | — | ns |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

## 4.7.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 15 provides weak pull figures. Both pull-up and pull-down resistances are supported.

**Table 17. MEDIUM configuration output buffer electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{OH}$ | CC | C | Output high level MEDIUM configuration | Push Pull | $I_{OH}$ = –3.8 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | $0.8V_{DD}$ | — | — | V |
| | | P | | | $I_{OH}$ = –2 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | $0.8V_{DD}$ | — | — | |
| | | C | | | $I_{OH}$ = –1 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[2] | $0.8V_{DD}$ | — | — | |
| | | C | | | $I_{OH}$ = –1 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | $V_{DD} – 0.8$ | — | — | |
| | | C | | | $I_{OH}$ = –100 µA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | $0.8V_{DD}$ | — | — | |
| $V_{OL}$ | CC | C | Output low level MEDIUM configuration | Push Pull | $I_{OL}$ = 3.8 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | $0.2V_{DD}$ | V |
| | | P | | | $I_{OL}$ = 2 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | $0.1V_{DD}$ | |
| | | C | | | $I_{OL}$ = 1 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1(2) | — | — | $0.1V_{DD}$ | |
| | | C | | | $I_{OL}$ = 1 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |
| | | C | | | $I_{OL}$ = 100 µA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | $0.1V_{DD}$ | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when $V_{DD}$ = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

## 4.7.4 Output pin transition times

**Table 18. Output pin transition times**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $t_{tr}$ | CC | D | Output transition time output pin[2] SLOW configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 50 | ns |
| | | T | | $C_L$ = 50 pF | | — | — | 100 | |
| | | D | | $C_L$ = 100 pF | | — | — | 125 | |
| | | D | | $C_L$ = 25 pF | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 50 | |
| | | T | | $C_L$ = 50 pF | | — | — | 100 | |
| | | D | | $C_L$ = 100 pF | | — | — | 125 | |
| $t_{tr}$ | CC | D | Output transition time output pin(2) MEDIUM configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1 | — | — | 10 | ns |
| | | T | | $C_L$ = 50 pF | | — | — | 20 | |
| | | D | | $C_L$ = 100 pF | | — | — | 40 | |
| | | D | | $C_L$ = 25 pF | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1 | — | — | 12 | |
| | | T | | $C_L$ = 50 pF | | — | — | 25 | |
| | | D | | $C_L$ = 100 pF | | — | — | 40 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 $C_L$ includes device and package capacitances ($C_{PKG}$ < 5 pF).

## 4.7.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a $V_{DD}/V_{SS}$ supply pair as described in Table 19.

Table 20 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the $I_{AVGSEG}$ maximum value.

**Table 19. I/O supply segment**

| Package | Supply segment | | | |
|---|---|---|---|---|
| | 1 | 2 | 3 | 4 |
| 100 LQFP | pin 16 – pin 35 | pin 37 – pin 69 | pin 70 – pin 83 | pin 84 – pin 15 |
| 64 LQFP | pin 8 – pin 26 | pin 28 – pin 55 | pin 56 – pin 7 | — |

**Table 21. I/O weight[1] (continued)**

| Pad | 100 LQFP/64 LQFP | | | |
|---|---|---|---|---|
| | Weight 5 V | | Weight 3.3 V | |
| | SRC[2] = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| PD[5] | 1% | 1% | 1% | 1% |
| PD[6] | 1% | 1% | 1% | 1% |
| PD[7] | 1% | 1% | 1% | 1% |
| PD[8] | 1% | 1% | 1% | 1% |
| PB[4] | 1% | 1% | 1% | 1% |
| PB[5] | 1% | 1% | 1% | 1% |
| PB[6] | 1% | 1% | 1% | 1% |
| PB[7] | 1% | 1% | 1% | 1% |
| PD[9] | 1% | 1% | 1% | 1% |
| PD[10] | 1% | 1% | 1% | 1% |
| PD[11] | 1% | 1% | 1% | 1% |
| PB[11] | 9% | 9% | 11% | 11% |
| PD[12] | 8% | 8% | 10% | 10% |
| PB[12] | 8% | 8% | 10% | 10% |
| PD[13] | 8% | 8% | 9% | 9% |
| PB[13] | 8% | 8% | 9% | 9% |
| PD[14] | 7% | 7% | 9% | 9% |
| PB[14] | 7% | 7% | 8% | 8% |
| PD[15] | 7% | 7% | 8% | 8% |
| PB[15] | 6% | 6% | 7% | 7% |
| PA[3] | 6% | 6% | 7% | 7% |
| PA[7] | 4% | 4% | 5% | 5% |
| PA[8] | 4% | 4% | 5% | 5% |
| PA[9] | 4% | 4% | 5% | 5% |
| PA[10] | 5% | 5% | 6% | 6% |
| PA[11] | 5% | 5% | 6% | 6% |
| PE[12] | 5% | 5% | 6% | 6% |
| PC[3] | 5% | 5% | 6% | 6% |
| PC[2] | 5% | 7% | 6% | 6% |
| PA[5] | 5% | 6% | 5% | 6% |
| PA[6] | 4% | 4% | 5% | 5% |
| PC[1] | 5% | 17% | 4% | 12% |

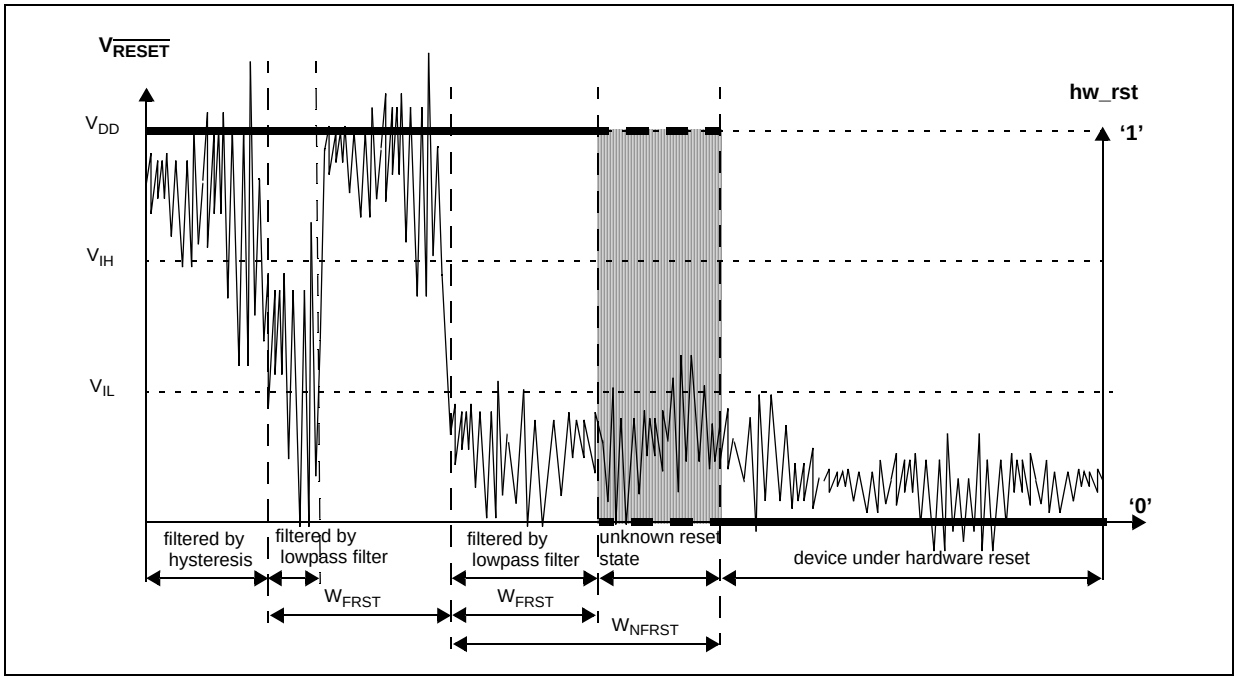


**Figure 6. Noise filtering on reset signal**

**Table 22. Reset electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{IH}$ | SR | P | Input High Level CMOS (Schmitt Trigger) | — | $0.65V_{DD}$ | — | $V_{DD}$ + 0.4 | V |
| $V_{IL}$ | SR | P | Input low Level CMOS (Schmitt Trigger) | — | –0.4 | — | $0.35V_{DD}$ | V |
| $V_{HYS}$ | CC | C | Input hysteresis CMOS (Schmitt Trigger) | — | $0.1V_{DD}$ | — | — | V |
| $V_{OL}$ | CC | P | Output low level | Push Pull, $I_{OL}$ = 2 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | $0.1V_{DD}$ | V |
| | | | | Push Pull, $I_{OL}$ = 1 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[2] | — | — | $0.1V_{DD}$ | |
| | | | | Push Pull, $I_{OL}$ = 1 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |

— Corrupted program counter
— Unexpected reset
— Critical data corruption (control registers...)

- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

## 4.12.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.

**Table 32. EMI radiated emission measurement[1] [2]**

| Symbol | | C | Parameter | Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| — | SR | — | Scan range | — | | 0.150 | — | 1000 | MHz |
| $f_{CPU}$ | SR | — | Operating frequency | — | | — | 48 | — | MHz |
| $V_{DD\_LV}$ | SR | — | LV operating voltages | — | | — | 1.28 | — | V |
| $S_{EMI}$ | CC | T | Peak level | $V_{DD}$ = 5 V, $T_A$ = 25 °C, 100 LQFP package Test conforming to IEC 61967-2, $f_{OSC}$ = 8 MHz/$f_{CPU}$ = 48 MHz | No PLL frequency modulation | — | — | 18 | dBµV |
| | | | | | ± 2% PLL frequency modulation | — | — | 14 | dBµV |

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

## 4.12.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

### 4.12.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

**Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{FIRCSTOP}$ | CC | T | Fast internal RC oscillator high frequency and system clock current in stop mode | $T_A$ = 25 °C | sysclk = off | — | 500 | — | µA |
| | | | | | sysclk = 2 MHz | — | 600 | — | |
| | | | | | sysclk = 4 MHz | — | 700 | — | |
| | | | | | sysclk = 8 MHz | — | 900 | — | |
| | | | | | sysclk = 16 MHz | — | 1250 | — | |
| $t_{FIRCSU}$ | CC | C | Fast internal RC oscillator start-up time | $V_{DD}$ = 5.0 V ± 10% | | — | 1.1 | 2.0 | µs |
| $\Delta_{FIRCPRE}$ | CC | C | Fast internal RC oscillator precision after software trimming of $f_{FIRC}$ | $T_A$ = 25 °C | | –1 | — | 1 | % |
| $\Delta_{FIRCTRIM}$ | CC | C | Fast internal RC oscillator trimming step | $T_A$ = 25 °C | | — | 1.6 | | % |
| $\Delta_{FIRCVAR}$ | CC | C | Fast internal RC oscillator variation in temperature and supply with respect to $f_{FIRC}$ at $T_A$ = 55 °C in high-frequency configuration | — | | –5 | — | 5 | % |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.

2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

## 4.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

**Table 39. Slow internal RC oscillator (128 kHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{SIRC}$ | CC | P | Slow internal RC oscillator low frequency | $T_A$ = 25 °C, trimmed | — | 128 | — | kHz |
| | SR | — | | — | 100 | — | 150 | |
| $I_{SIRC}$[2], | CC | C | Slow internal RC oscillator low frequency current | $T_A$ = 25 °C, trimmed | — | — | 5 | µA |
| $t_{SIRCSU}$ | CC | P | Slow internal RC oscillator start-up time | $T_A$ = 25 °C, $V_{DD}$ = 5.0 V ± 10% | — | 8 | 12 | µs |
| $\Delta_{SIRCPRE}$ | CC | C | Slow internal RC oscillator precision after software trimming of $f_{SIRC}$ | $T_A$ = 25 °C | –2 | — | 2 | % |
| $\Delta_{SIRCTRIM}$ | CC | C | Slow internal RC oscillator trimming step | — | — | 2.7 | — | |

**Table 39. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $\Delta_{SIRCVAR}$ | CC | P | Slow internal RC oscillator variation in temperature and supply with respect to $f_{SIRC}$ at $T_A$ = 55 °C in high frequency configuration | High frequency configuration | –10 | — | 10 | % |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.

2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

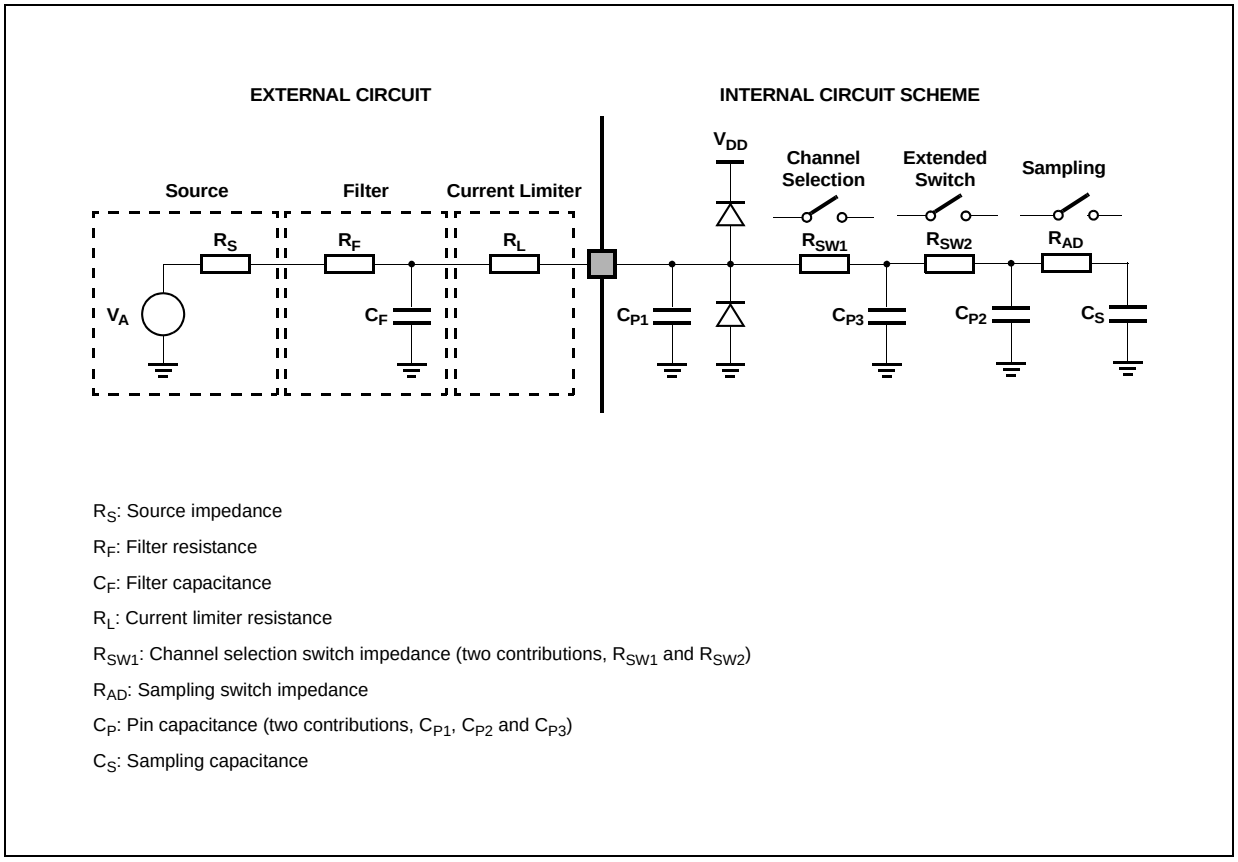


**Figure 13. Input equivalent circuit (extended channels)**

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances $C_F$, $C_{P1}$ and $C_{P2}$ are initially charged at the source voltage $V_A$ (refer to the equivalent circuit in Figure 13): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

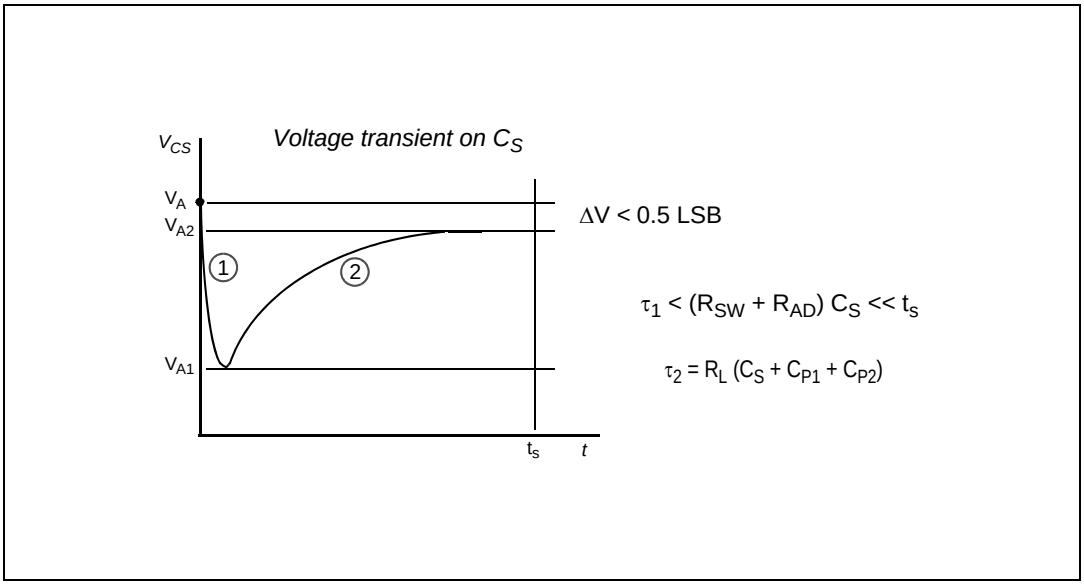


**Figure 14. Transient behavior during sampling phase**

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance $C_{P1}$ and $C_{P2}$ to the sampling capacitance $C_S$ occurs ($C_S$ is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which $C_{P2}$ is reported in parallel to $C_{P1}$ (call $C_P = C_{P1} + C_{P2}$), the two capacitances $C_P$ and $C_S$ are in series, and the time constant is

***Eqn. 5***

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only $C_S$ as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time $t_s$ is always much longer than the internal time constant:

***Eqn. 6***

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll t_s$$

The charge of $C_{P1}$ and $C_{P2}$ is redistributed also on $C_S$, determining a new value of the voltage $V_{A1}$ on the capacitance according to Equation 7:

***Eqn. 7***

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also $C_F$ (that is typically bigger than the on-chip capacitance) through the resistance $R_L$: again considering the worst case in which $C_{P2}$ and $C_S$ were in parallel to $C_{P1}$ (since the time constant in reality would be faster), the time constant is:

***Eqn. 8***

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time $t_s$, a constraints on $R_L$ sizing is obtained:

***Eqn. 9***

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

Of course, $R_L$ shall be sized also according to the current limitation constraints, in combination with $R_S$ (source impedance) and $R_F$ (filter resistance). Being $C_F$ definitively bigger than $C_{P1}$, $C_{P2}$ and $C_S$, then the final voltage $V_{A2}$ (at the end of the charge transfer transient) will be much higher than $V_{A1}$. Equation 10 must be respected (charge balance assuming now $C_S$ already charged at $V_{A1}$):

***Eqn. 10***

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on $C_S$ with respect to the ideal source $V_A$; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time ($t_s$). The filter is typically designed to act as anti-aliasing.

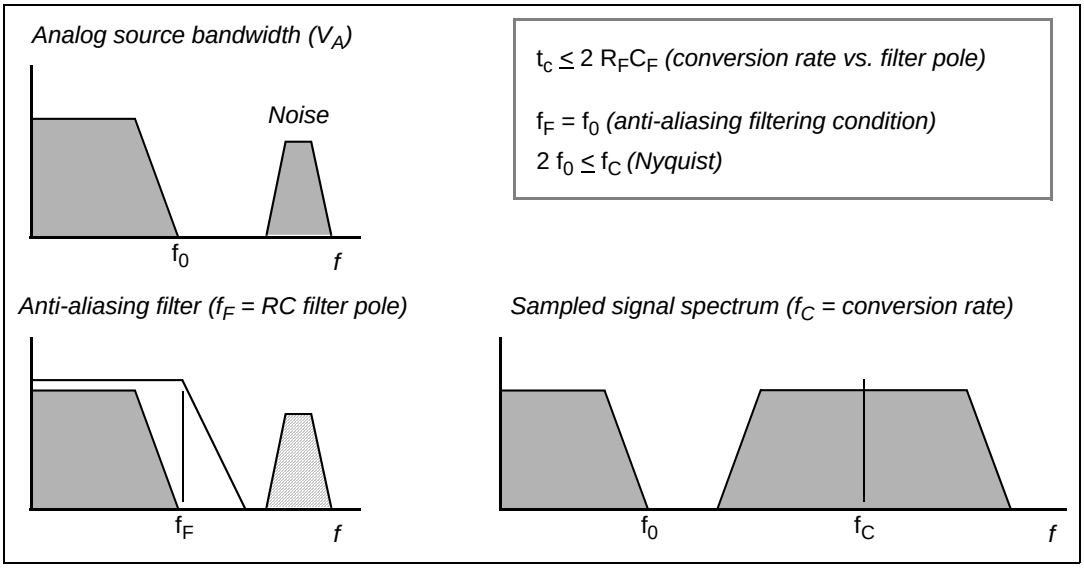


**Figure 15. Spectral representation of input signal**

Calling $f_0$ the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, $f_F$), according to the Nyquist theorem the conversion rate $f_C$ must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period ($t_c$). Again the conversion period $t_c$ is longer than the sampling time $t_s$, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time $t_s$, so the charge level on $C_S$ cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on $C_S$; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on $C_S$:

***Eqn. 11***

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when $V_A$ is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on $C_F$ value:

***Eqn. 12***

$$C_F > 2048 \bullet C_S$$

**Table 41. ADC conversion characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $t_c$ | CC | P | Conversion time[6] $V_{DD}$ = 3.3 V | $f_{ADC}$ = 20 MHz, INPCMP = 0 | | 2.4 | — | — | µs |
| | | | | $f_{ADC}$ = 13.33 MHz, INPCMP = 0 | | — | — | 3.6 | |
| | | P | Conversion time[(6)] $V_{DD}$ = 5.0 V | $f_{ADC}$ = 32 MHz, INPCMP = 0 | | 1.5 | — | — | µs |
| | | | | $f_{ADC}$ = 13.33 MHz, INPCMP = 0 | | — | — | 3.6 | |
| $C_S$ | CC | D | ADC input sampling capacitance | — | | | 5 | | pF |
| $C_{P1}$ | CC | D | ADC input pin capacitance 1 | — | | | 3 | | pF |
| $C_{P2}$ | CC | D | ADC input pin capacitance 2 | — | | | 1 | | pF |
| $C_{P3}$ | CC | D | ADC input pin capacitance 3 | — | | | 1.5 | | pF |
| $R_{SW1}$ | CC | D | Internal resistance of analog source | — | | — | — | 1 | kΩ |
| $R_{SW2}$ | CC | D | Internal resistance of analog source | — | | — | — | 2 | kΩ |
| $R_{AD}$ | CC | D | Internal resistance of analog source | — | | — | — | 0.3 | kΩ |
| $I_{INJ}$ | SR | — | Input current Injection | Current injection on one ADC input, different from the converted one | $V_{DD}$ = 3.3 V ± 10% | –5 | — | 5 | mA |
| | | | | | $V_{DD}$ = 5.0 V ± 10% | –5 | — | 5 | |
| INLP | CC | T | Absolute Integral non-linearity-precise channels | No overload | | — | 1 | 3 | LSB |
| INLX | CC | T | Absolute Integral non-linearity-extended channels | No overload | | — | 1.5 | 5 | LSB |
| DNL | CC | T | Absolute Differential non-linearity | No overload | | — | 0.5 | 1 | LSB |
| $E_O$ | CC | T | Absolute Offset error | — | | — | 2 | — | LSB |
| $E_G$ | CC | T | Absolute Gain error | — | | — | 2 | — | LSB |
| TUEP[7] | CC | P | Total unadjusted error for precise channels, input only pins | Without current injection | | –6 | | 6 | LSB |
| | | T | | With current injection | | –8 | | 8 | |

**Table 42. On-chip peripherals current consumption[1] (continued)**

| Symbol | | C | Parameter | Conditions | | Typical value[2] | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD\_BV(SPI)}$ | CC | T | SPI (DSPI) supply current on $V_{DD\_BV}$ | Ballast static consumption (only clocked) | | 1 | µA |
| | | | | Ballast dynamic consumption (continuous communication):<br>• Baudrate: 2 Mbit/s<br>• Transmission every 8 µs<br>• Frame: 16 bits | | 16 × $f_{periph}$ | µA |
| $I_{DD\_BV(ADC)}$ | CC | T | ADC supply current on $V_{DD\_BV}$ | $V_{DD}$ = 5.5 V | Ballast static consumption (no conversion) | 41 × $f_{periph}$ | µA |
| | | | | | Ballast dynamic consumption (continuous conversion)[3] | 5 × $f_{periph}$ | µA |
| $I_{DD\_HV\_ADC(ADC)}$ | CC | T | ADC supply current on $V_{DD\_HV\_ADC}$ | $V_{DD}$ = 5.5 V | Analog static consumption (no conversion) | 2 × $f_{periph}$ | µA |
| | | | | | Analog dynamic consumption (continuous conversion) | 75 × $f_{periph}$ + 32 | µA |
| $I_{DD\_HV(FLASH)}$ | CC | T | CFlash + DFlash supply current on $V_{DD\_HV}$ | $V_{DD}$ = 5.5 V | — | 8.21 | mA |
| $I_{DD\_HV(PLL)}$ | CC | T | PLL supply current on $V_{DD\_HV}$ | $V_{DD}$ = 5.5 V | — | 30 × $f_{periph}$ | µA |

1 Operating conditions: $T_A$ = 25 °C, $f_{periph}$ = 8 MHz to 48 MHz

2 $f_{periph}$ is an absolute value.

3 During the conversion, the total current consumption is given from the sum of the static and dynamic consumption, i.e., (41 + 5) × $f_{periph}$.

## 4.18.2 DSPI characteristics

**Table 43. DSPI characteristics[1]**

| No. | Symbol | | C | Parameter | | DSPI0/DSPI1 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| 1 | $t_{SCK}$ | SR | D | SCK cycle time | Master mode (MTFE = 0) | 125 | — | — | ns |
| | | | D | | Slave mode (MTFE = 0) | 125 | — | — | |
| | | | D | | Master mode (MTFE = 1) | 83 | — | — | |
| | | | D | | Slave mode (MTFE = 1) | 83 | — | — | |
| — | $f_{DSPI}$ | SR | D | DSPI digital controller frequency | | — | — | $f_{CPU}$ | MHz |

**Table 43. DSPI characteristics[1] (continued)**

| No. | Symbol | | C | Parameter | | DSPI0/DSPI1 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| — | $\Delta t_{CSC}$ | CC | D | Internal delay between pad associated to SCK and pad associated to CSn in master mode | Master mode | — | — | 130[2] | ns |
| — | $\Delta t_{ASC}$ | CC | D | Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1→1 | Master mode | — | — | 130(2) | ns |
| 2 | $t_{CSCext}$[3] | SR | D | CS to SCK delay | Slave mode | 32 | — | — | ns |
| 3 | $t_{ASCext}$[4] | SR | D | After SCK delay | Slave mode | $1/f_{DSPI} + 5$ | — | — | ns |
| 4 | $t_{SDC}$ | CC | D | SCK duty cycle | Master mode | — | $t_{SCK}/2$ | — | ns |
| | | SR | D | | Slave mode | $t_{SCK}/2$ | — | — | |
| 5 | $t_A$ | SR | D | Slave access time | — | $1/f_{DSPI} + 70$ | — | — | ns |
| 6 | $t_{DI}$ | SR | D | Slave SOUT disable time | — | 7 | — | — | ns |
| 7 | $t_{PCSC}$ | SR | D | PCS*x* to $\overline{\text{PCSS}}$ time | — | 0 | — | — | ns |
| 8 | $t_{PASC}$ | SR | D | $\overline{\text{PCSS}}$ to PCS*x* time | — | 0 | — | — | ns |
| 9 | $t_{SUI}$ | SR | D | Data setup time for inputs | Master mode | 43 | — | — | ns |
| | | | | | Slave mode | 5 | — | — | |
| 10 | $t_{HI}$ | SR | D | Data hold time for inputs | Master mode | 0 | — | — | ns |
| | | | | | Slave mode | 2[5] | — | — | |
| 11 | $t_{SUO}$[6] | CC | D | Data valid after SCK edge | Master mode | — | — | 32 | ns |
| | | | | | Slave mode | — | — | 52 | |
| 12 | $t_{HO}$(6) | CC | D | Data hold time for outputs | Master mode | 0 | — | — | ns |
| | | | | | Slave mode | 8 | — | — | |

1 Operating conditions: $C_{OUT}$ = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns

2 Maximum is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM pad

3 The $t_{CSC}$ delay value is configurable through a register. When configuring $t_{CSC}$ (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than $\Delta t_{CSC}$ to ensure positive $t_{CSCext}$.

4 The $t_{ASC}$ delay value is configurable through a register. When configuring $t_{ASC}$ (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than $\Delta t_{ASC}$ to ensure positive $t_{ASCext}$.

5 This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR.

6 SCK and SOUT configured as MEDIUM pad

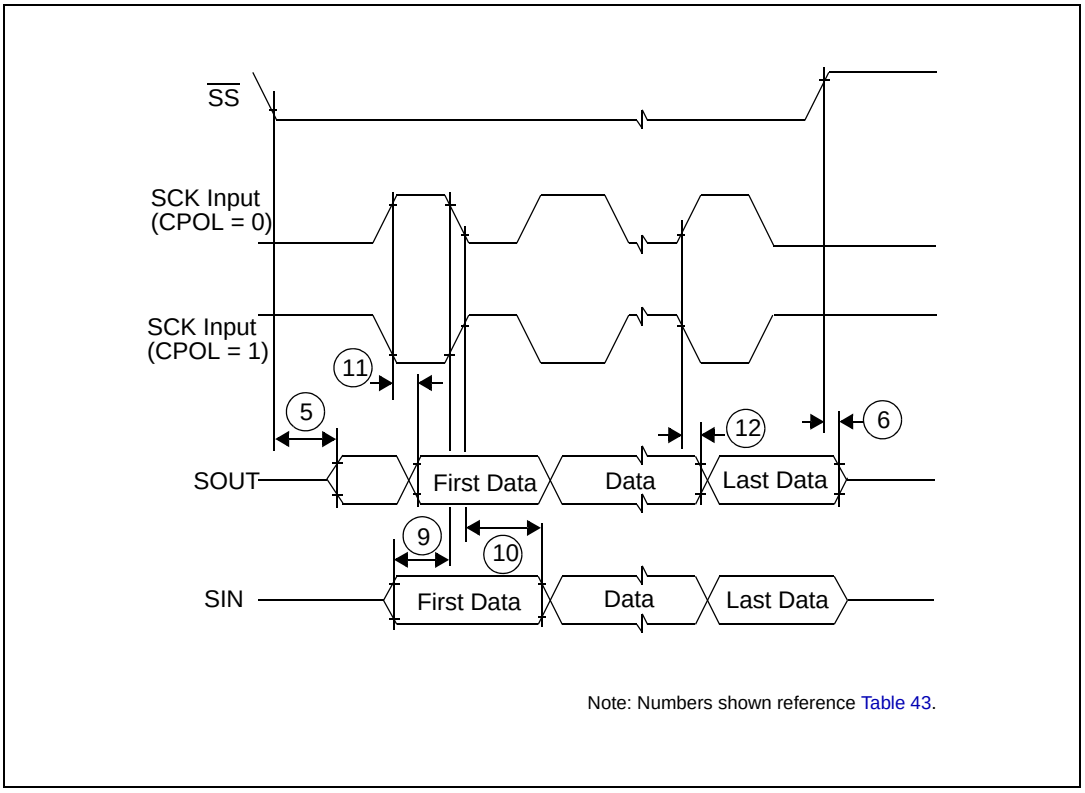


**Figure 19. DSPI classic SPI timing – slave, CPHA = 1**

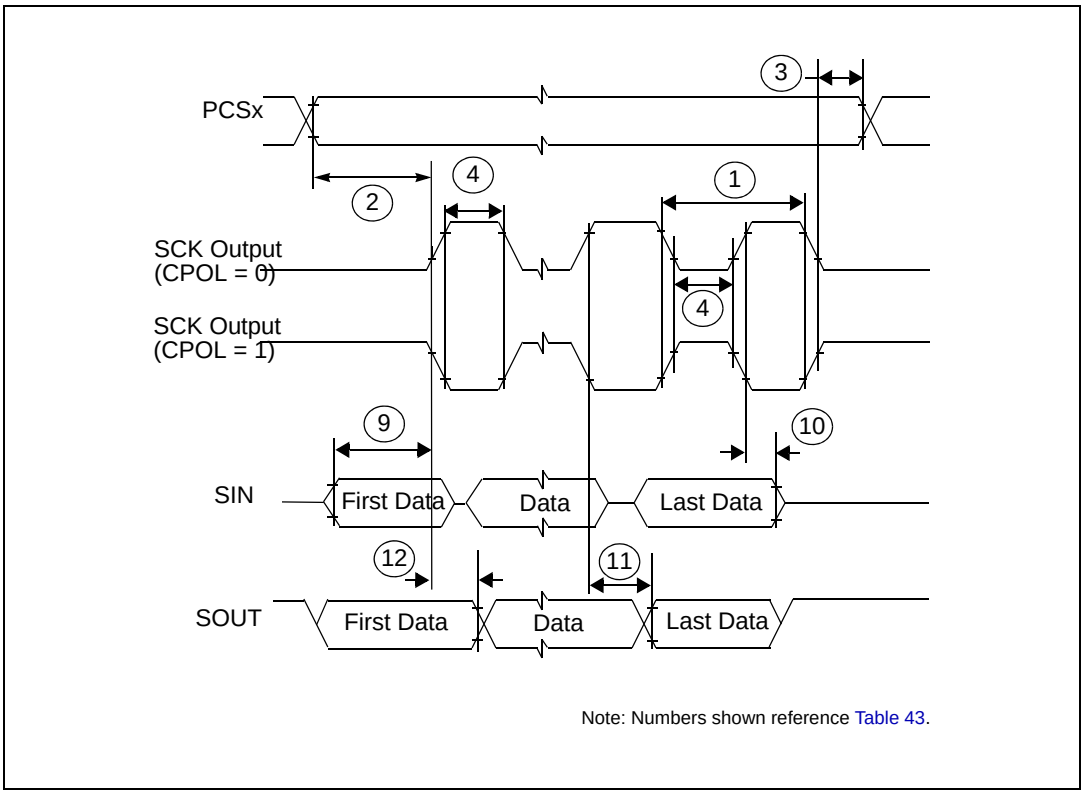


**Figure 20. DSPI modified transfer format timing – master, CPHA = 0**

# 6 Ordering information

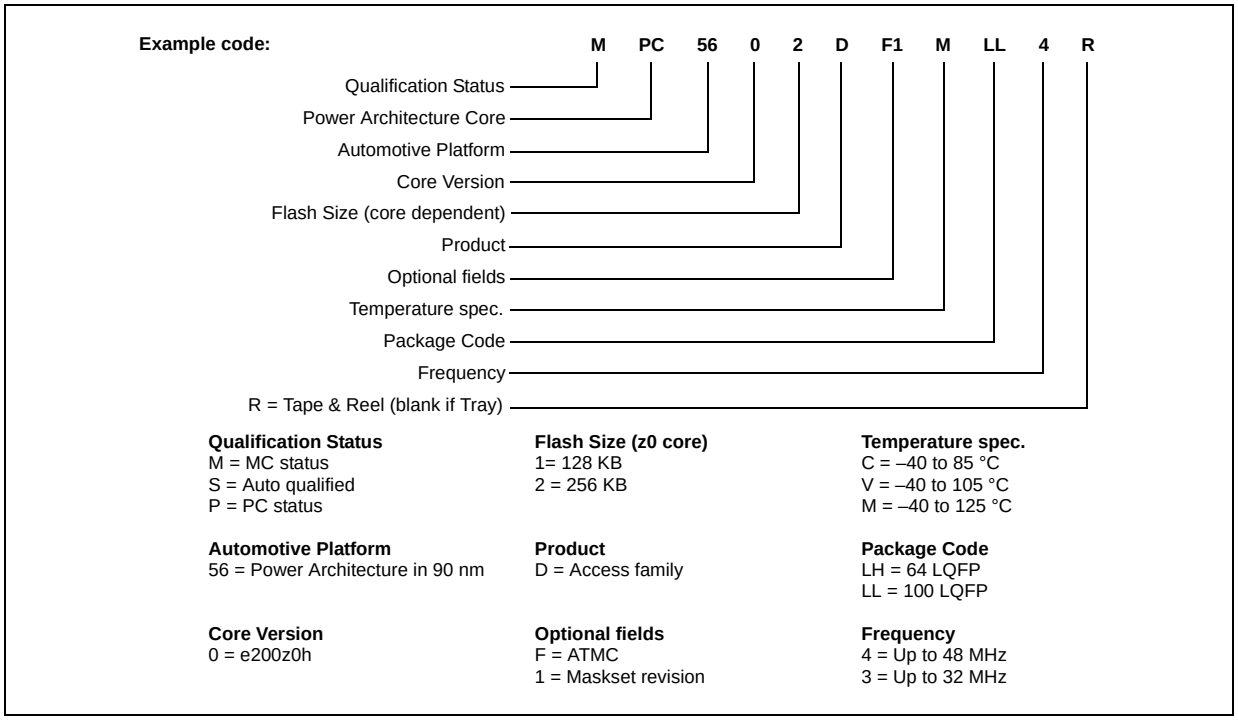


**Figure 32. Commercial product code structure**

# 7 Document revision history

Table 45 summarizes revisions to this document.

**Table 45. Revision history**

| Revision | Date | Description of Changes |
|---|---|---|
| 1 | 30 Sep 2009 | Initial release |
| 2 | 18 Feb 2010 | Updated the following tables:<br>- Absolute maximum ratings<br>- Low voltage power domain electrical characteristics;<br>- On-chip peripherals current consumption<br>- DSPI characteristics;<br>- JTAG characteristics;<br>- ADC conversion characteristics;<br>Inserted a note on “Flash power supply DC characteristics” section. |
| 3 | 10 Aug 2010 | “Features” section: Updated information concerning eMIOS, ADC, LINFlex, Nexus and low power capabilities<br>“MPC5602D device comparison” table: updated the “Execution speed” row<br>“MPC5602D series block diagram” figure:<br>• updated max number of Crossbar Switches<br>• updated Legend<br>“MPC5602D series block summary” table: added contents concernig the eDMA block<br>“100 LQFP pin configuration (top view)” figure:<br>• removed alternate functions<br>• updated supply pins<br>“64 LQFP pin configuration (top view)” figure: removed alternate functions<br>Added “Pin muxing” section<br>“NVUSRO register” section: Deleted “NVUSRO[WATCHDOG_EN] field description“ section<br>“Recommended operating conditions (3.3 V)” table:<br>• $TV_{DD}$: deleted min value<br>• In footnote No. 3, changed capacitance value between $V_{DD\_BV}$ and $V_{SS\_LV}$<br>“Recommended operating conditions (5.0 V)” table: deleted $TV_{DD}$ min value<br>“LQFP thermal characteristics” table: changed $R_{\theta JC}$ values<br>“I/O input DC electrical characteristics” table:<br>• $W_{FI}$: updated max value<br>• $W_{NFI}$: updated min value<br>“I/O consumption” table: removed $I_{DYNSEG}$ row<br>Added “I/O weight” table<br>“Program and erase specifications (Code Flash)” table: deleted $T_{Bank\_C}$ row<br>Updated the following tables:<br>• “Voltage regulator electrical characteristics”<br>• “Low voltage monitor electrical characteristics”<br>• “Low voltage power domain electrical characteristics”<br>• “Start-up time/Switch-off time”<br>• “Fast external crystal oscillator (4 to 16 MHz) electrical characteristics”<br>• “FMPLL electrical characteristics”<br>• “Fast internal RC oscillator (16 MHz) electrical characteristics”<br>• “ADC conversion characteristics”<br>• “On-chip peripherals current consumption”<br>• “DSPI characteristics”<br>“DSPI characteristics” section: removed “DSPI PCS strobe (PCSS) timing” figure |
| 3 (continued) | 10 Aug 2010 | “Ordering information” section: removed “Orderable part number summary“ table |

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