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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 16
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5602df1mlh4r

1 Introduction

1.1 Document overview

This document describes the device features and highlights the important electrical and physical characteristics.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices designed to be central to the development of the next wave of central vehicle body controller, smart junction box, front module, peripheral body, door control and seat control applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology and designed specifically for embedded applications.

The advanced and cost-efficient e200z0h host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (auxiliary processing unit), providing improved code density. It operates at speeds of up to 48 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with the user's implementations.

The device platform has a single level of memory hierarchy and can support a wide range of on-chip static random access memory (SRAM) and internal flash memory.

Table 1. MPC5602D device comparison

Feature	Device			
	MPC5601DxLH	**MPC5601DxLL**	**MPC5602DxLH**	**MPC5602DxLL**
CPU	e200z0h			
Execution speed	Static – up to 48 MHz			
Code flash memory	128 KB		256 KB	
Data flash memory	64 KB (4 × 16 KB)			
SRAM	12 KB		16 KB	
eDMA	16 ch			
ADC (12-bit)	16 ch	33 ch	16 ch	33 ch
CTU	16 ch			
Total timer I/O[1] eMIOS	14 ch, 16-bit	28 ch, 16-bit	14 ch, 16-bit	28 ch, 16-bit
• Type X[2]	2 ch	5 ch	2 ch	5 ch
• Type Y[3]	—	9 ch	—	9 ch
• Type G[4]	7 ch	7 ch	7 ch	7 ch
• Type H[5]	4 ch	7 ch	4 ch	7 ch
SCI (LINFlex)	3			
SPI (DSPI)	2			
CAN (FlexCAN)	1			
GPIO[6]	45	79	45	79

Table 2. MPC5602D series block summary (continued)

Block	Function
Real-time counter (RTC)	Provides a free-running counter and interrupt generation capability that can be used for timekeeping applications
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available LQFP pinouts are provided in the following figures. For pin signal descriptions, please refer to Table 5.

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC1_X[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	67
Port C									
PC[0][6]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	87
PC[1][6]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F	Tristate	54	82
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 — — EIRQ[5]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	M	Tristate	50	78
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 —	GPIO[35] CS0_1 MA[0] — EIRQ[6]	SIUL DSPI_1 ADC — SIUL	I/O I/O O — I	S	Tristate	49	77
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 EIRQ[18]	SIUL — — — DSPI_1 SIUL	I/O — — — I I	M	Tristate	62	92
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 — — EIRQ[7]	SIUL DSPI_1 — — SIUL	I/O O — — I	M	Tristate	61	91
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	16	25

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKPU[12][3]	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	17	26
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlex_2 eMIOS_0 —	I/O O I/O —	S	Tristate	63	99
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13][3]	SIUL — eMIOS_0 — LINFlex_2 WKPU	I/O — I/O — I I	S	Tristate	2	2
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] — — MA[1]	SIUL — — ADC	I/O — — O	M	Tristate	13	22
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 —	GPIO[43] — — MA[2] WKPU[5][3]	SIUL — — ADC WKPU	I/O — — O I	S	Tristate	—	21
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — EIRQ[19]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	97
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	98
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] — — EIRQ[8]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	—	3
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] — — EIRQ[20]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	4

[6] Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
If the user configures these JTAG pins in GPIO mode the device is no longer compliant with IEEE 1149.1 2001.

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 6 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.3 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

4.3.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. Table 7 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 7. PAD3V5V field description

Value[1]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

4.3.2 NVUSRO[OSCILLATOR_MARGIN] field description

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value. Table 8 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 8. OSCILLATOR_MARGIN field description

Value[1]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1 Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

4.3.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. Table 8 shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 9. WATCHDOG_EN field description

Value[1]	Description
0	Disable after reset)
1	Enable after reset

1 Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

4.4 Absolute maximum ratings

Table 10. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V

Table 10. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{DD_BV}	SR	Voltage on VDD_BV (regulator supply) pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment[1]	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
I_{CORELV}	SR	Low voltage static current sink through VDD_BV	—	—	150	mA
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C

1 Supply segments are described in Section 4.7.5, I/O pad current specification.

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

4.5 Recommended operating conditions

Table 11. Recommended operating conditions (3.3 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SS}	SR	—	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	—	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	—	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V

Table 11. Recommended operating conditions (3.3 V) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DD_BV}[3]	SR	—	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
				Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}[4]	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	3.0[5]	3.6	V
				Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	—	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
				Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	—	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	—	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
TV_{DD}	SR	—	V_{DD} slope to ensure correct power up[6]	—	—	0.25	V/µs
T_{A} C-Grade Part	SR	—	Ambient temperature under bias	$f_{CPU} \leq 48$ MHz	–40	85	°C
T_{J} C-Grade Part	SR	—	Junction temperature under bias		–40	110	
T_{A} V-Grade Part	SR	—	Ambient temperature under bias		–40	105	
T_{J} V-Grade Part	SR	—	Junction temperature under bias		–40	130	
T_{A} M-Grade Part	SR	—	Ambient temperature under bias		–40	125	
T_{J} M-Grade Part	SR	—	Junction temperature under bias		–40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

2 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

3 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).

4 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

5 Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.

6 Guaranteed by device validation

Table 12. Recommended operating conditions (5.0 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SS}	SR	—	Digital ground on VSS_HV pins	—	0	0	V

Table 21. I/O weight[1]

Pad	100 LQFP/64 LQFP			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PB[3]	9%	9%	10%	10%
PC[9]	8%	8%	10%	10%
PC[14]	8%	8%	10%	10%
PC[15]	8%	11%	9%	10%
PA[2]	8%	8%	9%	9%
PE[0]	7%	7%	9%	9%
PA[1]	7%	7%	8%	8%
PE[1]	7%	10%	8%	8%
PE[8]	6%	9%	8%	8%
PE[9]	6%	6%	7%	7%
PE[10]	6%	6%	7%	7%
PA[0]	5%	7%	6%	7%
PE[11]	5%	5%	6%	6%
PC[11]	7%	7%	9%	9%
PC[10]	8%	11%	9%	10%
PB[0]	8%	11%	9%	10%
PB[1]	8%	8%	10%	10%
PC[6]	8%	8%	10%	10%
PC[7]	8%	8%	10%	10%
PA[15]	8%	11%	9%	10%
PA[14]	7%	11%	9%	9%
PA[4]	7%	7%	8%	8%
PA[13]	7%	10%	8%	9%
PA[12]	7%	7%	8%	8%
PB[9]	1%	1%	1%	1%
PB[8]	1%	1%	1%	1%
PB[10]	5%	5%	6%	6%
PD[0]	1%	1%	1%	1%
PD[1]	1%	1%	1%	1%
PD[2]	1%	1%	1%	1%
PD[3]	1%	1%	1%	1%
PD[4]	1%	1%	1%	1%

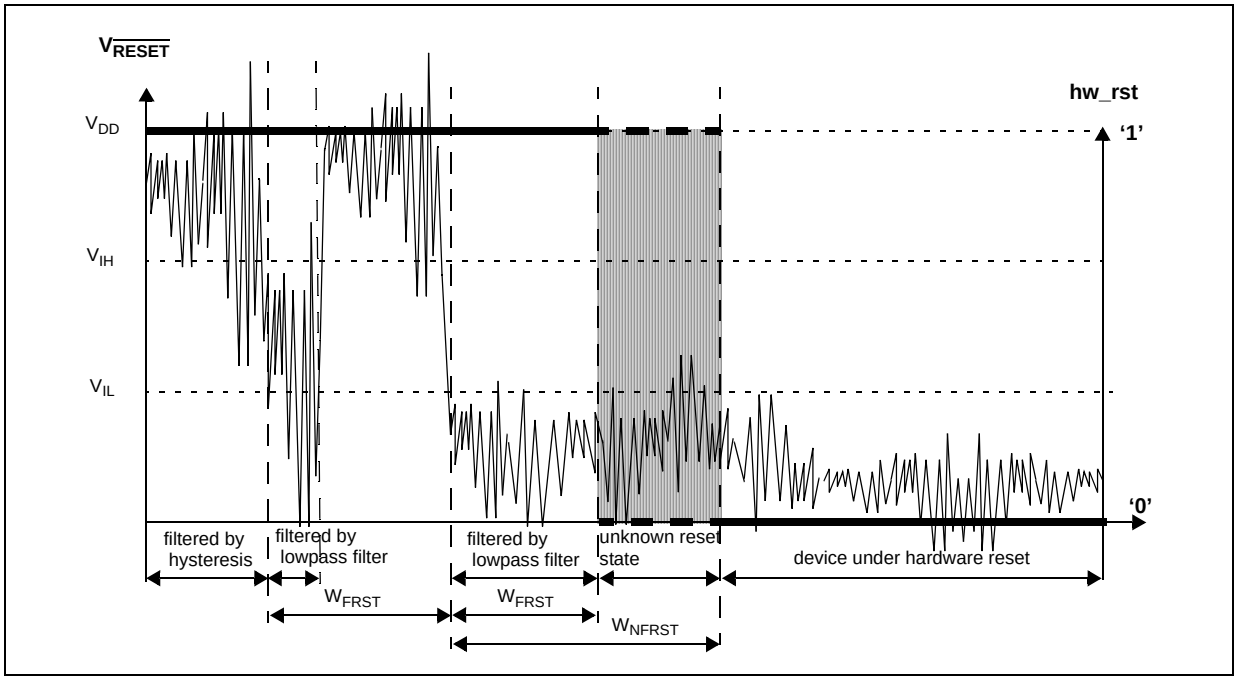

Figure 6. Noise filtering on reset signal

Table 22. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

Table 24. Low voltage detector electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORUP}	SR	P	Supply for functional POR module	T_A = 25 °C, after trimming	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold		1.5	—	2.6	V
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold		—	—	2.95	V
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold		2.6	—	2.9	V
$V_{LVDHV3BH}$	CC	P	LVDHV3B low voltage detector high threshold		—	—	2.95	V
$V_{LVDHV3BL}$	CC	P	LVDHV3B low voltage detector low threshold		2.6	—	2.9	V
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5	V
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4	V
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	1.16	V
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.16	V

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.10 Power consumption

Table 25 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 25. Power consumption on VDD_BV and VDD_HV

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—		—	90	130[3]	mA
I_{DDRUN}[4]	CC	T	RUN mode typical average current[5]	f_{CPU} = 8 MHz		—	7	—	mA
		T		f_{CPU} = 16 MHz		—	18	—	
		T		f_{CPU} = 32 MHz		—	29	—	
		P		f_{CPU} = 48 MHz		—	40	100	
I_{DDHALT}	CC	C	HALT mode current[6]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	8	15	mA
		P			T_A = 125 °C	—	14	25	
I_{DDSTOP}	CC	P	STOP mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	180	700[8]	µA
		D			T_A = 55 °C	—	500	—	
		D			T_A = 85 °C	—	1	6(8)	mA
		D			T_A = 105 °C	—	2	9(8)	
		P			T_A = 125 °C	—	4.5	12(8)	

Table 25. Power consumption on VDD_BV and VDD_HV (continued) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$I_{DDSTDBY}$	CC	P	STANDBY mode current[9]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	30	100	µA
		D			T_A = 55 °C	—	75	—	
		D			T_A = 85 °C	—	180	700	
		D			T_A = 105 °C	—	315	1000	
		P			T_A = 125 °C	—	560	1700	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

3 Higher current may be sinked by device during power-up and standby exit. Please refer to in-rush average current on Table 23.

4 RUN current measured with typical application with accesses on both flash memory and SRAM.

5 Only for the “P” classification: Code fetched from SRAM: serial IPs CAN and LIN in loop-back mode, DSPI as Master, PLL as system clock (3 × Multiplier) peripherals on (eMIOS/CTU/ADC) and running at maximum frequency, periodic SW/WDG timer reset enabled.

6 Data flash power down. Code flash in low power. SIRC (128 kHz) and FIRC (16 MHz) on. 10 MHz XTAL clock. FlexCAN: 0 ON (clocked but no reception or transmission). LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON.PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.

7 Only for the “P” classification: No clock, FIRC (16 MHz) off, SIRC (128 kHz) on, PLL off, HPVreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

8 When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

9 Only for the “P” classification: ULPVreg on, HP/LPVreg off, 16 KB SRAM on, device configured for minimum consumption, all possible modules switched off.

4.11 Flash memory electrical characteristics

The data flash operation depends strongly on the code flash operation. If code flash is switched-off, the data flash is disabled.

4.11.1 Program/Erase characteristics

Table 26 shows the program and erase characteristics.

Table 30. Flash power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{FLPW}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} during flash low-power mode	—	Code flash	—	—	910	µA
I_{CFPWD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} during flash power-down mode	—	Code flash	—	—	125	µA
I_{DFPWD}	CC	D			Data flash	—	—	25	µA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.11.3 Start-up/Switch-off timings

Table 31. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$t_{FLARSTEXIT}$	CC	T	Delay for flash module to exit reset mode	Code flash	—	—	125	µs
				Data flash	—	—	150	µs
$t_{FLALPEXIT}$	CC	T	Delay for flash module to exit low-power mode[2]	Code flash	—	—	0.5	µs
$t_{FLAPDEXIT}$	CC	T	Delay for flash module to exit power-down mode	Code flash	—	—	30	µs
				Data flash	—	—	30[3]	µs
$t_{FLALPENTRY}$	CC	T	Delay for flash module to enter low-power mode	Code flash	—	—	0.5	µs
$t_{FLAPDENTRY}$	CC	T	Delay for flash module to enter power-down mode	Code flash	—	—	1.5	µs
				Data flash	—	—	4(3)	µs

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Data flash does not support low-power mode

3 If code flash is already switched-on.

4.12 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.12.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:

— Corrupted program counter
— Unexpected reset
— Critical data corruption (control registers...)

- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.12.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.

Table 32. EMI radiated emission measurement[1] [2]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150	—	1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	48	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, 100 LQFP package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 48 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14	dBµV

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.12.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.12.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 33. ESD absolute maximum ratings[1] [2]

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	CC	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	CC	T	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
$V_{ESD(CDM)}$	CC	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	V
						750 (corners)	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.12.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 34. Latch-up results

Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

Table 35. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance (ESR) Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout $C_1 = C_2$ (pF)[1]	Shunt capacitance between xtalout and xtalin C0[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

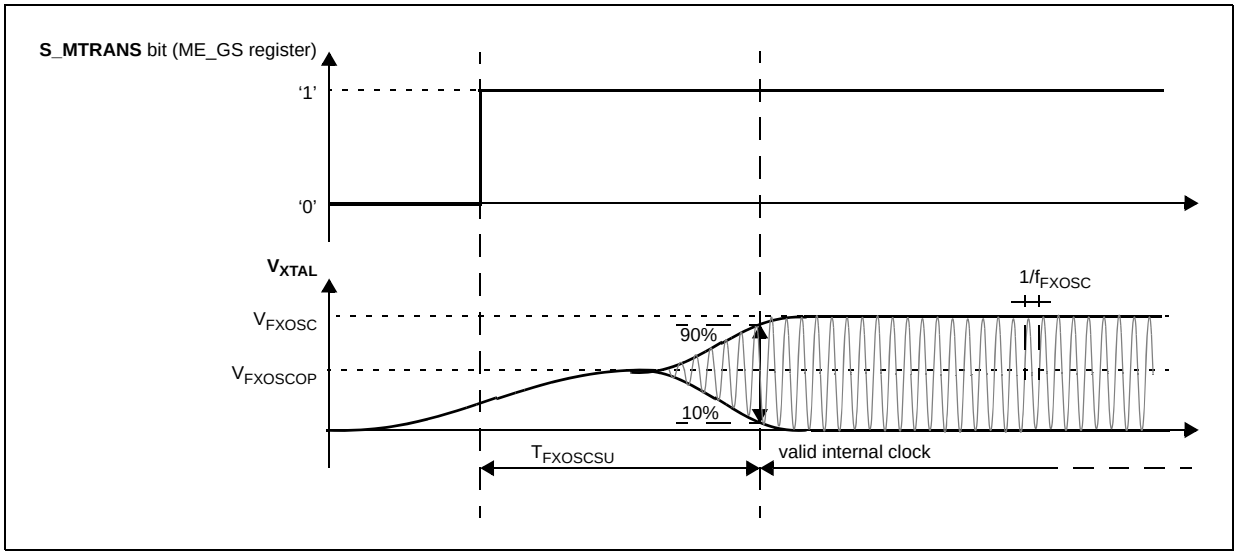

Figure 10. Fast external crystal oscillator (4 to 16 MHz) timing diagram

Table 36. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	16.0	MHz
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
$V_{FXOSCOP}$	CC	P	Oscillation operating point	—	—	0.95		V
I_{FXOSC}[2]	CC	T	Fast external crystal oscillator consumption	—	—	2	3	mA
$t_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD}$	—	V_{DD}+0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.4	—	$0.35V_{DD}$	V

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals)

Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
t_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	V_{DD} = 5.0 V ± 10%		—	1.1	2.0	µs
$\Delta_{FIRCPRE}$	CC	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C		–1	—	1	%
$\Delta_{FIRCTRIM}$	CC	C	Fast internal RC oscillator trimming step	T_A = 25 °C		—	1.6		%
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation in temperature and supply with respect to f_{FIRC} at T_A = 55 °C in high-frequency configuration	—		–5	—	5	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

Table 39. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100	—	150	
I_{SIRC}[2],	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
t_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	

4.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{p2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{p2} equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_c \times (C_S+C_{p2}))$, where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{p2}) and the sum of $R_S + R_F$, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on a resistive path.

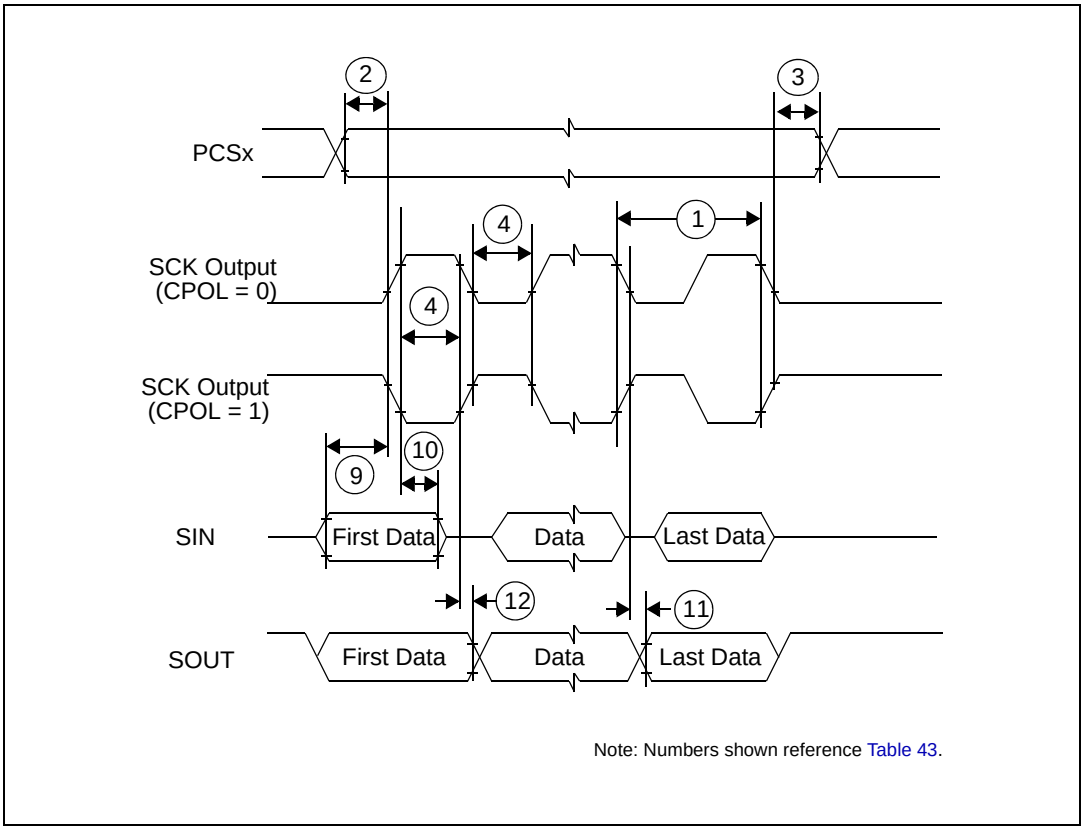

Figure 16. DSPI classic SPI timing – master, CPHA = 0