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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 16
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5602df1mll4

1 Introduction

1.1 Document overview

This document describes the device features and highlights the important electrical and physical characteristics.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices designed to be central to the development of the next wave of central vehicle body controller, smart junction box, front module, peripheral body, door control and seat control applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology and designed specifically for embedded applications.

The advanced and cost-efficient e200z0h host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (auxiliary processing unit), providing improved code density. It operates at speeds of up to 48 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with the user's implementations.

The device platform has a single level of memory hierarchy and can support a wide range of on-chip static random access memory (SRAM) and internal flash memory.

Table 1. MPC5602D device comparison

Feature	Device			
	MPC5601DxLH	**MPC5601DxLL**	**MPC5602DxLH**	**MPC5602DxLL**
CPU	e200z0h			
Execution speed	Static – up to 48 MHz			
Code flash memory	128 KB		256 KB	
Data flash memory	64 KB (4 × 16 KB)			
SRAM	12 KB		16 KB	
eDMA	16 ch			
ADC (12-bit)	16 ch	33 ch	16 ch	33 ch
CTU	16 ch			
Total timer I/O[1] eMIOS	14 ch, 16-bit	28 ch, 16-bit	14 ch, 16-bit	28 ch, 16-bit
• Type X[2]	2 ch	5 ch	2 ch	5 ch
• Type Y[3]	—	9 ch	—	9 ch
• Type G[4]	7 ch	7 ch	7 ch	7 ch
• Type H[5]	4 ch	7 ch	4 ch	7 ch
SCI (LINFlex)	3			
SPI (DSPI)	2			
CAN (FlexCAN)	1			
GPIO[6]	45	79	45	79

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — ADC1_P[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	55
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ADC1_S[4] WKPU[25][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	30	39
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ADC1_S[5] WKPU[26][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	29	38
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ADC1_S[6] WKPU[8][3]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	40
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC1_S[12]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	59
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC1_X[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	61
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC1_X[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	63
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC1_X[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	65

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 —	GPIO[64] E0UC[16] — — WKPU[6][3]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	—	6
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	8
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 — —	GPIO[66] E0UC[18] — — EIRQ[21] SIN_1	SIUL eMIOS_0 — — SIUL DSPI_1	I/O I/O — — I I	M	Tristate	—	89
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	—	90
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	—	93
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	M	Tristate	—	94
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC SIUL	I/O I/O O O I	M	Tristate	—	95
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC SIUL	I/O I/O O O I	M	Tristate	—	96
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] — E0UC[22] —	SIUL — eMIOS_0 —	I/O — I/O —	M	Tristate	—	9

[6] Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
If the user configures these JTAG pins in GPIO mode the device is no longer compliant with IEEE 1149.1 2001.

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 6 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 6. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.3 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

Table 17. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	$V_{DD} – 0.8$	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		P			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
		C			I_{OL} = 100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 21. I/O weight[1] (continued)

Pad	100 LQFP/64 LQFP			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PC[0]	6%	9%	7%	8%
PE[2]	7%	10%	8%	9%
PE[3]	7%	10%	9%	9%
PC[5]	8%	11%	9%	10%
PC[4]	8%	11%	9%	10%
PE[4]	8%	12%	10%	10%
PE[5]	8%	12%	10%	11%
PE[6]	9%	12%	10%	11%
PE[7]	9%	12%	10%	11%
PC[12]	9%	13%	11%	11%
PC[13]	9%	9%	11%	11%
PC[8]	9%	9%	11%	11%
PB[2]	9%	13%	11%	12%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 SRC: “Slew Rate Control” bit in SIU_PCR

4.8 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

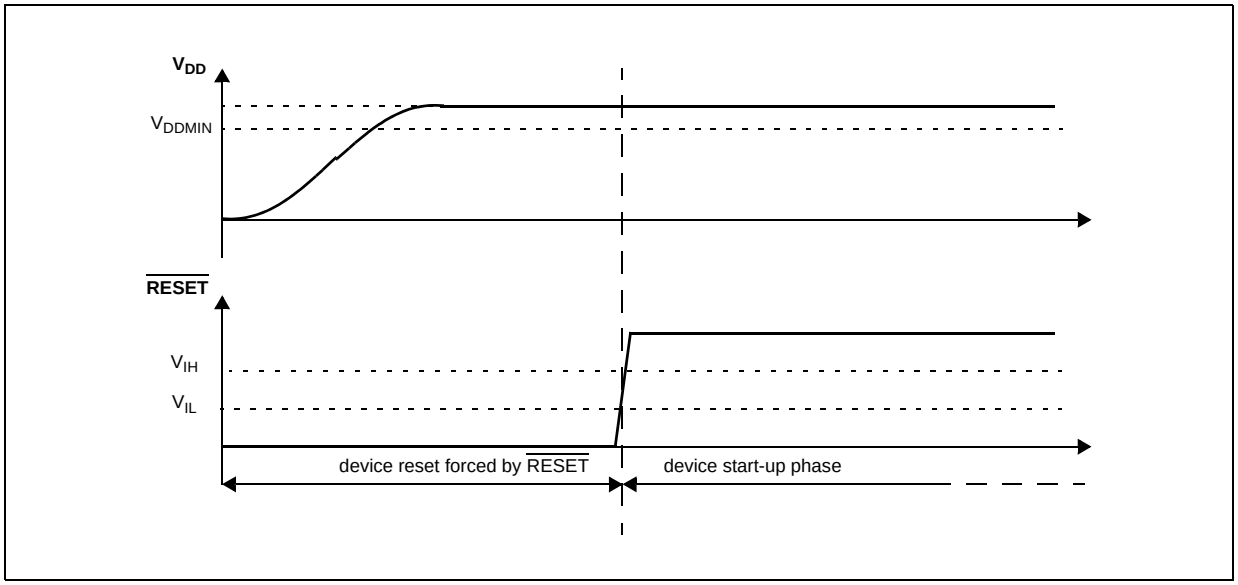

Figure 5. Start-up reset requirements

Table 23. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low-power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low-power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up[5]	—	—	—	300[6]	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.

3 This value is acceptable to guarantee operation from 4.5 V to 5.5 V.

4 External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

5 In-rush average current is seen only for short time during power-up and on standby exit (maximum 20 µs, depending on external capacitances to be loaded).

6 The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

Table 28. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block over the operating temperature range (T_J)	16 KB blocks	100,000	—	—	cycles
				32 KB blocks	10,000	100,000	—	cycles
				128 KB blocks	1,000	100,000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	
				Blocks with 10,001–100,000 P/E cycles	5	—	—	

1 Ambient temperature averaged over application duration. It is recommended not to exceed the product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 29. Flash memory read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{CFREAD}	CC	P	Maximum working frequency for reading code flash memory at given number of wait states in worst conditions	2 wait states	48	MHz
		C		0 wait states	20	
f_{DFREAD}	CC	P	Maximum working frequency for reading data flash memory at given number of wait states in worst conditions	6 wait states	48	MHz

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.11.2 Flash power supply DC characteristics

Table 30 shows the power supply DC characteristics on external supply.

NOTE

Power supply for data flash is actually provided by code flash; this means that data flash cannot work if code flash is not powered.

Table 30. Flash power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{CFREAD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} on read access	Flash module read f_{CPU} = 48 MHz	Code flash	—	—	33	mA
I_{DFREAD}	CC	D			Data flash	—	—	4	mA
I_{CFMOD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} on matrix modification (program/erase)	Program/Erase on-going while reading flash registers, f_{CPU} = 48 MHz	Code flash	—	—	33	mA
I_{DFMOD}	CC	D			Data flash	—	—	6	mA

— Corrupted program counter
— Unexpected reset
— Critical data corruption (control registers...)

- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.12.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.

Table 32. EMI radiated emission measurement[1] [2]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150	—	1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	48	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, 100 LQFP package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 48 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14	dBµV

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.12.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.12.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

4.14 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 37. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[2]	—	4	—	48	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle(2)	—	40	—	60	%
f_{PLLOUT}	CC	D	FMPLL output clock frequency	—	16	—	48	MHz
f_{VCO}[3]	CC	P	VCO frequency without frequency modulation	—	256	—	512	MHz
			VCO frequency with frequency modulation	—	245	—	533	
f_{CPU}	SR	—	System clock frequency	—	—	—	48	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 48 MHz, 4,000 cycles	—	—	10	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

3 Frequency modulation is considered ±4%.

4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[2],	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	10	µA

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_s is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll t_s$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_s, a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (t_s). The filter is typically designed to act as anti-aliasing.

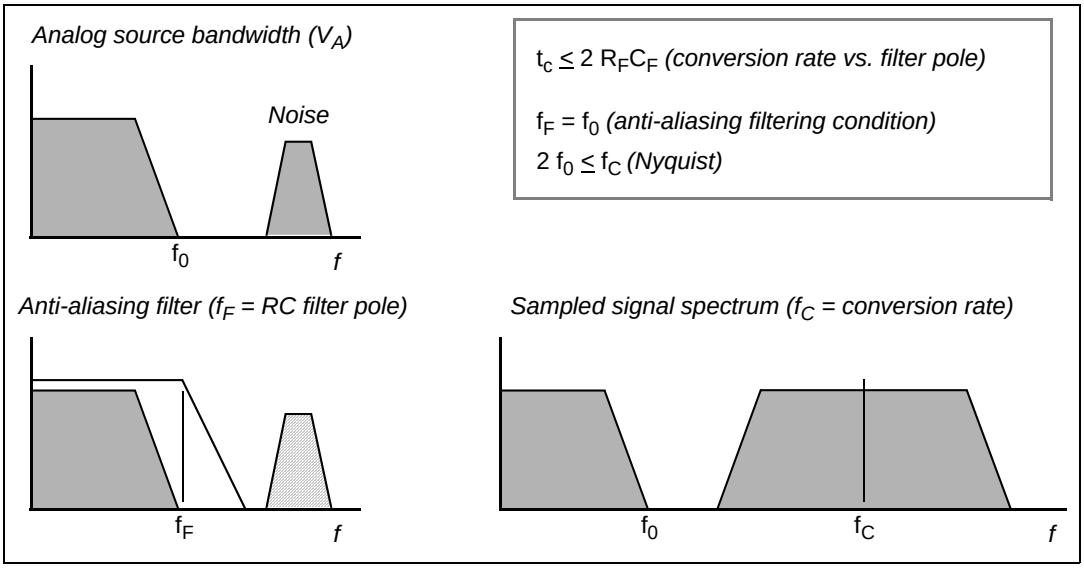

Figure 15. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (t_c). Again the conversion period t_c is longer than the sampling time t_s, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time t_s, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

Table 41. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_c	CC	P	Conversion time[6] V_{DD} = 3.3 V	f_{ADC} = 20 MHz, INPCMP = 0		2.4	—	—	µs
				f_{ADC} = 13.33 MHz, INPCMP = 0		—	—	3.6	
		P	Conversion time[(6)] V_{DD} = 5.0 V	f_{ADC} = 32 MHz, INPCMP = 0		1.5	—	—	µs
				f_{ADC} = 13.33 MHz, INPCMP = 0		—	—	3.6	
C_S	CC	D	ADC input sampling capacitance	—			5		pF
C_{P1}	CC	D	ADC input pin capacitance 1	—			3		pF
C_{P2}	CC	D	ADC input pin capacitance 2	—			1		pF
C_{P3}	CC	D	ADC input pin capacitance 3	—			1.5		pF
R_{SW1}	CC	D	Internal resistance of analog source	—		—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	0.3	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
INLP	CC	T	Absolute Integral non-linearity-precise channels	No overload		—	1	3	LSB
INLX	CC	T	Absolute Integral non-linearity-extended channels	No overload		—	1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload		—	0.5	1	LSB
E_O	CC	T	Absolute Offset error	—		—	2	—	LSB
E_G	CC	T	Absolute Gain error	—		—	2	—	LSB
TUEP[7]	CC	P	Total unadjusted error for precise channels, input only pins	Without current injection		–6		6	LSB
		T		With current injection		–8		8	

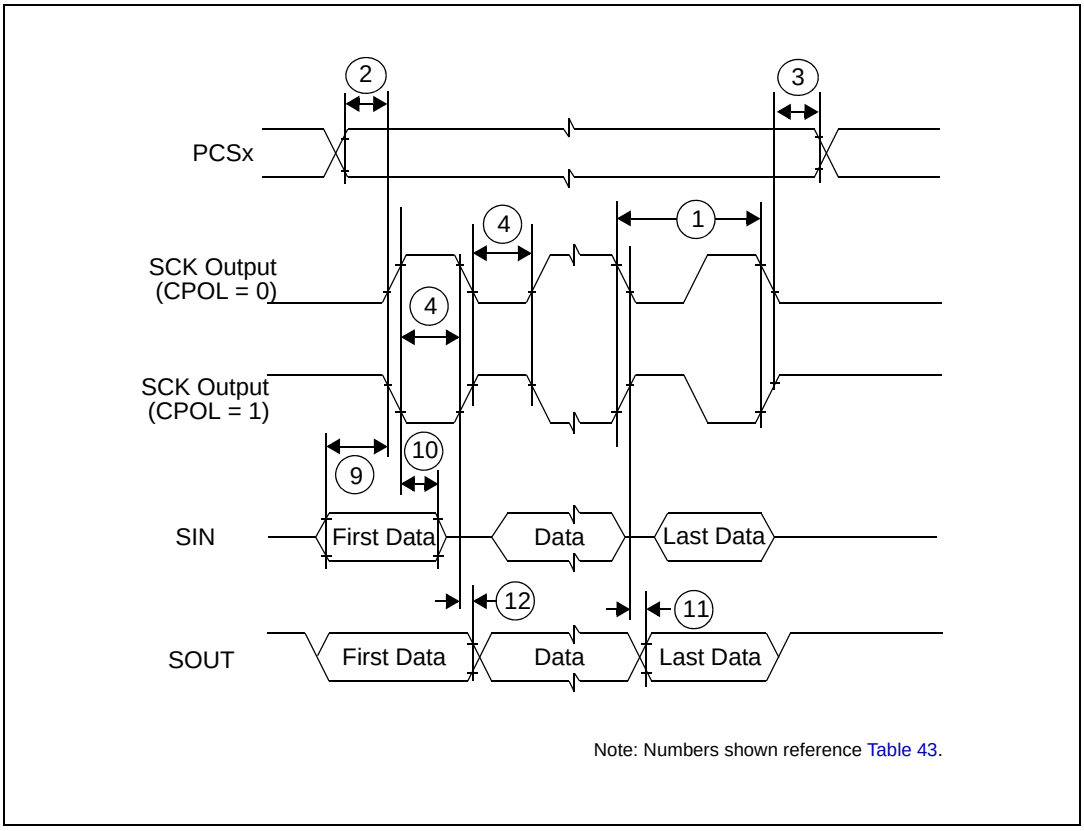

Figure 16. DSPI classic SPI timing – master, CPHA = 0

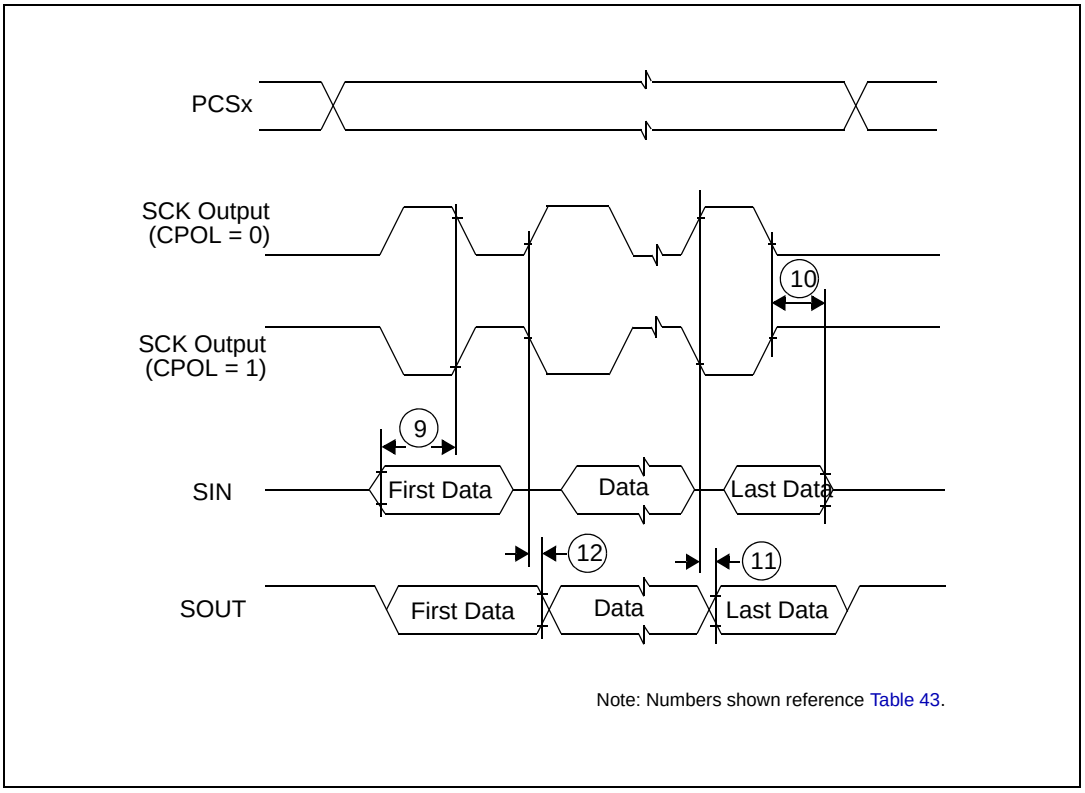

Figure 17. DSPI classic SPI timing – master, CPHA = 1

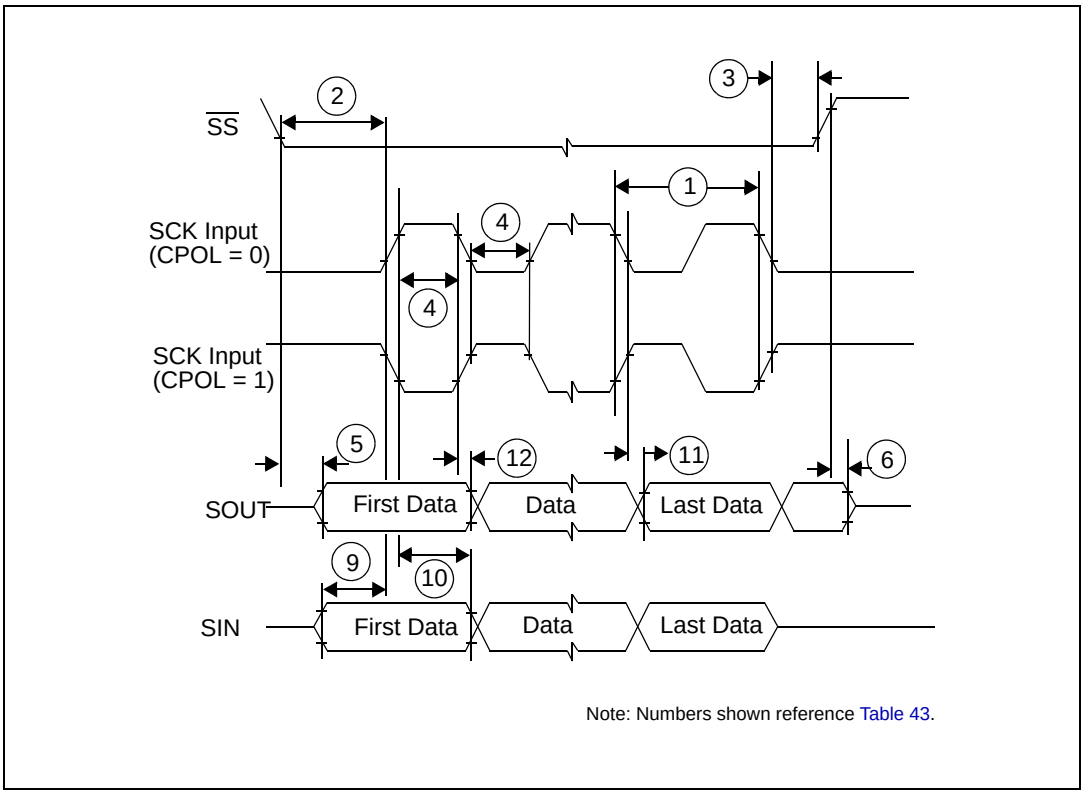

Figure 18. DSPI classic SPI timing – slave, CPHA = 0

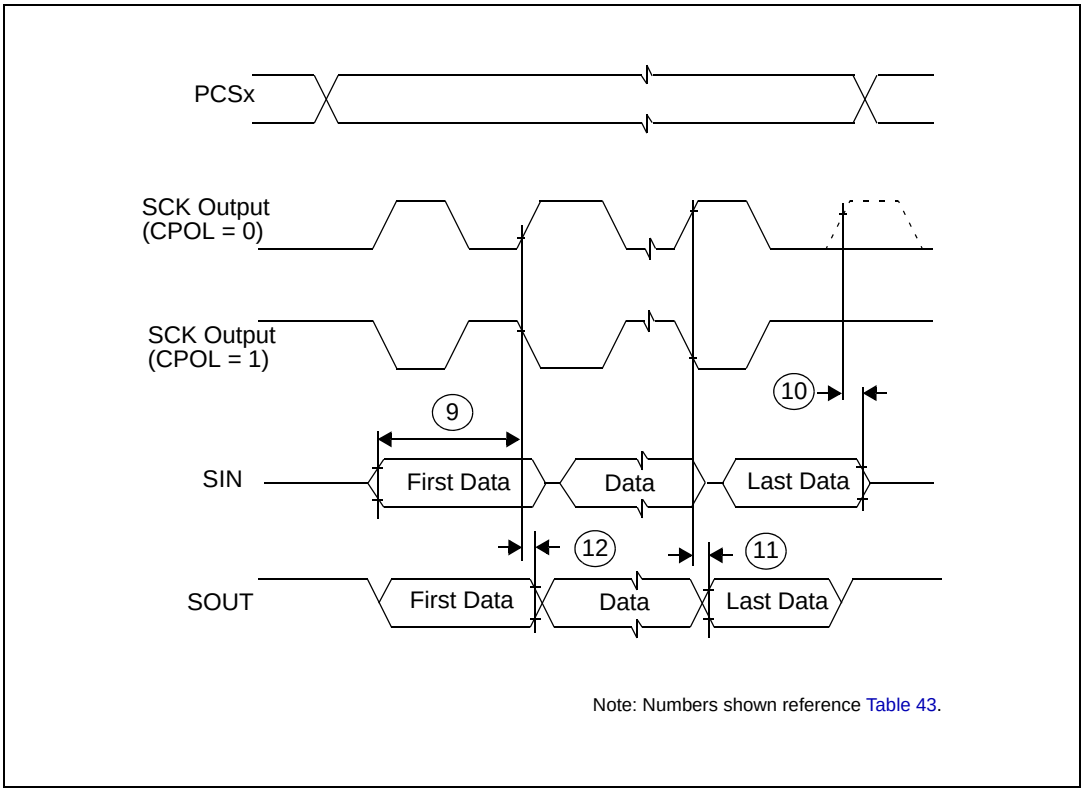

Figure 21. DSPI modified transfer format timing – master, CPHA = 1

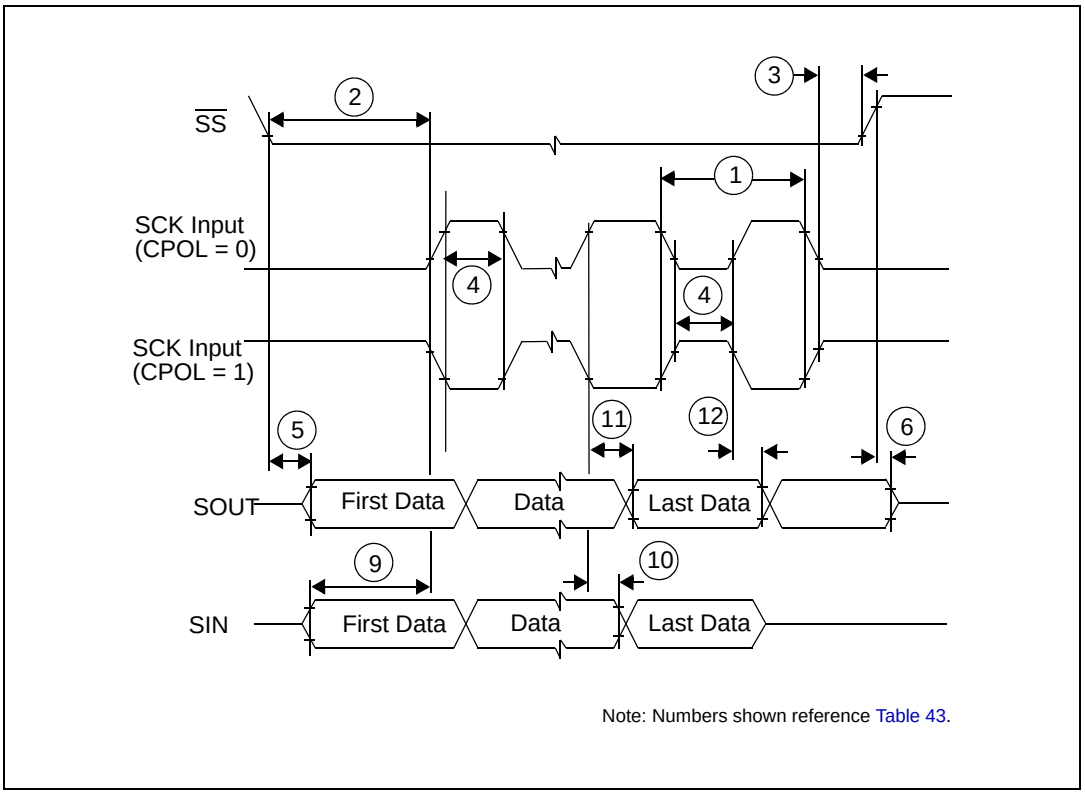

Figure 22. DSPI modified transfer format timing – slave, CPHA = 0

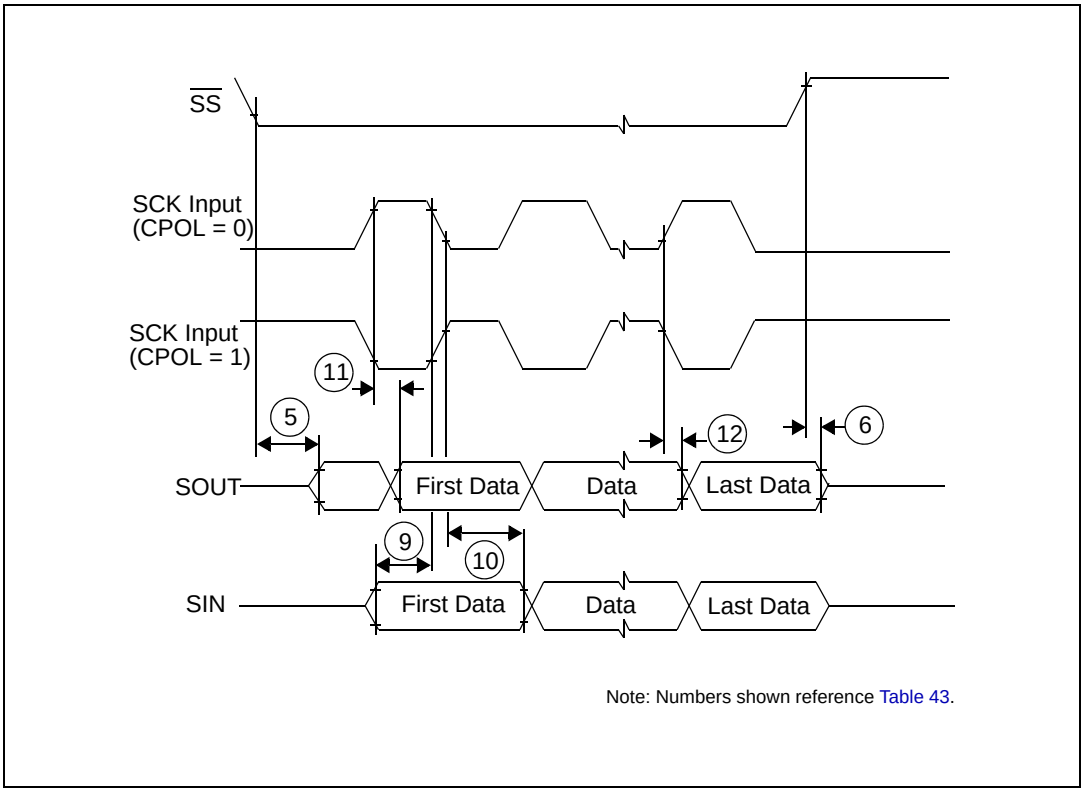

Figure 23. DSPI modified transfer format timing – slave, CPHA = 1

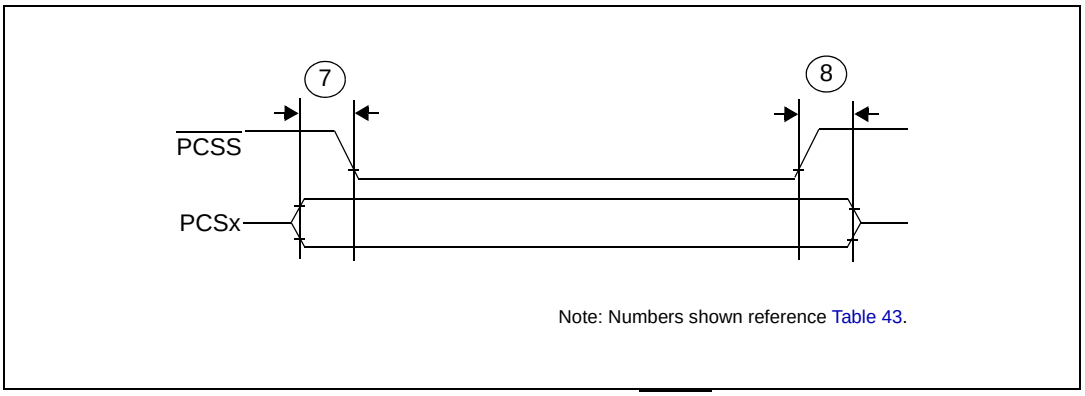

Figure 24. DSPI PCS strobe (PCSS) timing

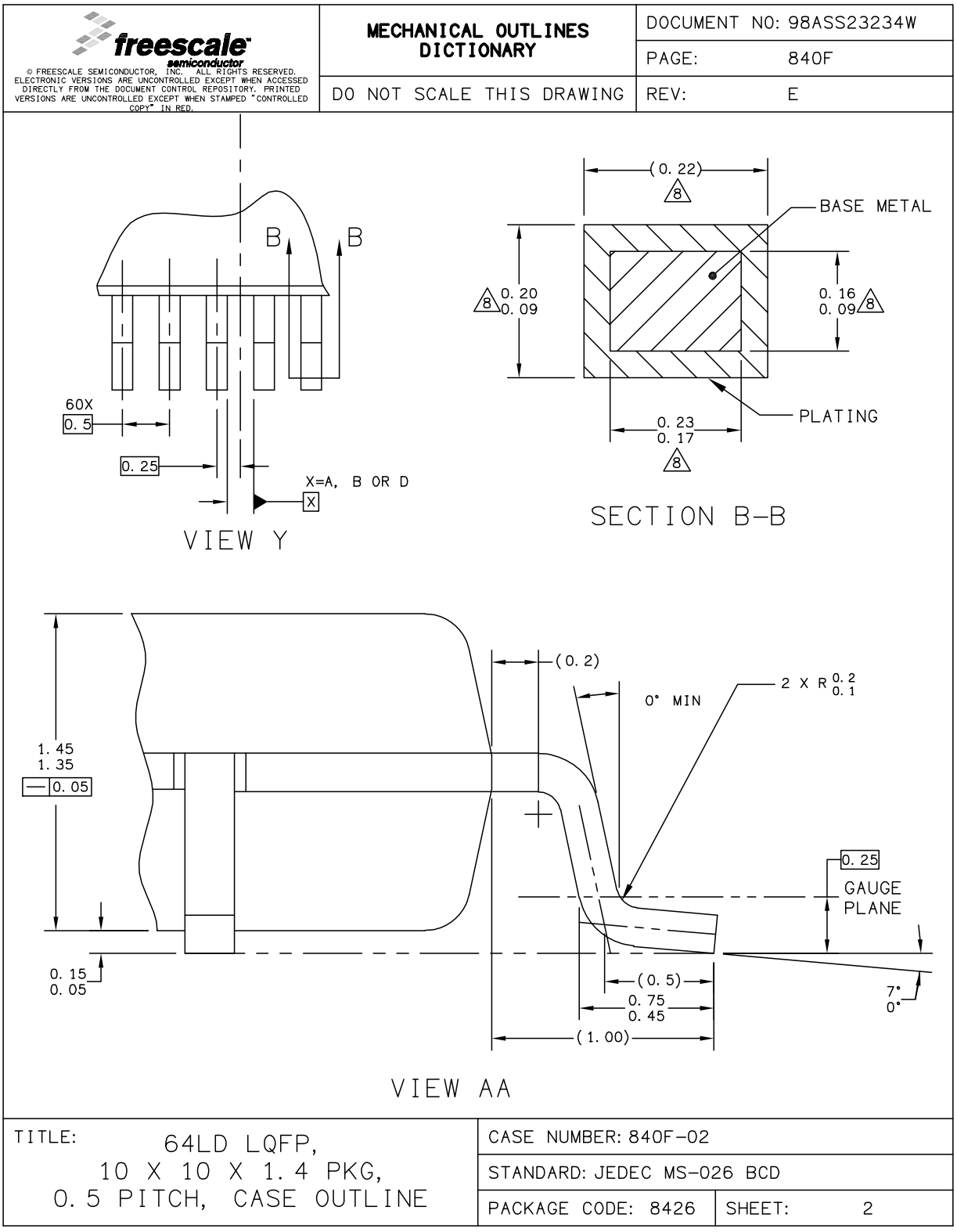

Figure 30. 64 LQFP mechanical drawing (part 2 of 3)

7 Document revision history

Table 45 summarizes revisions to this document.

Table 45. Revision history

Revision	Date	Description of Changes
1	30 Sep 2009	Initial release
2	18 Feb 2010	Updated the following tables: - Absolute maximum ratings - Low voltage power domain electrical characteristics; - On-chip peripherals current consumption - DSPI characteristics; - JTAG characteristics; - ADC conversion characteristics; Inserted a note on “Flash power supply DC characteristics” section.
3	10 Aug 2010	“Features” section: Updated information concerning eMIOS, ADC, LINFlex, Nexus and low power capabilities “MPC5602D device comparison” table: updated the “Execution speed” row “MPC5602D series block diagram” figure: • updated max number of Crossbar Switches • updated Legend “MPC5602D series block summary” table: added contents concernig the eDMA block “100 LQFP pin configuration (top view)” figure: • removed alternate functions • updated supply pins “64 LQFP pin configuration (top view)” figure: removed alternate functions Added “Pin muxing” section “NVUSRO register” section: Deleted “NVUSRO[WATCHDOG_EN] field description“ section “Recommended operating conditions (3.3 V)” table: • TV_{DD}: deleted min value • In footnote No. 3, changed capacitance value between V_{DD_BV} and V_{SS_LV} “Recommended operating conditions (5.0 V)” table: deleted TV_{DD} min value “LQFP thermal characteristics” table: changed $R_{\theta JC}$ values “I/O input DC electrical characteristics” table: • W_{FI}: updated max value • W_{NFI}: updated min value “I/O consumption” table: removed I_{DYNSEG} row Added “I/O weight” table “Program and erase specifications (Code Flash)” table: deleted T_{Bank_C} row Updated the following tables: • “Voltage regulator electrical characteristics” • “Low voltage monitor electrical characteristics” • “Low voltage power domain electrical characteristics” • “Start-up time/Switch-off time” • “Fast external crystal oscillator (4 to 16 MHz) electrical characteristics” • “FMPLL electrical characteristics” • “Fast internal RC oscillator (16 MHz) electrical characteristics” • “ADC conversion characteristics” • “On-chip peripherals current consumption” • “DSPI characteristics” “DSPI characteristics” section: removed “DSPI PCS strobe (PCSS) timing” figure
3 (continued)	10 Aug 2010	“Ordering information” section: removed “Orderable part number summary“ table

Table 45. Revision history (continued)

Revision	Date	Description of Changes
4	14 Jul 2011	Formatting and editorial changes throughout Device comparison table: for the “Total timer I/O eMIOS”, changed “13 ch” to “14 ch” Features: Replaced “e200z0“ with “e200z0h”; added an explanation of which LINFlex modules support master mode and slave MPC5601D/MPC5602D series block summary: • added definition for “AUTOSAR” acronym changed “System watchdog timer” to “Software watchdog timer”64 LQFP pin configuration (top view): changed pin 6 from VPP_TEST to VSS_HV Added section “Pad configuration during reset phases” Added section “Voltage supply pins” Added section “Pad types” Added section “System pins” Renamed and updated section “Functional ports” (was previously section “Pin muxing”); update includes replacing all instances of WKUP with WKPU (WKPU is the correct abbreviation for Wakeup Unit) Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality Added section “NVUSRO[WATCHDOG_EN] field description” Absolute maximum ratings: Removed “C” column from table Replaced “TBD” with “—” in T_{VDD} min value cell of 3.3 V and 5 V recommended operating conditions tables LQFP thermal characteristics: removed $R_{\theta JB}$ single layer board conditions; updated footnote 4 I/O input DC electrical characteristics: removed footnote “All values need to be confirmed during device validation”; updated I_{LKG} characteristics MEDIUM configuration output buffer electrical characteristics: changed “I_{OH} = 100 µA” to “I_{OL} = 100 µA” in V_{OL} conditions I/O consumption: replaced instances of “Root medium square” with “Root mean square” Updated section “Voltage regulator electrical characteristics” Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added a fifth LVD (LVDHV3B); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; deleted note referencing power domain No. 2 (this domain is not present on the device); updated electrical characteristics table Updated and renamed section “Power consumption” (was previously section “Low voltage domain power consumption”) Program and erase specifications (code flash): updated symbols; updated t_{esus} values Updated Flash memory read access timing EMI radiated emission measurement: updated S_{EMI} values Updated FMPLL electrical characteristics Crystal oscillator and resonator connection scheme: inserted footnote about possibly requiring a series resistor Fast internal RC oscillator (16 MHz) electrical characteristics: updated t_{FIRCSU} values Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 13 ADC conversion characteristics: • updated conditions for sampling time V_{DD} = 5.0 V • updated conditions for conversion time V_{DD} = 5.0 V Commercial product code structure: added character for frequency; updated optional fields character and description Restored the revision history table and added an entry for Rev. 3.1 Updated Abbreviations