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### NXP USA Inc. - SPC5602DF1VLL4 Datasheet



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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

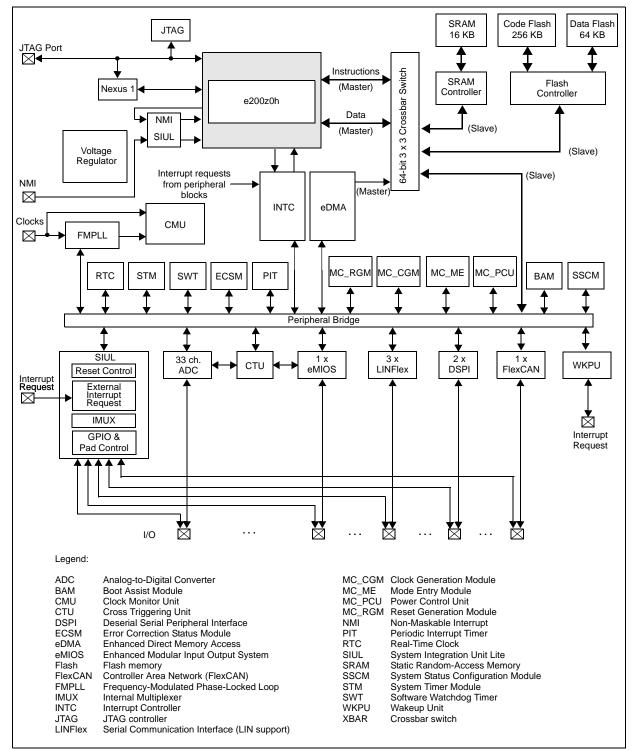
#### Details

Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 16
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5602df1vll4

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### **Block diagram**



### Figure 1. MPC5602D series block diagram

Table 2 summarizes the functions of all blocks present in the MPC5602D series of microcontrollers. Please note that the presence and number of blocks varies by device and package.

Block	Function
Real-time counter (RTC)	Provides a free-running counter and interrupt generation capability that can be used for timekeeping applications
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

Table 2. MPC5602D series block summary (continued)

# **3** Package pinouts and signal descriptions

## 3.1 Package pinouts

The available LQFP pinouts are provided in the following figures. For pin signal descriptions, please refer to Table 5.

### Package pinouts and signal descriptions

							T ation	Pin n	umber
Port pin	PCR	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET configuration	64 LQFP	100 LQFP
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — ADC1_P[3]	SIUL — — ADC	  -   	I	Tristate	37	55
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — ADC1_S[4] WKPU[25] <sup>3</sup>	SIUL — — ADC WKPU	  -     	I	Tristate	30	39
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 —	GPIO[25] — — ADC1_S[5] WKPU[26] <sup>3</sup>	SIUL — — ADC WKPU	     	I	Tristate	29	38
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 —	GPIO[26] — — ADC1_S[6] WKPU[8] <sup>3</sup>	SIUL — — ADC WKPU	I/O — — — — — — —	J	Tristate	31	40
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC1_S[12]	SIUL eMIOS_0  DSPI_0 ADC	I/O I/O I/O I	J	Tristate	38	59
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC1_X[0]	SIUL eMIOS_0  DSPI_0 ADC	I/O I/O — 0 I	J	Tristate	39	61
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC1_X[1]	SIUL eMIOS_0  DSPI_0 ADC	I/O I/O — 0 I	J	Tristate	40	63
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6]  CS3_0 ADC1_X[2]	SIUL eMIOS_0  DSPI_0 ADC	I/O I/O — 0 I	J	Tristate	41	65

 Table 5. Functional port pin descriptions (continued)

### Package pinouts and signal descriptions

							r tion	Pin n	umber
Port pin	PCR	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET configuration	64 LQFP	100 LQFP
PE[9]	PCR[73]	AF0 AF1	GPIO[73]	SIUL	I/O	S	Tristate	—	10
		AF2	E0UC[23]	eMIOS_0	I/O				
		AF3 —	— WKPU[7] <sup>3</sup>		-				
PE[10]	PCR[74]	AF0 AF1	GPIO[74]	SIUL	I/O	S	Tristate		11
		AF2	CS3_1	DSPI_1	0				
		AF3 —	 EIRQ[10]	SIUL	I				
PE[11]	PCR[75]	AF0 AF1 AF2 AF3	GPIO[75] E0UC[24] CS4_1 — WKPU[14] <sup>3</sup>	SIUL eMIOS_0 DSPI_1 — WKPU	I/O I/O O I	S	Tristate		13
PE[12]	PCR[76]	AF0	GPIO[76]	SIUL	I/O	S	Tristate		76
		AF1 AF2 AF3 —	 	— — — ADC	— — — —				
		-	EIRQ[11]	SIUL	I				
				Port	H	_			
PH[9] <sup>6</sup>	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	60	88
PH[10] <sup>6</sup>	PCR[122]	AF0 AF1 AF2 AF3	GPIO[122] — TMS —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	53	81

<sup>1</sup> Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 → AF0; PCR.PA = 01 → AF1; PCR.PA = 10 → AF2; PCR.PA = 11 → AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

<sup>2</sup> Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

<sup>3</sup> All WKPU pins also support external interrupt capability. See "wakeup unit" chapter of the device reference manual for further details.

<sup>4</sup> NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

<sup>5</sup> "Not applicable" because these functions are available only while the device is booting. Refer to "BAM" chapter of the device reference manual for details.

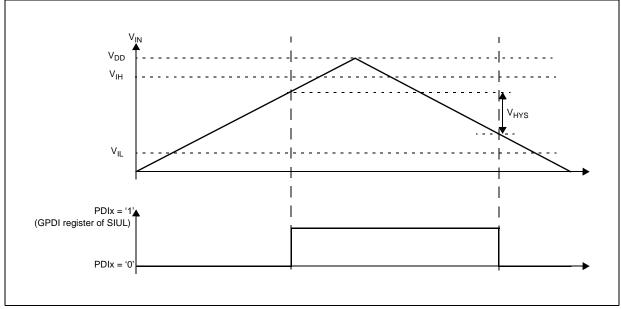


Figure 4. Input DC electrical characteristics definition

Symb		с	Parameter	Condit	tions <sup>1</sup>		Value		Unit	
Symb		C	Falance	Condit		Min	Тур	Max	Unit	
V <sub>IH</sub>	SR	Ρ	Input high level CMOS (Schmitt Trigger)	_		0.65V <sub>DD</sub>	—	V <sub>DD</sub> +0.4	V	
V <sub>IL</sub>	SR	Ρ	Input low level CMOS (Schmitt Trigger)	_	-0.4	_	0.35V <sub>DD</sub>	V		
V <sub>HYS</sub>	СС	С	Input hysteresis CMOS (Schmitt Trigger)	_		0.1V <sub>DD</sub>	_		V	
I <sub>LKG</sub>	СС	D	Digital input leakage	No injection	$T_A = -40 \ ^\circ C$	—	2	200	nA	
		D		on adjacent	pin	T <sub>A</sub> = 25 °C	—	2	200	
		D			T <sub>A</sub> = 85 °C	—	5	300		
		D			T <sub>A</sub> = 105 °C	—	12	500		
		Ρ			T <sub>A</sub> = 125 °C	—	70	1000		
$W_{FI}^2$	SR		Digital input filtered pulse	—		—	—	40	ns	
$W_{NFI}^{(2)}$	SR	Ρ	Digital input not filtered pulse	_	_	1000		—	ns	

 $^{1}$  V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

### 4.7.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

• Table 15 provides weak pull figures. Both pull-up and pull-down resistances are supported.

- Table 16 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 17 provides output driver characteristics for I/O pads when in MEDIUM configuration.

Symt	Symbol		Parameter	Conditions <sup>1</sup>			Value			
- Oyini			r arameter				Тур	Мах	Unit	
I <sub>WPU</sub>	CC	Ρ	Weak pull-up current	$V_{IN} = V_{IL}, V_{DD} = 5.0 \text{ V} \pm 10\%$	PAD3V5V = 0	10	—	150	μA	
		С	absolute value		$PAD3V5V = 1^2$	10	—	250		
		Ρ		$V_{IN} = V_{IL}, V_{DD} = 3.3 \text{ V} \pm 10\%$	PAD3V5V = 1	10	—	150		
$ I_{WPD} $	СС	Ρ	Weak pull-down current	$V_{IN} = V_{IH}, V_{DD} = 5.0 \text{ V} \pm 10\%$	PAD3V5V = 0	10	—	150	μA	
		С	absolute value		$PAD3V5V = 1^{(2)}$	10	—	250		
		Ρ		$V_{IN} = V_{IH}, V_{DD} = 3.3 \text{ V} \pm 10\%$	PAD3V5V = 1	10	—	150		

### Table 15. I/O pull-up/pull-down DC electrical characteristics

 $^1~V_{DD}$  = 3.3 V  $\pm$  10% / 5.0 V  $\pm$  10%,  $T_A$  = –40 to 125 °C, unless otherwise specified.

<sup>2</sup> The configuration PAD3V5 = 1 when  $V_{DD}$  = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

### Table 16. SLOW configuration output buffer electrical characteristics

Sym	bol	0	Parameter		Conditions <sup>1</sup>	V	alue		Unit
Joyni	001	U	i arameter		Conditions	Min	Тур	Max	Onic
V <sub>OH</sub>	CC	Ρ	Output high level SLOW configuration	Push Pull	$I_{OH} = -2 \text{ mA},$ $V_{DD} = 5.0 \text{ V} \pm 10\%, \text{ PAD3V5V} = 0$ (recommended)	0.8V <sub>DD</sub>		_	V
		С			I <sub>OH</sub> = -2 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 1 <sup>2</sup>	0.8V <sub>DD</sub>	_	_	
		С			I <sub>OH</sub> = −1 mA, V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V <sub>DD</sub> – 0.8		_	
V <sub>OL</sub>	СС	Ρ	Output low level SLOW configuration	Push Pull	$I_{OL} = 2 \text{ mA},$ $V_{DD} = 5.0 \text{ V} \pm 10\%, \text{ PAD3V5V} = 0$ (recommended)	_		0.1V <sub>DD</sub>	V
		С			$I_{OL} = 2 \text{ mA},$ $V_{DD} = 5.0 \text{ V} \pm 10\%, \text{ PAD3V5V} = 1^{(2)}$	_		0.1V <sub>DD</sub>	
		С			$I_{OL} = 1 \text{ mA},$ $V_{DD} = 3.3 \text{ V} \pm 10\%, \text{ PAD3V5V} = 1$ (recommended)	—	_	0.5	

 $\overline{}^{1}$  V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> The configuration PAD3V5 = 1 when V<sub>DD</sub> = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Symbol		с	Parameter	Condi	tions <sup>1</sup>		Value		Unit
Symbol		C	Farameter	Condi	Conditions			Max	Unit
I <sub>SWTSLW</sub> ,2	СС	D	for SLOW	C <sub>L</sub> = 25 pF	$V_{DD} = 5.0 V \pm 10\%,$ PAD3V5V = 0	_		20	mA
			configuration		V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1		—	16	
I <sub>SWTMED</sub> <sup>(2)</sup>	СС	D	for MEDIUM	C <sub>L</sub> = 25 pF	$V_{DD} = 5.0 V \pm 10\%,$ PAD3V5V = 0	_		29	mA
			configuration		V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1			17	
I <sub>RMSSLW</sub>		Root mean square	C <sub>L</sub> = 25 pF, 2 MHz	$V_{DD} = 5.0 V \pm 10\%,$		—	2.3	mA	
			I/O current for SLOW configuration	C <sub>L</sub> = 25 pF, 4 MHz		—	—	3.2	
			<b>3</b>	C <sub>L</sub> = 100 pF, 2 MHz		-	—	6.6	
				C <sub>L</sub> = 25 pF, 2 MHz	$V_{DD} = 3.3 V \pm 10\%,$	_	—	1.6	
				C <sub>L</sub> = 25 pF, 4 MHz	PAD3V5V = 1	—	—	2.3	
				C <sub>L</sub> = 100 pF, 2 MHz			—	4.7	
IRMSMED	СС	D	Root mean square	C <sub>L</sub> = 25 pF, 13 MHz	$V_{DD} = 5.0 V \pm 10\%,$	_	—	6.6	mA
			I/O current for MEDIUM	C <sub>L</sub> = 25 pF, 40 MHz	PAD3V5V = 0	—	—	13.4	
			configuration	C <sub>L</sub> = 100 pF, 13 MHz		-	—	18.3	
				C <sub>L</sub> = 25 pF, 13 MHz	$V_{DD} = 3.3 V \pm 10\%,$		—	5	
				C <sub>L</sub> = 25 pF, 40 MHz	PAD3V5V = 1	—	—	8.5	
				C <sub>L</sub> = 100 pF, 13 MHz	1	—	—	11	
I <sub>AVGSEG</sub>	SR	D	Sum of all the static	V <sub>DD</sub> = 5.0 V ± 10%, P	AD3V5V = 0	—	—	70	mA
			I/O current within a supply segment	V <sub>DD</sub> = 3.3 V ± 10%, P	AD3V5V = 1		—	65	

### Table 20. I/O consumption

 $^{1}$  V\_{DD} = 3.3 V  $\pm$  10% / 5.0 V  $\pm$  10%, T\_A = -40 to 125 °C, unless otherwise specified

<sup>2</sup> Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 21 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below 100%.

		100 LQFF	P/64 LQFP	
Pad	Weigl	ht 5 V	Weigh	t 3.3 V
	SRC <sup>2</sup> = 0	SRC = 1	SRC = 0	SRC = 1
PC[0]	6%	9%	7%	8%
PE[2]	7%	10%	8%	9%
PE[3]	7%	10%	9%	9%
PC[5]	8%	11%	9%	10%
PC[4]	8%	11%	9%	10%
PE[4]	8%	12%	10%	10%
PE[5]	8%	12%	10%	11%
PE[6]	9%	12%	10%	11%
PE[7]	9%	12%	10%	11%
PC[12]	9%	13%	11%	11%
PC[13]	9%	9%	11%	11%
PC[8]	9%	9%	11%	11%
PB[2]	9%	13%	11%	12%

### Table 21. I/O weight<sup>1</sup> (continued)

<sup>1</sup>  $V_{DD} = 3.3 \text{ V} \pm 10\% \text{ / } 5.0 \text{ V} \pm 10\%, \text{ T}_{A} = -40 \text{ to } 125 \text{ °C}, \text{ unless otherwise specified}$ <sup>2</sup> SRC: "Slew Rate Control" bit in SIU\_PCR

#### **RESET** electrical characteristics 4.8

The device implements a dedicated bidirectional RESET pin.

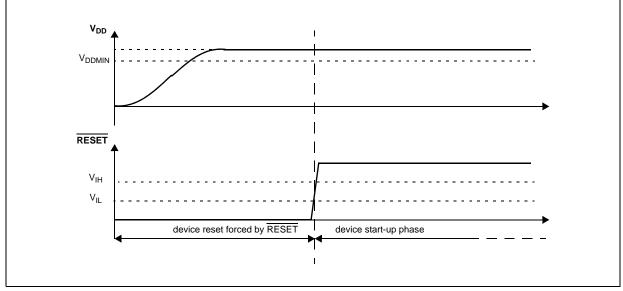


Figure 5. Start-up reset requirements

Symbol		с	Parameter	Conditions <sup>1</sup>		Value			Unit
Gymb		Ŭ	i didineter	Conditions		Min	Тур	Max	
I <sub>FLPW</sub>	СС		Sum of the current consumption on $V_{DDHV}$ and $V_{DDBV}$ during flash low-power mode	_	Code flash		—	910	μA
I <sub>CFPWD</sub>	СС		Sum of the current consumption on	—	Code flash		—	125	μA
I <sub>DFPWD</sub>	СС	D	V <sub>DDHV</sub> and V <sub>DDBV</sub> during flash power-down mode		Data flash		—	25	μA

Table 30. Flash power supply DC electrical characteristics

 $^1~$  V\_{DD} = 3.3 V  $\pm$  10% / 5.0 V  $\pm$  10%, T\_A = -40 to 125 °C, unless otherwise specified

## 4.11.3 Start-up/Switch-off timings

Table 31. Start-up	time/Switch-off	time
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Symbol		с	Parameter	Conditions <sup>1</sup>	Value			Unit
Cymbol		Ŭ	i didineter	Conditions	Min	Тур	Мах	
t <sub>FLARSTEXIT</sub>	CC	Т	Delay for flash module to exit reset mode	Code flash	—	—	125	μs
				Data flash			150	μs
t <sub>FLALPEXIT</sub>	СС	Т	Delay for flash module to exit low-power mode <sup>2</sup>	Code flash	—	—	0.5	μs
t <sub>FLAPDEXIT</sub>	СС	Т	Delay for flash module to exit power-down	Code flash		_	30	μs
			mode	Data flash		—	30 <sup>3</sup>	μs
t <sub>FLALPENTRY</sub>	CC	Т	Delay for flash module to enter low-power mode	Code flash	—	—	0.5	μs
t <sub>FLAPDENTRY</sub>	СС	Т	Delay for flash module to enter	Code flash		—	1.5	μs
			power-down mode	Data flash	—	—	4 <sup>(3)</sup>	μs

 $\overline{1}$  V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> Data flash does not support low-power mode

<sup>3</sup> If code flash is already switched-on.

# 4.12 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

### 4.12.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

• Software recommendations – The software flowchart must include the management of runaway conditions such as:

Symbol		Deremeter	Conditional		Value		Unit
	C	Parameter	Conditions	Min	Тур	Max	Unit
SR		Fast external crystal — oscillator frequency		4.0	_	16.0	MHz
g <sub>mFXOSC</sub> CC         C         Fast external crystal oscillator transconductance			$V_{DD} = 3.3 V \pm 10\%$ , PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	_	8.2	mA/V
СС	Ρ		$V_{DD} = 5.0 V \pm 10\%$ , PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	_	7.4	
СС	С		$V_{DD} = 3.3 V \pm 10\%$ , PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	_	9.7	
СС	С		$V_{DD} = 5.0 V \pm 10\%$ , PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	_	9.2	
СС	Т	Oscillation amplitude at EXTAL	f <sub>OSC</sub> = 4 MHz, OSCILLATOR_MARGIN = 0	1.3		—	V
			f <sub>OSC</sub> = 16 MHz, OSCILLATOR_MARGIN = 1	1.3		—	
CC	Ρ	Oscillation operating point	—	_	0.95		V
СС	Т	Fast external crystal oscillator consumption	_	—	2	3	mA
СС	Т	Fast external crystal oscillator start-up time	f <sub>OSC</sub> = 4 MHz, OSCILLATOR_MARGIN = 0	—	_	6	ms
			f <sub>OSC</sub> = 16 MHz, OSCILLATOR_MARGIN = 1	—	_	1.8	
SR	Ρ	Input high level CMOS (Schmitt Trigger)			_	V <sub>DD</sub> +0.4	V
SR	Ρ	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	-0.4	_	0.35V <sub>DD</sub>	V
	SR CC CC CC CC CC CC CC SR	SR — CC C CC P CC C CC C CC T CC T CC T CC T	SR—Fast external crystal oscillator frequencyCCCFast external crystal oscillator transconductanceCCPCCCCCCCCCCCCCCTOscillation amplitude at EXTALCCPOscillation operating pointCCTFast external crystal oscillator consumptionCCTFast external crystal oscillator start-up timeSRPInput high level CMOS (Schmitt Trigger)SRPInput low level CMOS	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	CParameterConditions1SR-Fast external crystal oscillator frequency-4.0-CCCFast external crystal oscillator transconductanceVDD = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 02.2-CCPVDD = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 02.0-CCCVDD = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 02.0-CCCVDD = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 12.7-CCCVDD = 5.0 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 12.5-CCTOscillation amplitude at EXTALfosc = 4 MHz, OSCILLATOR_MARGIN = 01.3-CCTOscillation operating point0.95CCTFast external crystal oscillator consumption2CCTFast external crystal oscillator start-up timefosc = 4 MHz, OSCILLATOR_MARGIN = 0CCTFast external crystal oscillator start-up time2SRPInput high level CMOS (Schmitt Trigger)Oscillator bypass mode0.65VDD DSRPInput low level CMOS (Schmitt Trigger)Oscillator bypass mode-0.4	CParameterConditions1MinTypMaxSR-Fast external crystal oscillator frequency4.016.0CCCFast external crystal oscillator transconductanceVDD = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 02.28.2CCP $V_{DD} = 5.0 V \pm 10\%,$ PAD3V5V = 0 OSCILLATOR_MARGIN = 02.07.4CCCVDD = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 12.79.7CCCVDD = 5.0 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 12.59.2CCTOscillation amplitude at EXTAL $f_{OSC} = 4$ MHz, OSCILLATOR_MARGIN = 11.3CCPOscillation operating point0.95CCTFast external crystal 

 $^{1}$  V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals)

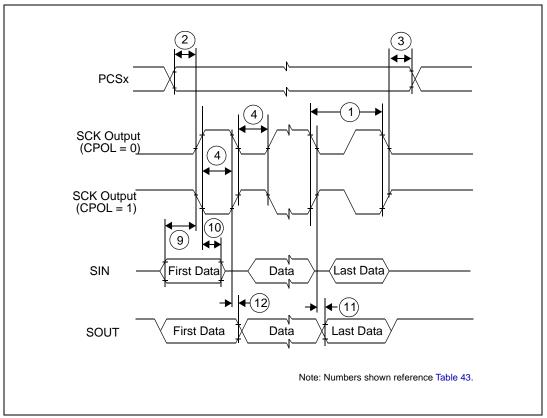


Figure 16. DSPI classic SPI timing – master, CPHA = 0

# 4.18.3 JTAG characteristics

No	No. Symbol		Symbol C	Parameter		Unit		
NO.			C	Farameter	Min	Тур	Мах	onit
1	t <sub>JCYC</sub>	CC	D	TCK cycle time	83.33	_	_	ns
2	t <sub>TDIS</sub>	CC	D	TDI setup time	15	_	—	ns
3	t <sub>TDIH</sub>	CC	D	TDI hold time	5		—	ns
4	t <sub>TMSS</sub>	CC	D	TMS setup time	15	_	_	ns
5	t <sub>TMSH</sub>	CC	D	TMS hold time	5	_	—	ns
6	t <sub>TDOV</sub>	CC	D	TCK low to TDO valid	_	_	49	ns
7	t <sub>TDOI</sub>	CC	D	TCK low to TDO invalid	6	_	—	ns

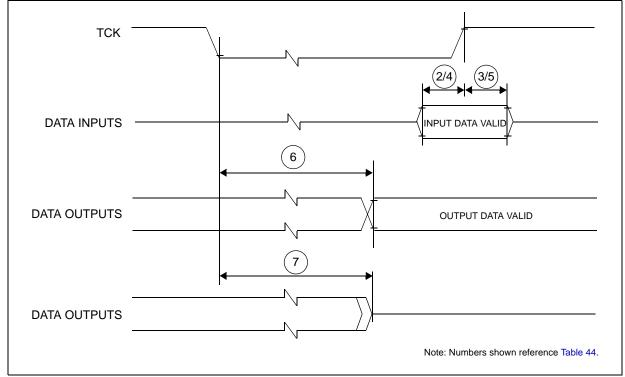


Figure 25. Timing diagram – JTAG boundary scan

# **5** Package characteristics

- 5.1 Package mechanical data
- 5.1.1 100 LQFP

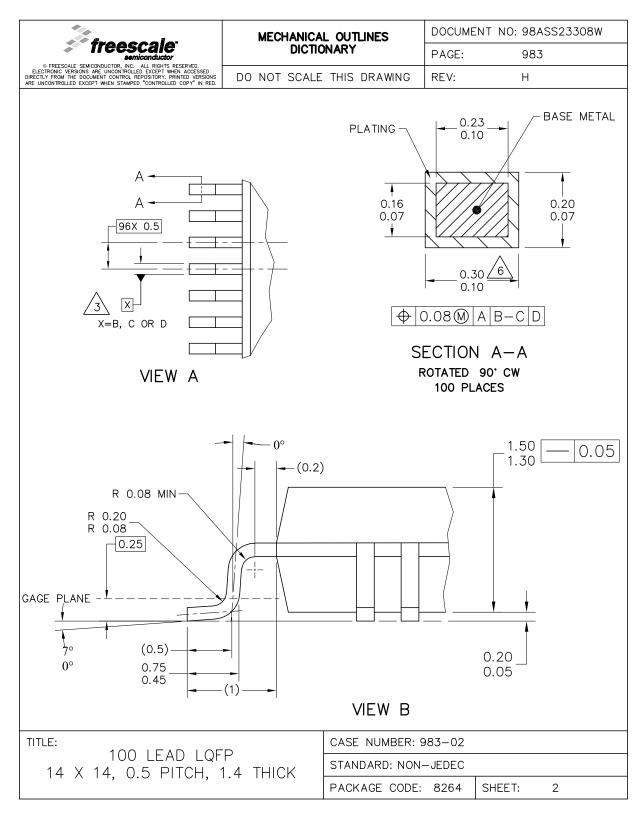


Figure 27. 100 LQFP package mechanical drawing (Part 2 of 3)

### 5.1.2 64 LQFP

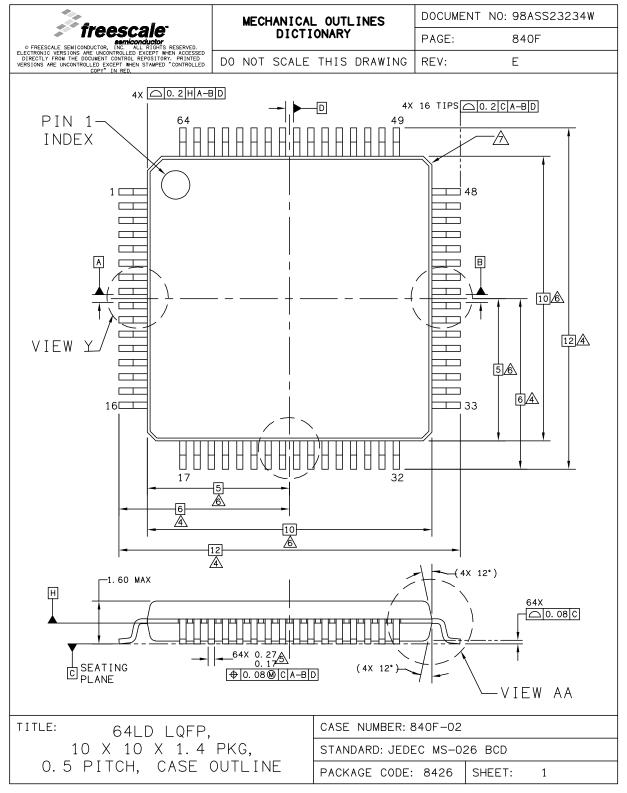


Figure 29. 64 LQFP mechanical drawing (part 1 of 3)

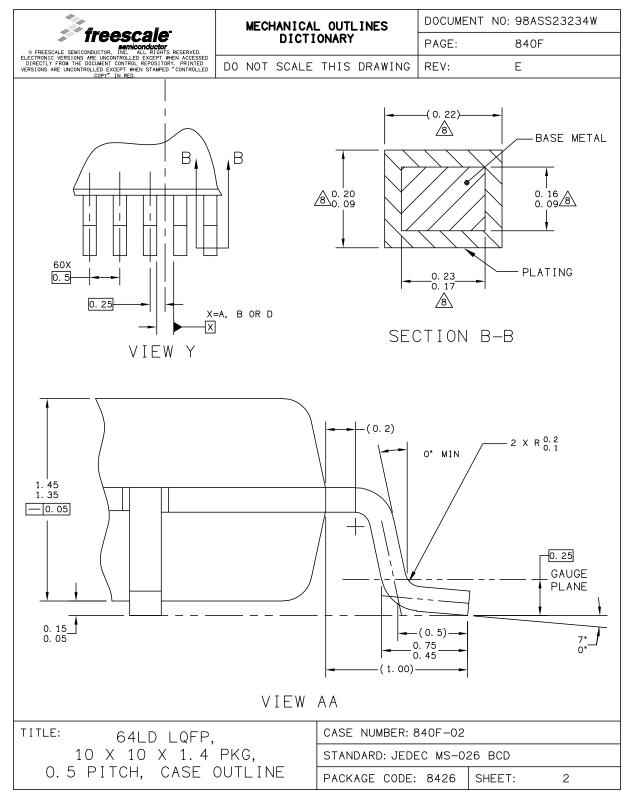


Figure 30. 64 LQFP mechanical drawing (part 2 of 3)

	*	MECHANICAL OUTLINES DICTIONARY		DOCUMENT NO: 98ASS23234W					
© EREESCALE				PAGE:	840F				
ELECTRONIC VE DIRECTLY FRO VERSIONS ARE	5 SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. RSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED ON THE DOCUMENT CONTROL REPOSITORY, PRINTED UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.	DO NOT SCALE	THIS DRAWING	REV:	E				
NO	NOTES:								
1.	1. DIMENSIONS ARE IN MILLIMETERS.								
2.	DIMENSIONING AND TOL	ERANCING PER	ASME Y14.5M-19	994.					
3.	DATUMS A, B AND D TO	BE DETERMINE	D AT DATUM PLA	NE H.					
4	DIMENSIONS TO BE DET	ERMINED AT SE	ATING PLANE C.						
	THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.								
	THIS DIMENSION DOES IS 0.25 mm PER SIDE. DIMENSION INCLUDING	THIS DIMENSI	ON IS MAXIMUM						
$\triangle$	EXACT SHAPE OF EACH	CORNER IS OPT	IONAL.						
<u> </u>	${\&}$ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.								
TITLE:	64LD LQFP, 10 X 10 X 1.4	PKG,	CASE NUMBER: 8 STANDARD: JEDE		BCD				
0.	5 PITCH, CASE (	DUTLINE	PACKAGE CODE:	8426 SH	HEET: 3				

### Figure 31. 64 LQFP mechanical drawing (part 3 of 3)

# 6 Ordering information

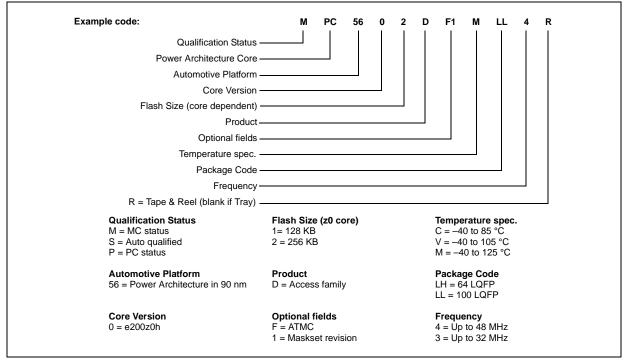


Figure 32. Commercial product code structure

Document revision history

# 7 Document revision history

Table 45 summarizes revisions to this document.

### Table 45. Revision history

Revision	Date	Description of Changes
1	30 Sep 2009	Initial release
2	18 Feb 2010	Updated the following tables: - Absolute maximum ratings - Low voltage power domain electrical characteristics; - On-chip peripherals current consumption - DSPI characteristics; - JTAG characteristics; - ADC conversion characteristics; Inserted a note on "Flash power supply DC characteristics" section.
3	10 Aug 2010	<ul> <li>"Features" section: Updated information concerning eMIOS, ADC, LINFlex, Nexus and low power capabilities</li> <li>"MPC5602D device comparison" table: updated the "Execution speed" row</li> <li>"MPC5602D series block diagram" figure:</li> <li>updated max number of Crossbar Switches</li> <li>updated Legend</li> <li>"MPC5602D series block summary" table: added contents concernig the eDMA block</li> <li>"100 LQFP pin configuration (top view)" figure:</li> <li>removed alternate functions</li> <li>updated supply pins</li> <li>"64 LQFP pin configuration (top view)" figure: removed alternate functions</li> <li>Added "Pin muning" section</li> <li>"NVUSRO register" section: Deleted "NVUSRO[WATCHDOG_EN] field description" section</li> <li>"Recommended operating conditions (3.3 V)" table:</li> <li>TV<sub>DD</sub>: deleted min value</li> <li>In footnote No. 3, changed capacitance value between V<sub>DD_BV</sub> and V<sub>SS_LV</sub></li> <li>"Recommended operating conditions (5.0 V)" table: deleted TV<sub>DD</sub> min value</li> <li>"LQFP thermal characteristics" table: changed R<sub>0JC</sub> values</li> <li>"I/O input DC electrical characteristics" table:</li> <li>W<sub>FI</sub>: updated min value</li> <li>"Vo consumption" table: removed I<sub>DYNSEG</sub> row</li> <li>Added "I/O weight" table</li> <li>"Program and erase specifications (Code Flash)" table: deleted T<sub>Bank_C</sub> row</li> <li>Updated the following tables:</li> <li>"Voltage regulator electrical characteristics"</li> <li>"Low voltage power domain electrical characteristics"</li> <li>"Low voltage power domain electrical characteristics"</li> <li>"Fast external crystal oscillator (16 MHz) electrical characteristics"</li> <li>"Fast internal RC oscillator (16 MHz) electrical characteristics"</li> <li>"ADC conversion characteristics"</li> <li>"ADC conversion characteristics"</li> <li>"DSPI characteristics" section: removed "DSPI PCS strobe (PCSS) timing" figure</li> </ul>
3 (continued)	10 Aug 2010	"Ordering information" section: removed "Orderable part number summary" table

### Abbreviations

Abbreviation	Meaning	
OPWMCB	Center aligned output pulse width modulation buffered with dead time	
OPWMT	Output pulse width modulation trigger	
PWM	Pulse width modulation	
SAIC	Single action input capture	
SAOC	Single action output compare	
SCK	Serial communications clock	
SOUT	Serial data out	
TBD	To be defined	
ТСК	Test clock input	
TDI	Test data input	
TDO	Test data output	
TMS	Test mode select	

### Table A-1. Abbreviations (continued)

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