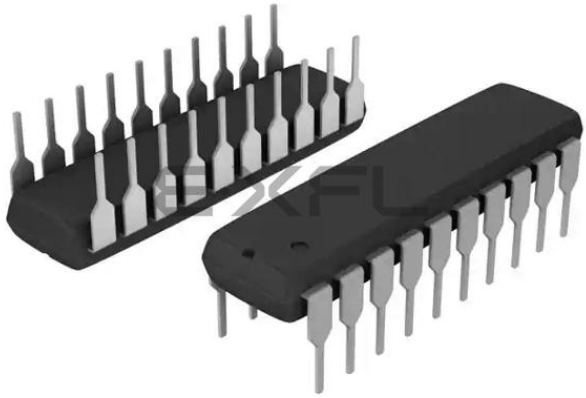

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

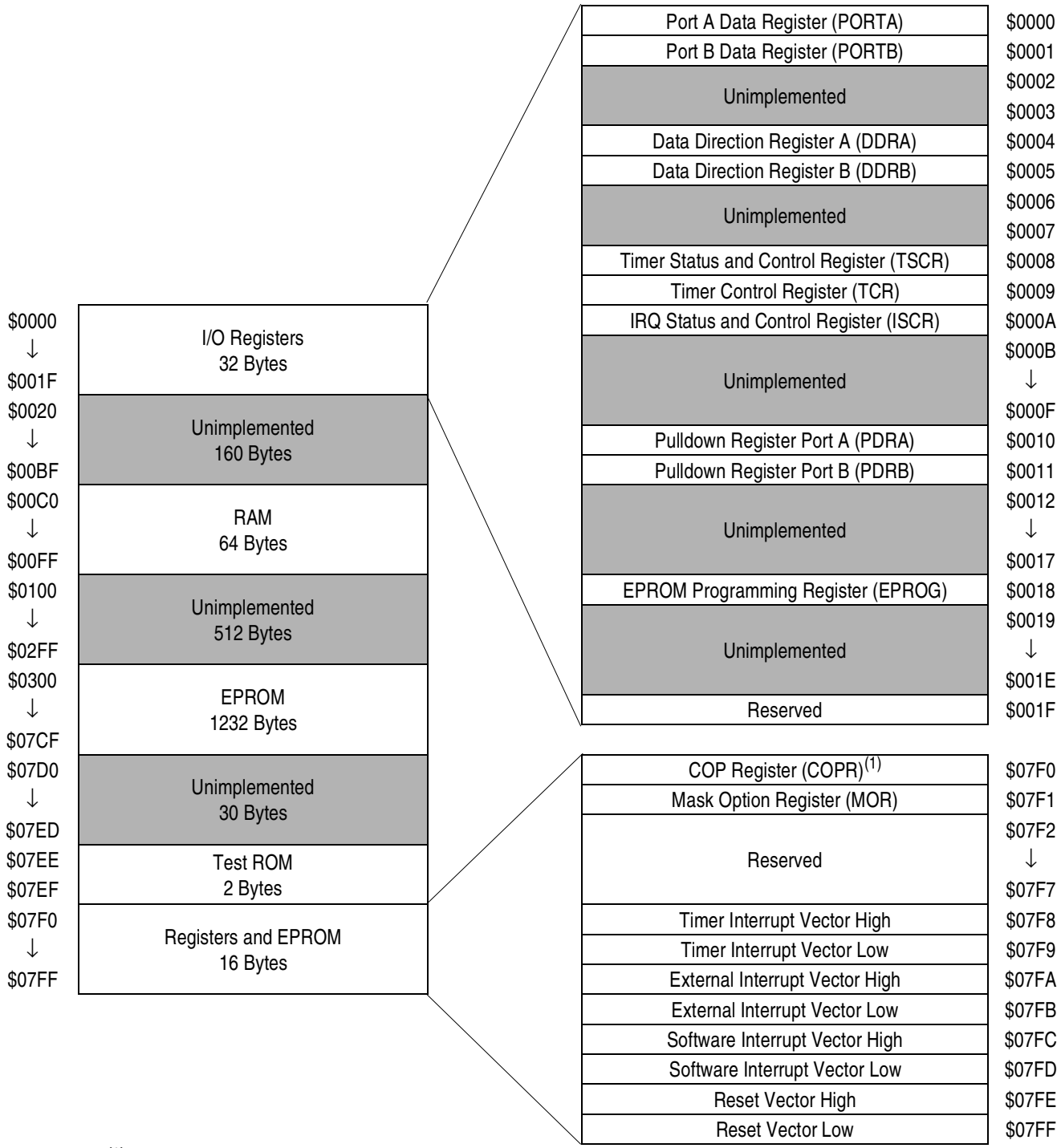
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705j1acp

Section 1. General Description

1.1 Contents

2.3 Memory Map



(1) Writing to bit 0 of $07F0 clears the computer operating properly (COP) watchdog.

Figure 2-1. Memory Map

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0019	Unimplemented									
↓										
$001E	Unimplemented									
$001F	Reserved		R	R	R	R	R	R	R	R
$07F0	COP Register (COPR) See page 99.	Read:								
		Write:								COPC
		Reset:								0
$07F1	Mask Option Register (MOR) See page 41.	Read:	SOSCD	EPMSEC	OSCRES	SWAIT	SWPDI	PIRQ	LEVEL	COPEN
		Write:								
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved

Figure 2-2. I/O Register Summary (Sheet 3 of 3)

2.5 RAM

The 64 addresses from $00C0 to $00FF serve as both the user RAM and the stack RAM. Before processing an interrupt, the central processor unit (CPU) uses five bytes of the stack to save the contents of the CPU registers. During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements when the CPU stores a byte on the stack and increments when the CPU retrieves a byte from the stack.

NOTE: *Be careful when using nested subroutines or multiple interrupt levels. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.*

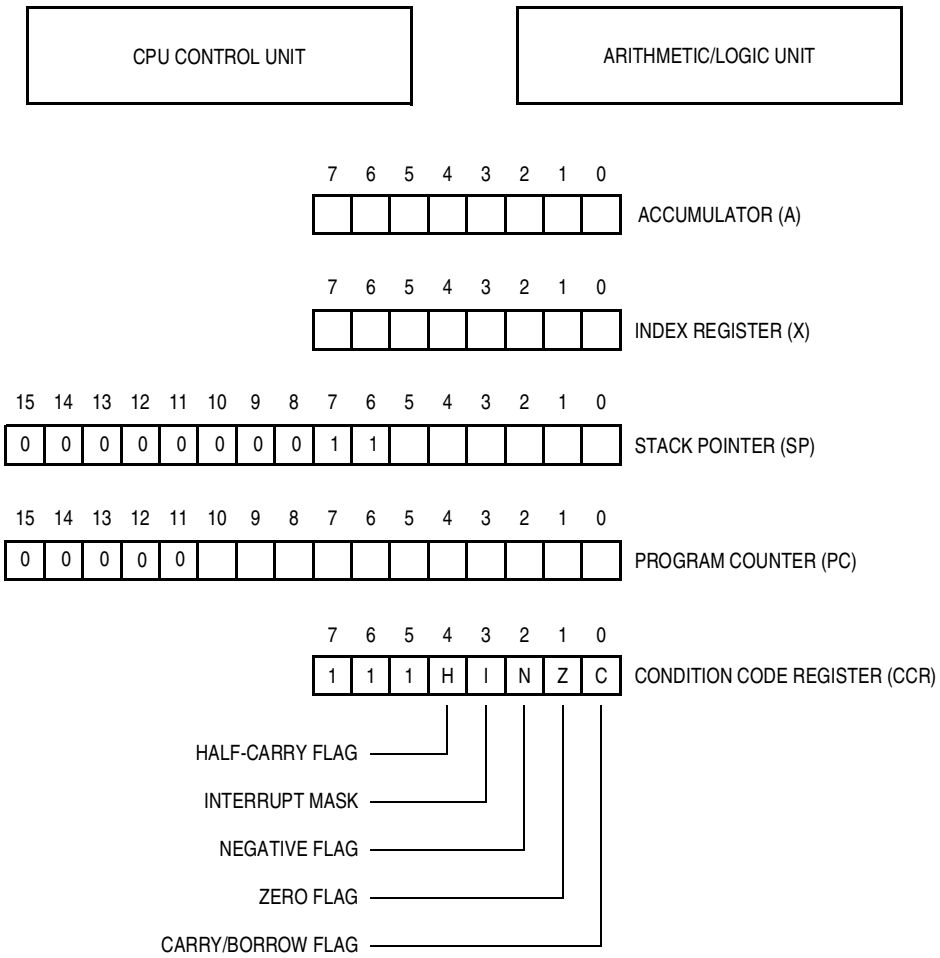


Figure 3-1. Programming Model

3.6.2 Instruction Types

The MCU instructions fall into these five categories:

- Register/memory instructions
- Read-modify-write instructions
- Jump/branch instructions
- Bit manipulation instructions
- Control instructions

3.6.2.1 Register/Memory Instructions

These instructions operate on CPU registers and memory locations. Most of them use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory.

Table 3-1. Register/Memory Instructions

Instruction	Mnemonic
Add memory byte and carry bit to accumulator	ADC
Add memory byte to accumulator	ADD
AND memory byte with accumulator	AND
Bit test accumulator	BIT
Compare accumulator	CMP
Compare index register with memory byte	CPX
EXCLUSIVE OR accumulator with memory byte	EOR
Load accumulator with memory byte	LDA
Load index register with memory byte	LDX
Multiply	MUL
OR accumulator with memory byte	ORA
Subtract memory byte and carry bit from accumulator	SBC
Store accumulator in memory	STA
Store index register in memory	STX
Subtract memory byte from accumulator	SUB

Table 3-3. Jump and Branch Instructions

Instruction	Mnemonic
Branch if carry bit clear	BCC
Branch if carry bit set	BCS
Branch if equal	BEQ
Branch if half-carry bit clear	BHCC
Branch if half-carry bit set	BHCS
Branch if higher	BHI
Branch if higher or same	BHS
Branch if $\overline{\text{IRQ}}$ pin high	BIH
Branch if $\overline{\text{IRQ}}$ pin low	BIL
Branch if lower	BLO
Branch if lower or same	BLS
Branch if interrupt mask clear	BMC
Branch if minus	BMI
Branch if interrupt mask set	BMS
Branch if not equal	BNE
Branch if plus	BPL
Branch always	BRA
Branch if bit clear	BRCLR
Branch never	BRN
Branch if bit set	BRSET
Branch to subroutine	BSR
Unconditional jump	JMP
Jump to subroutine	JSR

Table 3-6. Instruction Set Summary (Sheet 2 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3
BHS *rel*	Branch if Higher or Same	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BIH *rel*	Branch if IRQ Pin High	PC ← (PC) + 2 + *rel* ? IRQ = 1	—	—	—	—	—	REL	2F	rr	3
BIL *rel*	Branch if IRQ Pin Low	PC ← (PC) + 2 + *rel* ? IRQ = 0	—	—	—	—	—	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X	Bit Test Accumulator with Memory Byte	(A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff	2 3 4 5 4 3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? C ∨ Z = 1	—	—	—	—	—	REL	23	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? I = 0	—	—	—	—	—	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? N = 1	—	—	—	—	—	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? I = 1	—	—	—	—	—	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? Z = 0	—	—	—	—	—	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? N = 0	—	—	—	—	—	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel* ? 1 = 1	—	—	—	—	—	REL	20	rr	3
BRCLR *n opr rel*	Branch if Bit n Clear	PC ← (PC) + 2 + *rel* ? Mn = 0	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2 + *rel* ? 1 = 0	—	—	—	—	—	REL	21	rr	3
BRSET *n opr rel*	Branch if Bit n Set	PC ← (PC) + 2 + *rel* ? Mn = 1	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n opr*	Set Bit n	Mn ← 1	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5

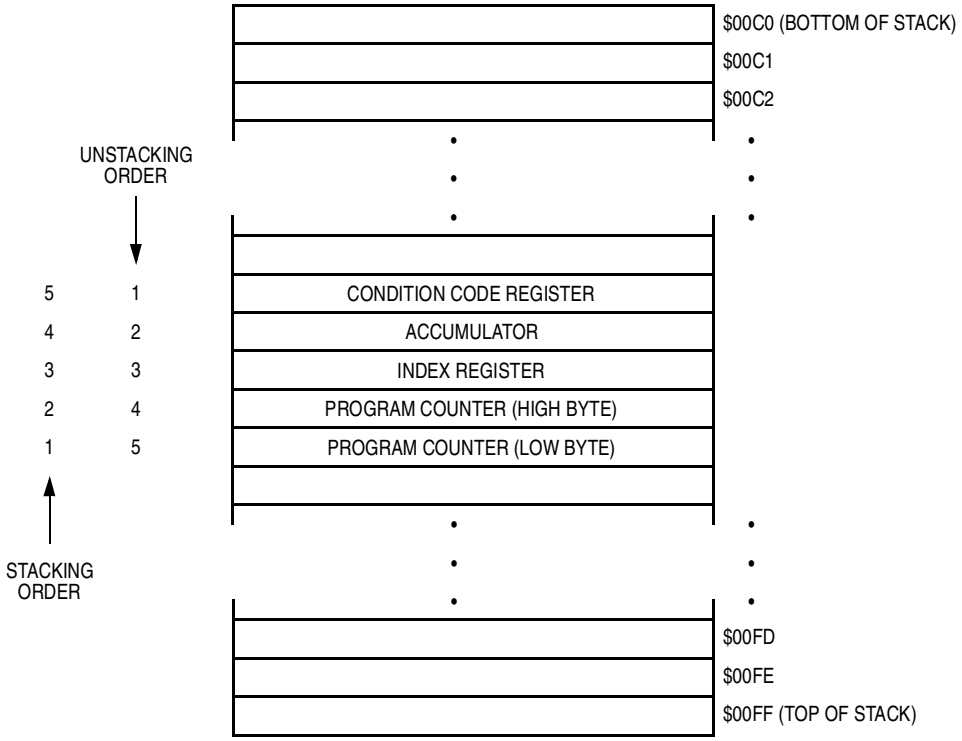


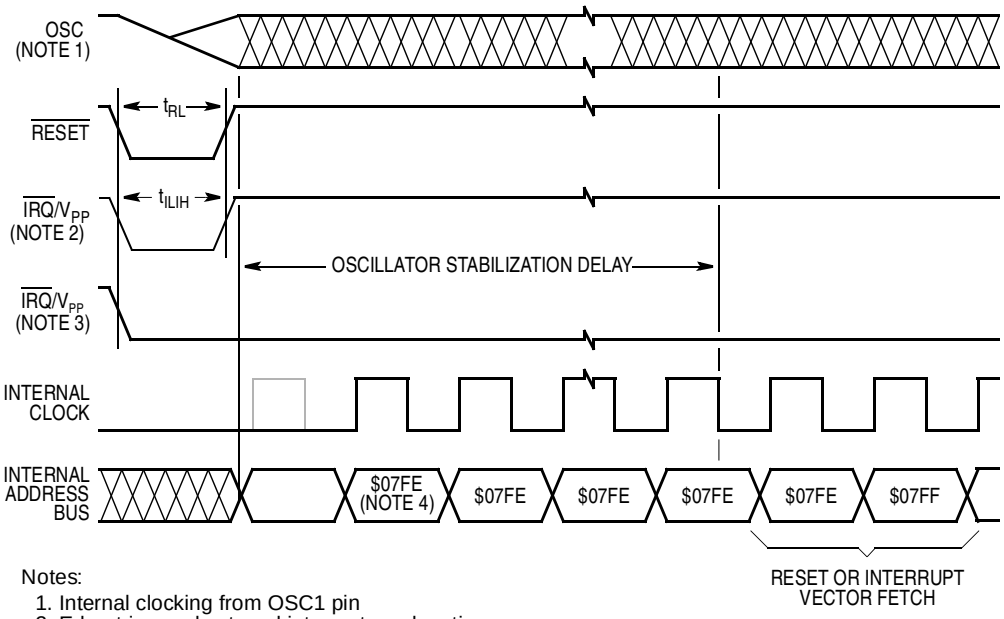
Figure 4-6. Interrupt Stacking Order

Table 4-4. Reset/Interrupt Vector Addresses

Function	Source	Local Mask	Global Mask	Priority (1 = Highest)	Vector Address
Reset	$\overline{\text{Power-on}}$ $\overline{\text{RESET}}$ pin COP watchdog[1] illegal address	None	None	1	$07FE–$07FF
Software interrupt (SWI)	User code	None	None	Same priority as instruction	$07FC–$07FD
External interrupt	$\overline{\text{IRQ}}/V_{PP}$ pin	IRQE	I bit	2	$07FA–$07FB
Timer interrupts	RTIF bit TOF bit	RTIE bit TOIE bit	I bit	3	$07F8–$07F9

1. The COP watchdog is programmable in the mask option register.

5.5 Timing



Notes:
1. Internal clocking from OSC1 pin
2. Edge-triggered external interrupt mask option
3. Edge- and level-triggered external interrupt mask option
4. Reset vector shown as example

Figure 5-1. Stop Mode Recovery Timing

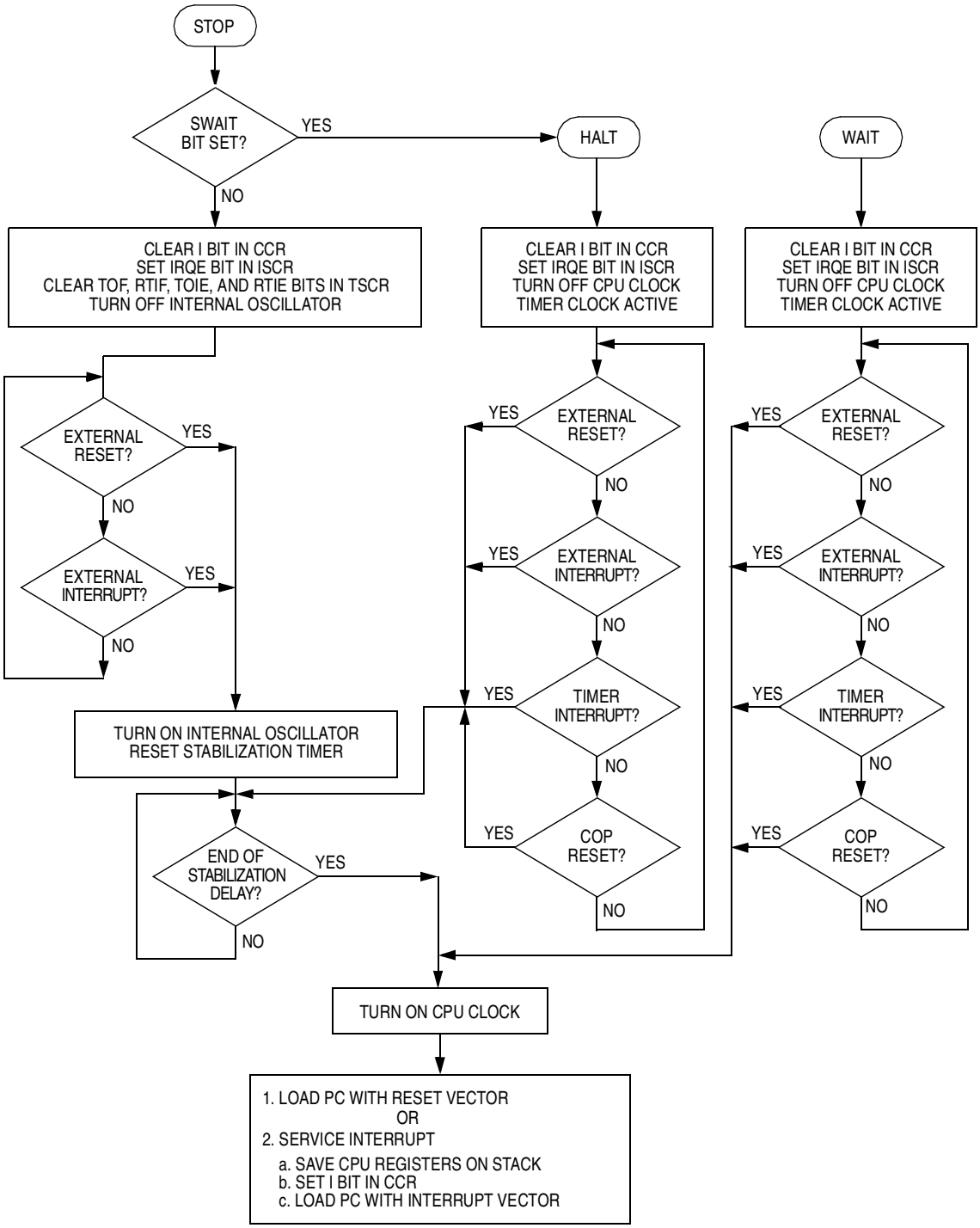


Figure 5-2. Stop/Halt/Wait Flowchart

7.3 Operation

Operation of the COP is described in this subsection.

7.3.1 COP Watchdog Timeout

Four counter stages at the end of the timer make up the COP watchdog. The COP resets the MCU if the timeout period occurs before the COP watchdog timer is cleared by application software and the $\overline{IRQ}/V_{PP}$ pin voltage is between V_{SS} and V_{DD}. Periodically clearing the counter starts a new timeout period and prevents COP reset. A COP watchdog timeout indicates that the software is not executing instructions in the correct sequence.

NOTE: *The internal clock drives the COP watchdog. Therefore, the COP watchdog cannot generate a reset for errors that cause the internal clock to stop.*

The COP watchdog depends on a power supply voltage at or above a minimum specification and is not guaranteed to protect against brownout.

7.3.2 COP Watchdog Timeout Period

The COP watchdog timer function is implemented by dividing the output of the real-time interrupt circuit (RTI) by eight. The RTI select bits in the timer status and control register control RTI output, and the selected output drives the COP watchdog. See timer status and control register in **Section 9. Multifunction Timer Module**.

NOTE: *The minimum COP timeout period is seven times the RTI period. The COP is cleared asynchronously with the value in the RTI divider; hence, the COP timeout period will vary between 7x and 8x the RTI period.*

7.3.3 Clearing the COP Watchdog

To clear the COP watchdog and prevent a COP reset, write a logic 0 to bit 0 (COPC) of the COP register at location $07F0 (see **Figure 7-1**).

Section 9. Multifunction Timer Module

9.1 Contents

9.2 Introduction

The multifunction timer provides a timing reference with programmable real-time interrupt (RTI) capability. **Figure 9-1** shows the timer organization.

Features include:

- Timer overflow
- Four selectable interrupt rates
- Computer operating properly (COP) watchdog timer

interrupt request to be generated. To prevent this occurrence, clear the COP timer before changing RT1 and RT0.

Table 9-1. Real-Time Interrupt Rate Selection

RT1:RT0	Number of Cycles to RTI	RTI Period(1)	Number of Cycles to COP Reset	COP Timeout Period(1)
0 0	2^{14} = 16,384	8.2 ms	2^{17} = 131,072	65.5 ms
0 1	2^{15} = 32,768	16.4 ms	2^{18} = 262,144	131.1 ms
1 0	2^{16} = 65,536	32.8 ms	2^{19} = 524,288	262.1 ms
1 1	2^{17} = 131,072	65.5 ms	2^{20} = 1,048,576	524.3 ms

1. At 2-MHz bus, 4-MHz XTAL, 0.5 µs per cycle

9.5.2 Timer Counter Register

A 15-stage ripple counter is the core of the timer. The value of the first eight stages is readable at any time from the read-only timer counter register (TCR) shown in **Figure 9-4**.

Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-4. Timer Counter Register (TCR)

Power-on clears the entire counter chain and the internal clock begins clocking the counter. After 4064 cycles (or 16 cycles if the SOSCD bit in the mask option register is set), the power-on reset circuit is released, clearing the counter again and allowing the MCU to come out of reset.

A timer overflow function at the eighth counter stage allows a timer interrupt every 1024 internal clock cycles.

10.6 Power Considerations

The average chip junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

Where:

T_A = ambient temperature in °C
θ_{JA} = package thermal resistance, junction to ambient in °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$ = chip internal power dissipation
$P_{I/O}$ = power dissipation on input and output pins (user-determined)

For most applications, $P_{I/O} < P_{INT}$ and can be neglected.

Ignoring $P_{I/O}$, the relationship between P_D and T_J is approximately:

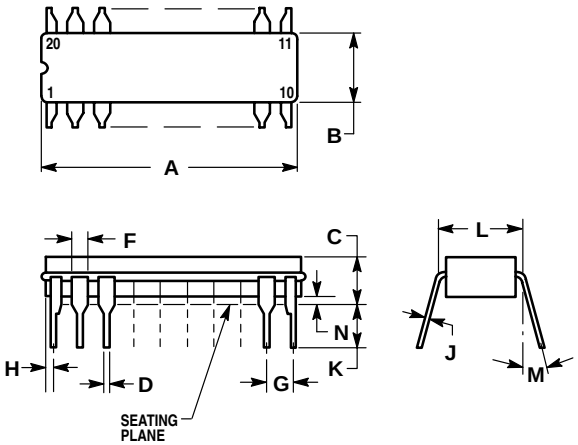
$$P_D = \frac{K}{T_J + 273°C} \quad (2)$$

Solving equations (1) and (2) for K gives:

$$= P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

11.5 Ceramic Dual In-Line Package (Case 732)



NOTES:
1. LEADS WITHIN 0.010 DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	INCHES	
DIM	MIN	MAX
A	0.940	0.990
B	0.260	0.295
C	0.150	0.200
D	0.015	0.022
F	0.055	0.065
G	0.100 BSC	
H	0.020	0.050
J	0.008	0.012
K	0.125	0.160
L	0.300 BSC	
M	0°	15°
N	0.010	0.040

Section 12. Ordering Information

12.1 Contents

12.2 Introduction

This section contains ordering information for the available package types.

12.3 MCU Order Numbers

Table 12-1 lists the MC order numbers.

Table 12-1. Order Numbers

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number(1)
PDIP	738-03	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1AP(2) MC68HC705J1AC(3)P MC68HC705J1AV(4)P
SOIC	751D-04	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1ADW(5) MC68HC705J1ACDW MC68HC705J1AVDW
Cerdip	732-03	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1AS(6) MC68HC705J1ACS MC68HC705J1AVS

1. Refer to **Appendix A. MC68HRC705J1A**, **Appendix B. MC68HSC705J1A**, and **Appendix C. MC68HSR705J1A** for ordering information on optional high-speed and resistor-capacitor oscillator devices.
2. P = Plastic dual in-line package (PDIP)
3. C = Extended temperature range
4. V = Automotive temperature range
5. DW = Small outline integrated circuit (SOIC)
6. S = Ceramic dual in-line package (cerdip)

Ordering Information

J

L