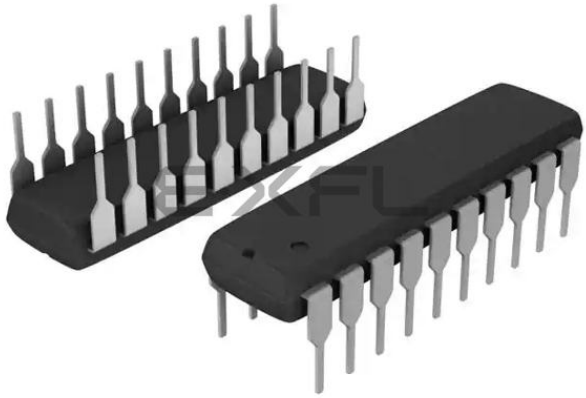

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Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705j1acpe

Revision History

Date	Revision Level	Description	Page Number(s)
May, 2002	4.0	**Figure 2-2. I/O Register Summary** — Corrected reset state for last entry (Mask Option Register)	37
		Figure 2-4. Mask Option Register (MOR) — Corrected reset state	41
		6.3.3 Pulldown Register A — Corrected note	91
		6.4.3 Pulldown Register B — Corrected note	94

List of Tables

1.3 Features

Features of the MC68HC705J1A include:

- Peripheral modules:
  - 15-stage multifunction timer
  - Computer operating properly (COP) watchdog
- 14 bidirectional input/output (I/O) lines, including:
  - 10-mA sink capability on four I/O pins
  - Mask option register (MOR) and software programmable pulldowns on all I/O pins
  - MOR selectable interrupt on four I/O pins, a keyboard scan feature
- MOR selectable sensitivity on external interrupt (edge- and level-sensitive or edge-sensitive only)
- On-chip oscillator with connections for:
  - Crystal
  - Ceramic resonator
  - Resistor-capacitor (RC) oscillator
  - External clock
- 1240 bytes of EPROM/OTPROM, including eight bytes for user vectors
- 64 bytes of user random-access memory (RAM)
- Memory-mapped I/O registers
- Fully static operation with no minimum clock speed
- Power-saving stop, halt, wait, and data-retention modes
- External interrupt mask bit and acknowledge bit
- Illegal address reset
- Internal steering diode and pullup resistor from $\overline{\text{RESET}}$ pin to V_{DD}

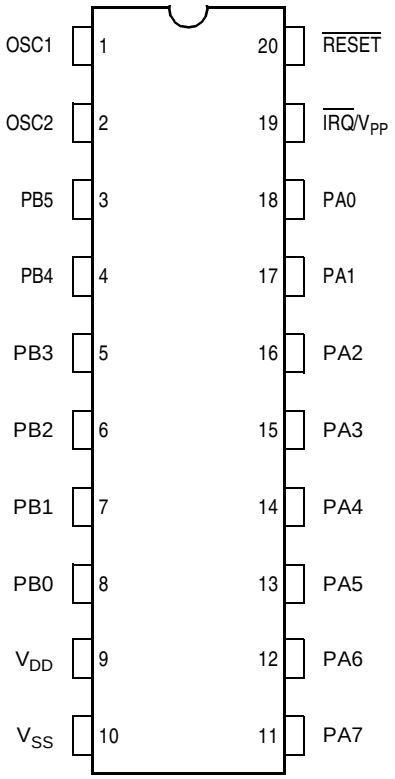

Figure 1-2. Pin Assignments

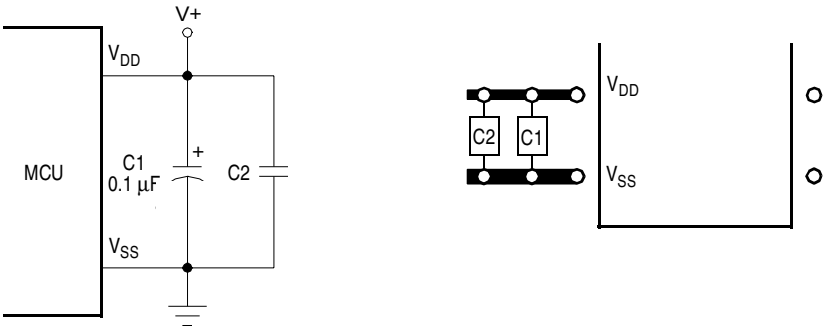

Figure 1-3. Bypassing Layout Recommendation

Mount the resonator and components as close as possible to the pins for startup stabilization and to minimize output distortion. An internal startup resistor of approximately 2 MΩ is provided between OSC1 and OSC2 as a programmable mask option.

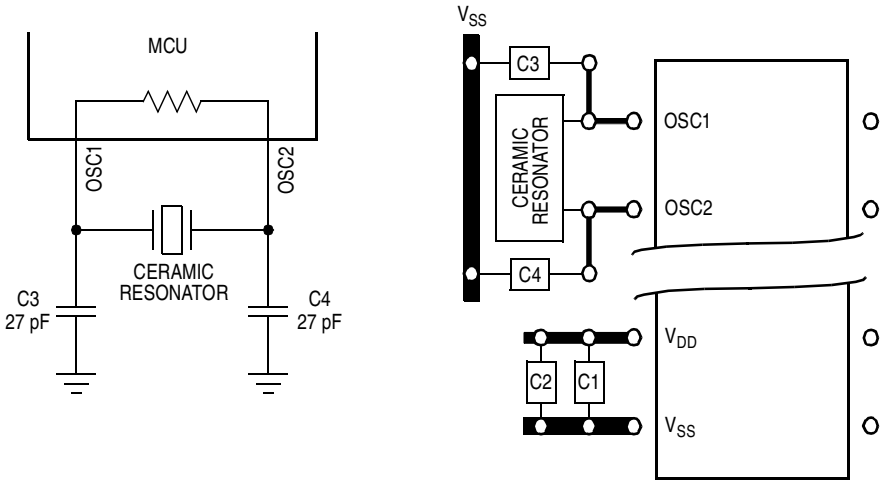

Figure 1-6. Ceramic Resonator Connections with Oscillator Internal Resistor Mask Option

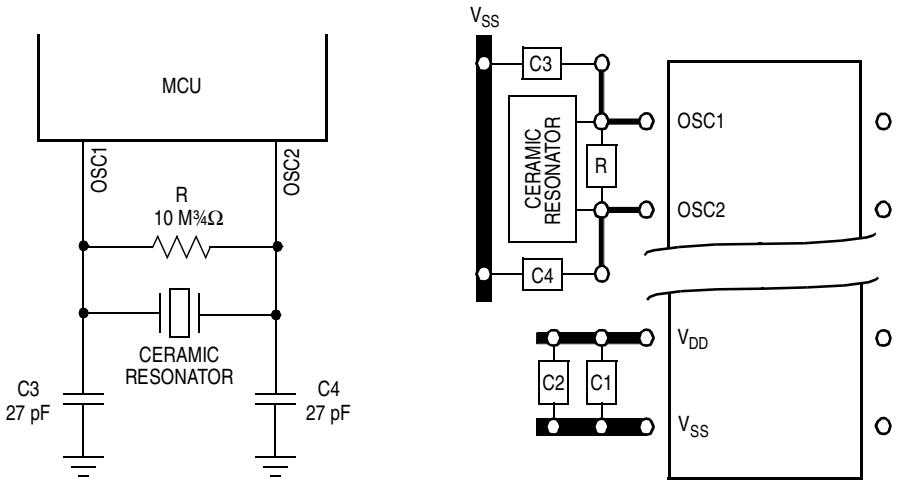

Figure 1-7. Ceramic Resonator Connections without Oscillator Internal Resistor Mask Option

1.7 $\overline{IRQ}/V_{PP}$

The external interrupt/programming voltage pin ($\overline{IRQ}/V_{PP}$) drives the asynchronous IRQ interrupt function of the CPU. Additionally, it is used to program the user EPROM and mask option register. (See **Section 2. Memory** and **Section 8. External Interrupt Module (IRQ)**.)

The LEVEL bit in the mask option register provides negative edge-sensitive triggering or both negative edge-sensitive and low level-sensitive triggering for the interrupt function.

If level-sensitive triggering is selected, the $\overline{IRQ}/V_{PP}$ input requires an external resistor to V_{DD} for wired-OR operation. If the $\overline{IRQ}/V_{PP}$ pin is not used, it must be tied to the V_{DD} supply.

The $\overline{IRQ}/V_{PP}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin should not exceed V_{DD} except when the pin is being used for programming the EPROM.

NOTE: *The mask option register can enable the PA0–PA3 pins to function as external interrupt pins.*

1.8 PA0–PA7

These eight input/output (I/O) lines comprise port A, a general-purpose, bidirectional I/O port. See **Section 8. External Interrupt Module (IRQ)** for information on PA0–PA3 external interrupts.

1.9 PB0–PB5

These six I/O lines comprise port B, a general-purpose, bidirectional I/O port.

2.6 EPROM/OTPROM

A microcontroller unit (MCU) with a quartz window has 1240 bytes of erasable, programmable ROM (EPROM). The quartz window allows EPROM erasure with ultraviolet light.

NOTE: *Keep the quartz window covered with an opaque material except when programming the MCU. Ambient light can affect MCU operation.*

In an MCU without the quartz window, the EPROM cannot be erased and serves as 1240 bytes of one-time programmable ROM (OTPROM).

These addresses are user EPROM/OTPROM locations:

- $0300–$07CF
- $07F8–$07FF, used for user-defined interrupt and reset vectors

The computer operating properly (COP) register (COPR) is an EPROM/OTPROM location at address $07F0.

The mask option register (MOR) is an EPROM/OTPROM location at address $07F1.

2.6.1 EPROM/OTPROM Programming

The two ways to program the EPROM/OTPROM are:

1. Manipulating the control bits in the EPROM programming register to program the EPROM/OTPROM on a byte-by-byte basis
2. Programming the EPROM/OTPROM with the M68HC705J in-circuit simulator (M68HC705JICS) available from Freescale

Table 3-6. Instruction Set Summary (Sheet 3 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	—	—	—	—	—	REL	AD	rr	6
CLC	Clear Carry Bit	C ← 0	—	—	—	—	0	INH	98		2
CLI	Clear Interrupt Mask	I ← 0	—	0	—	—	—	INH	9A		2
CLR *opr* CLRA CLRX CLR *opr*,X CLR ,X	Clear Byte	M ← $00 A ← $00 X ← $00 M ← $00 M ← $00	—	—	0	1	—	DIR INH INH IX1 IX	3F 4F 5F 6F 7F	dd ff 	5 3 3 6 5
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X	Compare Accumulator with Memory Byte	(A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A1 B1 C1 D1 E1 F1	ii dd hh ll ee ff ff 	2 3 4 5 4 3
COM *opr* COMA COMX COM *opr*,X COM ,X	Complement Byte (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (A) X ← ($\overline{X}$) = $FF – (X) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	—	—	↕	↕	1	DIR INH INH IX1 IX	33 43 53 63 73	dd ff 	5 3 3 6 5
CPX #*opr* CPX *opr* CPX *opr* CPX *opr*,X CPX *opr*,X CPX ,X	Compare Index Register with Memory Byte	(X) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A3 B3 C3 D3 E3 F3	ii dd hh ll ee ff ff 	2 3 4 5 4 3
DEC *opr* DECA DECX DEC *opr*,X DEC ,X	Decrement Byte	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3A 4A 5A 6A 7A	dd ff 	5 3 3 6 5
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X	EXCLUSIVE OR Accumulator with Memory Byte	A ← (A) ⊕ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A8 B8 C8 D8 E8 F8	ii dd hh ll ee ff ff 	2 3 4 5 4 3
INC *opr* INCA INCX INC *opr*,X INC ,X	Increment Byte	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3C 4C 5C 6C 7C	dd ff 	5 3 3 6 5

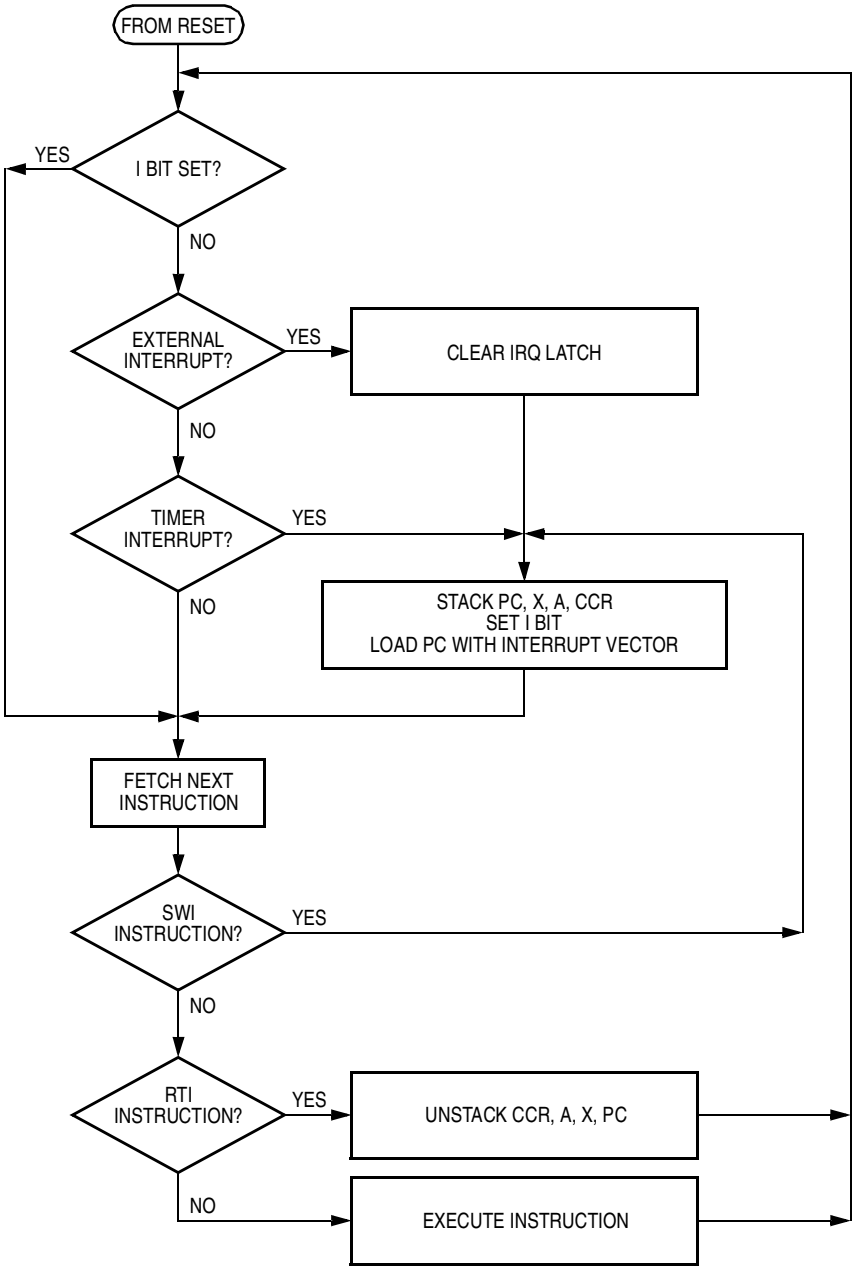

Figure 4-7. Interrupt Flowchart

Enabling halt mode prevents the computer operating properly (COP) watchdog from being inadvertently turned off by a STOP instruction.

- Data-retention mode — In data-retention mode, the MCU retains RAM contents and CPU register contents at V_{DD} voltages as low as 2.0 Vdc. The data-retention feature allows the MCU to remain in a low power-consumption state during which it retains data, but the CPU cannot execute instructions.

5.3 Exiting Stop and Wait Modes

The events described in this subsection bring the MCU out of stop mode and load the program counter with the reset vector or with an interrupt vector.

Exiting stop mode:

- External reset — A logic 0 on the $\overline{\text{RESET}}$ pin resets the MCU, starts the CPU clock, and loads the program counter with the contents of locations $07FE and $07FF.
- External interrupt — A high-to-low transition on the $\overline{\text{IRQ}}/V_{PP}$ pin or a low-to-high transition on an enabled port A external interrupt pin starts the CPU clock and loads the program counter with the contents of locations $07FA and $07FB.

Exiting wait mode:

- External reset — A logic 0 on the $\overline{\text{RESET}}$ pin resets the MCU, starts the CPU clock, and loads the program counter with the contents of locations $07FE and $07FF.
- External interrupt — A high-to-low transition on the $\overline{\text{IRQ}}/V_{PP}$ pin or a low-to-high transition on an enabled port A external interrupt pin starts the CPU clock and loads the program counter with the contents of locations $07FA and $07FB.

Section 6. Parallel Input/Output (I/O) Ports

6.1 Contents

6.2 Introduction

Fourteen bidirectional pins form one 8-bit input/output (I/O) port and one 6-bit I/O port. All the bidirectional port pins are programmable as inputs or outputs.

NOTE: *Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS}. Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.*

6.3 Port A

Port A is an 8-bit bidirectional port.

6.3.1 Port A Data Register

The port A data register (PORTA) contains a latch for each port A pin.

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset:	Unaffected by reset							

Figure 6-2. Port A Data Register (PORTA)

PA[7:0] — Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

Writing a logic 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a logic 0 disables the output buffer.

When bit DDRAx is a logic 1, reading address $0000 reads the PAx data latch. When bit DDRAx is a logic 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. **Table 6-1** summarizes the operation of the port A pins.

Table 6-1. Port A Pin Operation

Data Direction Bit	I/O Pin Mode	Accesses to Data Bit	
		Read	Write
0	Input, high-impedance	Pin	Latch(1)
1	Output	Latch	Latch

1. Writing affects the data register but does not affect input.

6.3.3 Pulldown Register A

Pulldown register A (PDRA) inhibits the pulldown devices on port A pins programmed as inputs.

NOTE: *If the SWPDI bit in the mask option register is programmed to logic 1, reset initializes all port A pins as inputs with disabled pulldown devices.*

Address: $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:	PDIA7	PDIA6	PDIA5	PDIA4	PDIA3	PDIA2	PDIA1	PDIA0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 6-5. Pulldown Register A (PDRA)

PDIA[7:0] — Pulldown Inhibit A Bits

PDIA[7:0] disable the port A pulldown devices. Reset clears PDIA[7:0].

1 = Corresponding port A pulldown device disabled
0 = Corresponding port A pulldown device not disabled

8.3.1 $\overline{IRQ}/V_{PP}$ Pin

An interrupt signal on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. The LEVEL bit in the mask option register provides negative edge-sensitive triggering or both negative edge-sensitive and low level-sensitive triggering for the interrupt function.

If edge- and level-sensitive triggering is selected, a falling edge or a low level on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. Edge- and level-sensitive triggering allows the use of multiple wired-OR external interrupt sources. An external interrupt request is latched as long as any source is holding the $\overline{IRQ}/V_{PP}$ pin low.

If level-sensitive triggering is selected, the $\overline{IRQ}/V_{PP}$ input requires an external resistor to V_{DD} for wired-OR operation. If the $\overline{IRQ}/V_{PP}$ pin is not used, it must be tied to the V_{DD} supply.

If edge-sensitive-only triggering is selected, a falling edge on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. A subsequent external interrupt request can be latched only after the voltage level on the $\overline{IRQ}/V_{PP}$ pin returns to logic 1 and then falls again to logic 0.

The $\overline{IRQ}/V_{PP}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin can affect the mode of operation and should not exceed V_{DD}.

8.3.2 Optional External Interrupts

The inputs for the lower four bits of port A (PA0–PA3) can be connected to the $\overline{IRQ}$ pin input of the CPU if enabled by the PIRQ bit in the mask option register. This capability allows keyboard scan applications where the transitions or levels on the I/O pins will behave the same as the $\overline{IRQ}/V_{PP}$ pin except for the inverted phase (logic 1, rising edge). The active state of the $\overline{IRQ}/V_{PP}$ pin is a logic 0 (falling edge).

The PA0–PA3 pins are selected as a group to function as IRQ interrupts and are enabled by the IRQE bit in the IRQ status and control register. The PA0–PA3 pins can be positive-edge triggered only or positive-edge and high-level triggered.

Section 9. Multifunction Timer Module

9.1 Contents

9.2 Introduction

The multifunction timer provides a timing reference with programmable real-time interrupt (RTI) capability. **Figure 9-1** shows the timer organization.

Features include:

- Timer overflow
- Four selectable interrupt rates
- Computer operating properly (COP) watchdog timer

TOF — Timer Overflow Flag

This read-only flag becomes set when the first eight stages of the counter roll over from $FF to $00. TOF generates a timer overflow interrupt request if TOIE is also set. Clear TOF by writing a logic 1 to the TOFR bit. Writing to TOF has no effect. Reset clears TOF.

RTIF — Real-Time Interrupt Flag

This read-only flag becomes set when the selected RTI output becomes active. RTIF generates a real-time interrupt request if RTIE is also set. Clear RTIF by writing a logic 1 to the RTIFR bit. Writing to RTIF has no effect. Reset clears RTIF.

TOIE — Timer Overflow Interrupt Enable Bit

This read/write bit enables timer overflow interrupts. Reset clears TOIE.

1 = Timer overflow interrupts enabled
0 = Timer overflow interrupts disabled

RTIE — Real-Time Interrupt Enable Bit

This read/write bit enables real-time interrupts. Reset clears RTIE.

1 = Real-time interrupts enabled
0 = Real-time interrupts disabled

TOFR — Timer Overflow Flag Reset Bit

Writing a logic 1 to this write-only bit clears the TOF bit. TOFR always reads as logic 0. Reset clears TOFR.

RTIFR — Real-Time Interrupt Flag Reset Bit

Writing a logic 1 to this write-only bit clears the RTIF bit. RTIFR always reads as logic 0. Reset clears RTIFR.

RT1 and RT0 — Real-Time Interrupt Select Bits

These read/write bits select one of four real-time interrupt rates, as shown in **Table 9-1**. Because the selected RTI output drives the COP watchdog, changing the real-time interrupt rate also changes the counting rate of the COP watchdog. Reset sets RT1 and RT0.

NOTE: *Changing RT1 and RT0 when a COP timeout is imminent can cause a real-time interrupt request to be missed or an additional real-time*

10.8 3.3-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD}– 0.1	 — —	 0.1 —	 V
Output high voltage (I_{Load} = –0.2 mA) PA0–PA7, PB0–PB5	V_{OH}	V_{DD} – 0.3	—	—	V
Output low voltage (I_{Load} = 0.4 mA) PA0–PA3, PB0–PB5 (I_{Load} = 5.0 mA) PA4–PA7	V_{OL}	—	—	 0.3 0.3	V
Input high voltage PA0–PA7, PB0–PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current Run Mode[3] Wait Mode[4] Stop Mode[5] 25°C –40 to 105°C	 I_{DD}	 — — — —	 1.2 0.25 0.1 1.0	 4.0 1.5 5 10	 mA mA µA µA
I/O ports hi-z leakage current PA0–PA7, PB0–PB5 (without individual pulldown activated)	I_{IL}	—	0.1	±1	µA
Input pulldown current PA0–PA7, PB0–PB5 (with individual pulldown activated)	I_{IL}	12	30	100	µA
Input pullup current $\overline{RESET}$	I_{IL}	–10	–25	–45	µA
Input current[6] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{In}	—	0.1	±1	µA
Capacitance Ports (as inputs or outputs) $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1, OSC2	 C_{Out} C_{In}	 — —	 — —	 12 8	 pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2[7]	R_{osc}	1.0	2.0	3.0	MΩ

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source (f_{osc} = 2.0 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source (f_{osc} = 2.0 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V
6. Only input high current rated to +1 µA on $\overline{RESET}$.
7. The R_{osc} value selected for RC oscillator versions of this device is unspecified. See **Appendix C. MC68HSR705J1A** for additional information.

Appendix A. MC68HRC705J1A

A.1 Contents

A.2 Introduction

This appendix introduces the MC68HRC705J1A, a resistor-capacitor (RC) oscillator mask option version of the MC68HC705J1A. All of the information in this document applies to the MC68HRC705J1A with the exceptions given in this appendix.

C.7 Package Types and Order Numbers

Table C-1. MC68HSR705J1A (High-Speed RC Oscillator Option) Order Numbers(1)

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number
PDIP	738-03	20	0 to 70°C –40 to +85°C	MC68HSR705J1AP(2) MC68HSR705J1AC(3)P
SOIC	751D-04	20	0 to 70°C –40 to +85°C	MC68HSR705J1ADW(4) MC68HSR705J1ACDW
Cerdip	732-03	20	0 to 70°C –40 to +85°C	MC68HSR705J1AS(5) MC68HSR705J1ACS

1. Refer to **Section 12. Ordering Information** for standard part ordering information.
2. P = plastic dual in-line package (PDIP)
3. C = extended temperature range
4. DW = small outline integrated circuit (SOIC)
5. S = ceramic dual in-line package (cerdip)

M

N