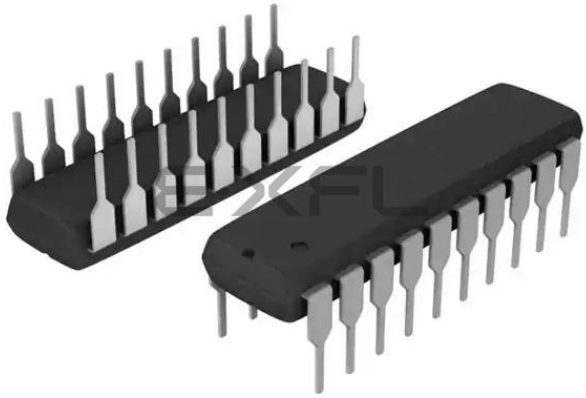

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Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hsc705j1acpe

List of Figures

2.4 Input/Output Register Summary

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 89.	Read:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PORTB) See page 92.	Read:	0	0	PB5	PB4	PB3	PB2	PB1	PB0
		Write:								
		Reset:	Unaffected by reset							
$0002	Unimplemented									
$0003	Unimplemented									
$0004	Data Direction Register A (DDRA) See page 90.	Read:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 93.	Read:	0	0	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0006	Unimplemented									
$0007	Unimplemented									
$0008	Timer Status and Control Register (TSCR) See page 112.	Read:	TOF	RTIF	TOIE	RTIE	0	0	RT1	RT0
		Write:					TOFR	RTIFR		
		Reset:	0	0	0	0	0	0	1	1

= Unimplemented R = Reserved

Figure 2-2. I/O Register Summary (Sheet 1 of 3)

Table 3-6. Instruction Set Summary (Sheet 2 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3
BHS *rel*	Branch if Higher or Same	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BIH *rel*	Branch if IRQ Pin High	PC ← (PC) + 2 + *rel* ? IRQ = 1	—	—	—	—	—	REL	2F	rr	3
BIL *rel*	Branch if IRQ Pin Low	PC ← (PC) + 2 + *rel* ? IRQ = 0	—	—	—	—	—	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X	Bit Test Accumulator with Memory Byte	(A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff	2 3 4 5 4 3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? C ∨ Z = 1	—	—	—	—	—	REL	23	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? I = 0	—	—	—	—	—	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? N = 1	—	—	—	—	—	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? I = 1	—	—	—	—	—	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? Z = 0	—	—	—	—	—	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? N = 0	—	—	—	—	—	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel* ? 1 = 1	—	—	—	—	—	REL	20	rr	3
BRCLR *n opr rel*	Branch if Bit n Clear	PC ← (PC) + 2 + *rel* ? Mn = 0	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2 + *rel* ? 1 = 0	—	—	—	—	—	REL	21	rr	3
BRSET *n opr rel*	Branch if Bit n Set	PC ← (PC) + 2 + *rel* ? Mn = 1	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n opr*	Set Bit n	Mn ← 1	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5

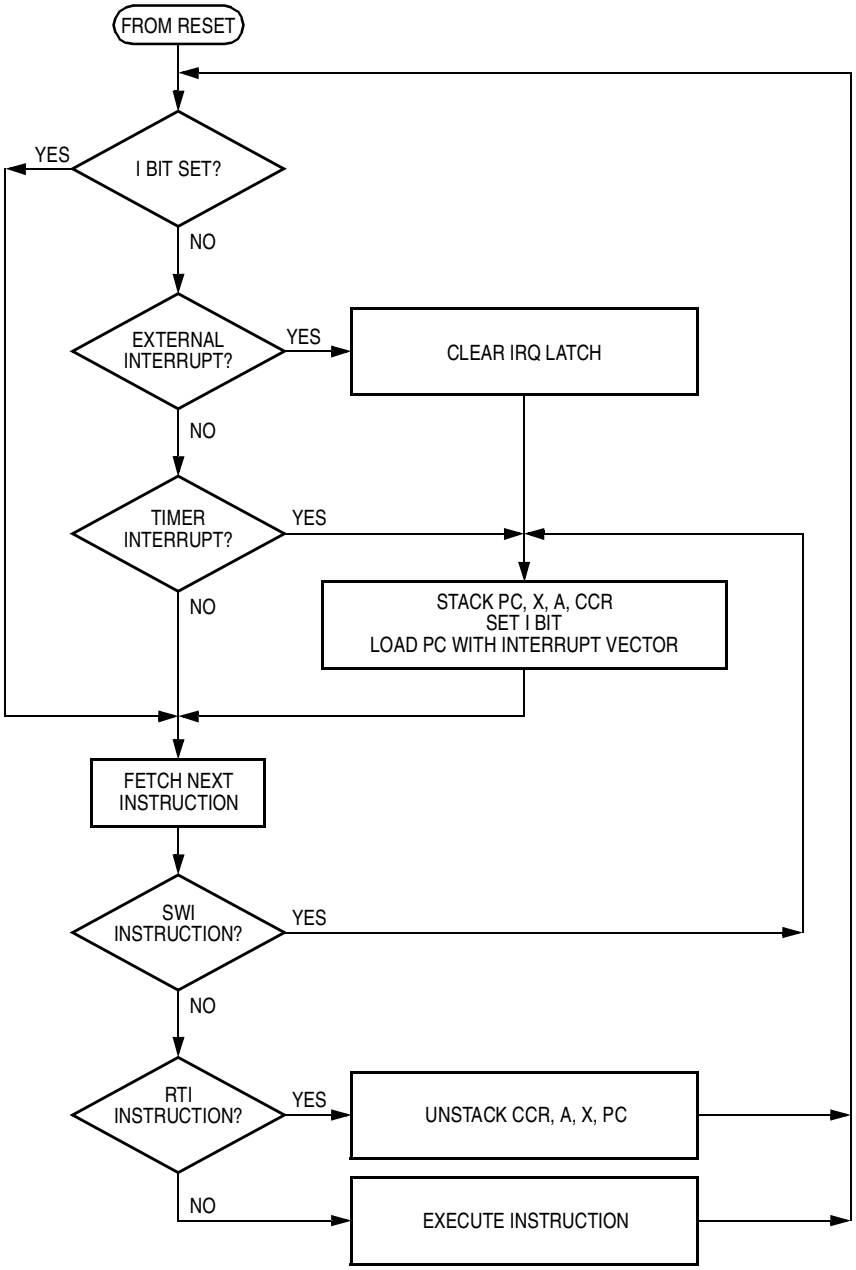

Figure 4-7. Interrupt Flowchart

6.3.2 Data Direction Register A

Data direction register A (DDRA) determines whether each port A pin is an input or an output.

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

Figure 6-3. Data Direction Register A (DDRA)

DDRA[7:0] — Data Direction Register A Bits

These read/write bits control port A data direction. Reset clears DDRA[7:0], configuring all port A pins as inputs.

1 = Corresponding port A pin configured as output
0 = Corresponding port A pin configured as input

NOTE: *Avoid glitches on port A pins by writing to the port A data register before changing data direction register A bits from 0 to 1.*

Figure 6-4 shows the I/O logic of port A.

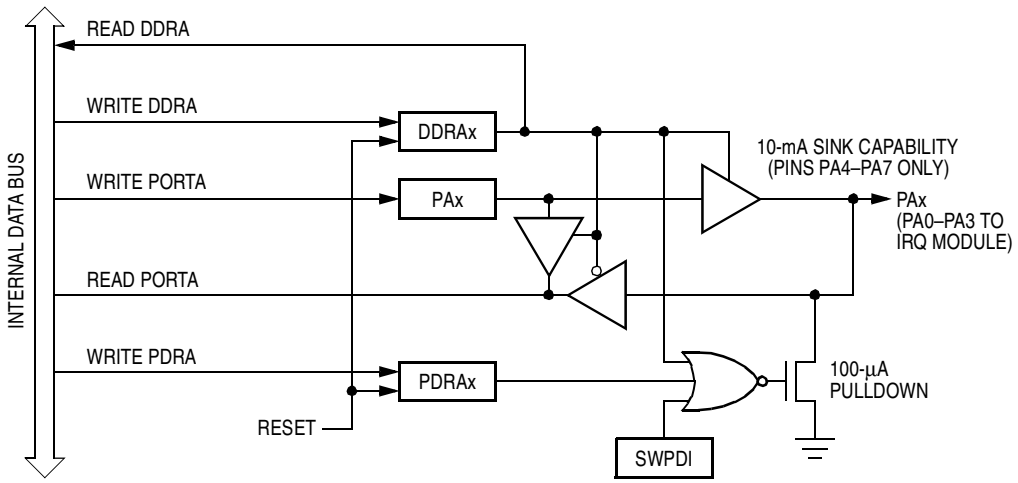

Figure 6-4. Port A I/O Circuitry

Clearing the COP bit disables the COP watchdog timer regardless of the $\overline{IRQ}/V_{PP}$ pin voltage.

If the main program executes within the COP timeout period, the clearing routine should be executed only once. If the main program takes longer than the COP timeout period, the clearing routine must be executed more than once.

NOTE: *Place the clearing routine in the main program and not in an interrupt routine. Clearing the COP watchdog in an interrupt routine might prevent COP watchdog timeouts even though the main program is not operating properly.*

7.4 Interrupts

The COP watchdog does not generate interrupts.

7.5 COP Register

The COP register (COPR) is a write-only register that returns the contents of EPROM location $07F0 when read.

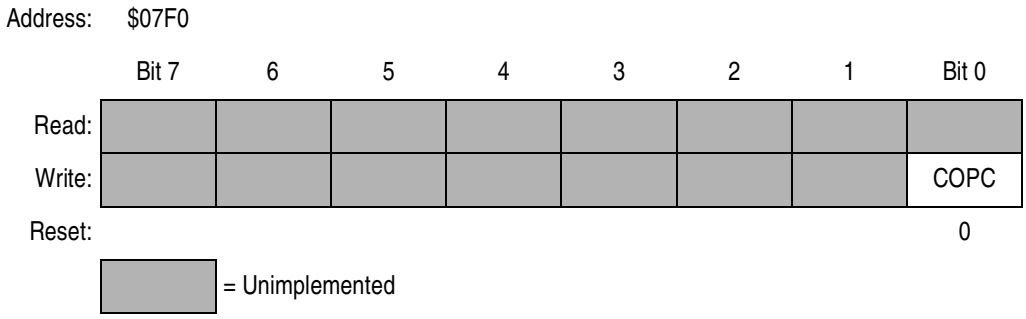

Figure 7-1. COP Register (COPR)

COPC — COP Clear Bit

This write-only bit resets the COP watchdog. Reading address $07F0 returns undefined results.

Section 8. External Interrupt Module (IRQ)

8.1 Contents

8.2 Introduction

The external interrupt (IRQ) module provides asynchronous external interrupts to the CPU. These sources can generate external interrupts:

- $\overline{IRQ}/V_{PP}$ pin
- PA0–PA3 pins

Features include:

- Dedicated external interrupt pin ($\overline{IRQ}/V_{PP}$)
- Selectable interrupt on four input/output (I/O) pins (PA0–PA3)
- Programmable edge-only or edge- and level-interrupt sensitivity

8.5 External Interrupt Timing

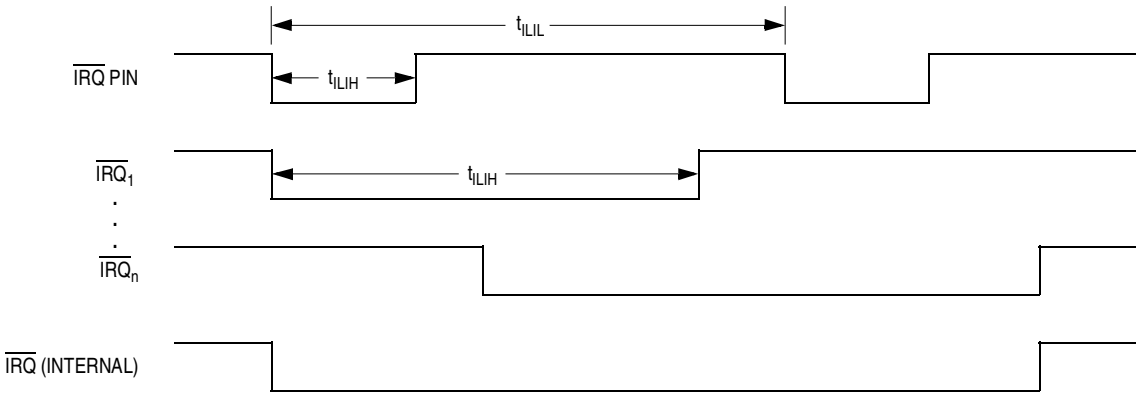

Figure 8-4. External Interrupt Timing

8.5.1 5.0-Volt External Interrupt Timing Characteristics

Characteristic(1)	Symbol	Min	Max	Unit
IRQ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}(2)
IRQ interrupt pulse width (edge- and level-triggered)	t_{ILIH}	1.5	Note(3)	t_{cyc}
PA0–PA3 interrupt pulse width high (edge-triggered)	t_{ILIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width high (edge- and level-triggered)	t_{ILIH}	1.5	Note(3)	t_{cyc}

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. $t_{cyc} = 1/f_{op}$; $f_{op} = f_{osc}/2$.
3. The minimum, t_{ILIL}, should not be less than the number of interrupt service routine cycles plus 19 t_{cyc}.

8.5.2 3.3-Volt External Interrupt Timing Characteristics

Characteristic(1)	Symbol	Min	Max	Unit
IRQ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}(2)
IRQ interrupt pulse width (edge- and level-triggered)	t_{ILIH}	1.5	Note(3)	t_{cyc}
PA0–PA3 interrupt pulse width high (edge-triggered)	t_{ILIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width high (edge- and level-triggered)	t_{ILIH}	1.5	Note(3)	t_{cyc}

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. $t_{cyc} = 1/f_{op}$; $f_{op} = f_{osc}/2$.
3. The minimum, t_{ILIL}, should not be less than the number of interrupt service routine cycles plus 19 t_{cyc}.

10.4 Operating Temperature Range

Package Type	Symbol	Value (T_L to T_H)	Unit
MC68HC705J1AP(1), DW(2), S(3)	T_A	0 to 70	°C
MC68HC705J1AC(4)P, CDW, CS	T_A	–40 to +85	°C
MC68HC705J1AV(5)P, VDW, VS	T_A	–40 to +105	°C

1. P = plastic dual in-line package (PDIP)
2. DW = small outline integrated circuit (SOIC)
3. S = ceramic DIP (cerdip)
4. C = extended temperature range
5. V = automotive temperature range

10.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance MC68HC705J1AP(1) MC68HC705J1ADW(2) MC68HC705J1AS(3)	θ_{JA}	60	°C/W

1. P = plastic dual in-line package (PDIP)
2. DW = small outline integrated circuit (SOIC)
3. S = ceramic DIP (cerdip)

10.7 5.0-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD} – 0.1	 — —	 0.1 —	 V
Output high voltage (I_{Load} = –0.8 mA) PA0–PA7, PB0–PB5	V_{OH}	V_{DD} – 0.8	—	—	V
Output low voltage (I_{Load} = 1.6 mA) PA0–PA3, PB0–PB5 (I_{Load} = 10.0 mA) PA4–PA7	V_{OL}	—	—	0.4 0.4	V
Input high voltage PA0–PA7, PB0–PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current Run mode[3] Wait mode[4] Stop mode[5] 25°C –40 to 105°C	I_{DD}	 — — — —	 3.5 0.45 0.2 2.0	 6.0 2.75 10 20	 mA mA µA µA
I/O ports hi-z leakage current PA0–PA7, PB0–PB5 (without individual pulldown activated)	I_{IL}	—	0.2	±1	µA
Input pulldown current PA0–PA7, PB0–PB5 (with individual pulldown activated)	I_{IL}	35	80	200	µA
Input pullup current $\overline{RESET}$	I_{IL}	–15	–35	–85	µA
Input current[6] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{In}	—	0.2	±1	µA
Capacitance Ports (as inputs or outputs) $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1, OSC2	 C_{Out} C_{In}	 — —	 — —	 12 8	 pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2[7]	R_{osc}	1.0	2.0	3.0	MΩ

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source (f_{osc} = 4.2 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source (f_{osc} = 4.2 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V
6. Only input high current rated to +1 µA on $\overline{RESET}$.
7. The R_{osc} value selected for RC oscillator versions of this device is unspecified. See **Appendix C. MC68HSR705J1A** for additional information.

10.8 3.3-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD}– 0.1	 — —	 0.1 —	 V
Output high voltage (I_{Load} = –0.2 mA) PA0–PA7, PB0–PB5	V_{OH}	V_{DD} – 0.3	—	—	V
Output low voltage (I_{Load} = 0.4 mA) PA0–PA3, PB0–PB5 (I_{Load} = 5.0 mA) PA4–PA7	V_{OL}	—	—	 0.3 0.3	V
Input high voltage PA0–PA7, PB0–PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current Run Mode[3] Wait Mode[4] Stop Mode[5] 25°C –40 to 105°C	 I_{DD}	 — — — —	 1.2 0.25 0.1 1.0	 4.0 1.5 5 10	 mA mA µA µA
I/O ports hi-z leakage current PA0–PA7, PB0–PB5 (without individual pulldown activated)	I_{IL}	—	0.1	±1	µA
Input pulldown current PA0–PA7, PB0–PB5 (with individual pulldown activated)	I_{IL}	12	30	100	µA
Input pullup current $\overline{RESET}$	I_{IL}	–10	–25	–45	µA
Input current[6] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{In}	—	0.1	±1	µA
Capacitance Ports (as inputs or outputs) $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1, OSC2	 C_{Out} C_{In}	 — —	 — —	 12 8	 pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2[7]	R_{osc}	1.0	2.0	3.0	MΩ

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source (f_{osc} = 2.0 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source (f_{osc} = 2.0 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V
6. Only input high current rated to +1 µA on $\overline{RESET}$.
7. The R_{osc} value selected for RC oscillator versions of this device is unspecified. See **Appendix C. MC68HSR705J1A** for additional information.

Electrical Specifications

Section 12. Ordering Information

12.1 Contents

12.2 Introduction

This section contains ordering information for the available package types.

12.3 MCU Order Numbers

Table 12-1 lists the MC order numbers.

Table 12-1. Order Numbers

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number(1)
PDIP	738-03	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1AP(2) MC68HC705J1AC(3)P MC68HC705J1AV(4)P
SOIC	751D-04	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1ADW(5) MC68HC705J1ACDW MC68HC705J1AVDW
Cerdip	732-03	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1AS(6) MC68HC705J1ACS MC68HC705J1AVS

1. Refer to **Appendix A. MC68HRC705J1A**, **Appendix B. MC68HSC705J1A**, and **Appendix C. MC68HSR705J1A** for ordering information on optional high-speed and resistor-capacitor oscillator devices.
2. P = Plastic dual in-line package (PDIP)
3. C = Extended temperature range
4. V = Automotive temperature range
5. DW = Small outline integrated circuit (SOIC)
6. S = Ceramic dual in-line package (cerdip)

C.5 RC Oscillator Connections (No External Resistor)

For maximum cost reduction, the RC oscillator mask connections shown in **Figure C-2** allow the on-chip oscillator to be driven with **no** external components. This can be accomplished by programming the oscillator internal resistor (OSCRES) bit in the mask option register to a logic 1. When programming the OSCRES bit for the MC68HSR705J1A, an internal resistor is selected which yields typical internal oscillator frequencies as shown in **Figure C-3**. The internal resistance for this device is different than the resistance of the selectable internal resistor on the MC68HC705J1A and the MC68HSC705J1A devices.

NOTE: *This option is not available on the ROM version of this device (MC68HC05J1A).*

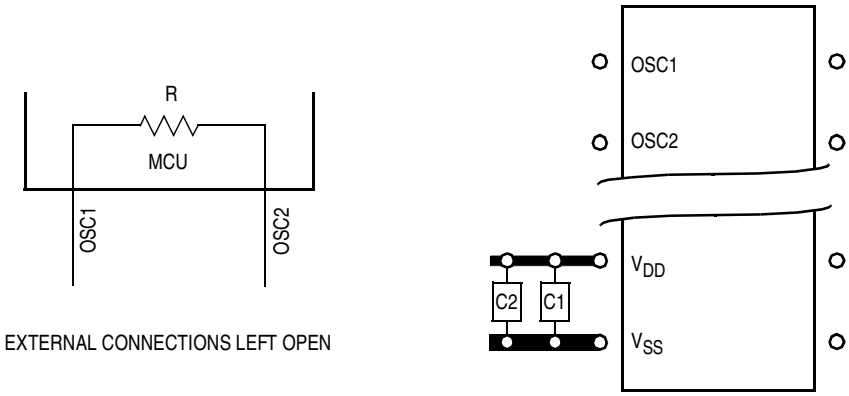

Figure C-2. RC Oscillator Connections (No External Resistor)

J

L

R

S

T