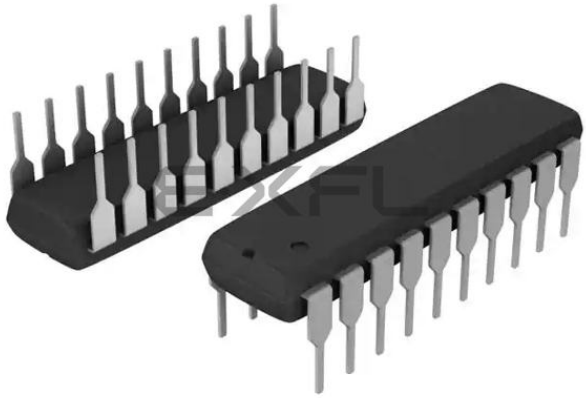

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hsr705j1acpe

List of Sections

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Section 1. General Description

Section 2. Memory

Table of Contents

1.2 Introduction

The MC68HC705J1A is a member of Motorola's low-cost, high-performance M68HC05 Family of 8-bit microcontroller units (MCUs). The M68HC05 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the popular M68HC05 central processor unit (CPU) and are available with a variety of subsystems, memory sizes and types, and package types.

On-chip memory of the MC68HC705J1A includes 1240 bytes of erasable, programmable read-only memory (EPROM). In packages without the transparent window for EPROM erasure, the 1240 EPROM bytes serve as one-time programmable read-only memory (OTPROM).

The MC68HRC705J1A is a resistor-capacitor (RC) oscillator mask option version of the MC68HC705J1A and is discussed in **Appendix A. MC68HRC705J1A**.

A high-speed version of the MC68HC705J1A, the MC68HSC705J1A, is discussed in **Appendix B. MC68HSC705J1A**.

The MC68HSR705J1A, discussed in **Appendix C. MC68HSR705J1A**, is a high-speed version of the MC68HRC705J1A.

A functional block diagram of the MC68HC705J1A is shown in **Figure 1-1**.

1.4 Programmable Options

The options in **Table 1-1** are programmable in the mask option register (MOR).

Table 1-1. Programmable Options

Feature	Option
COP watchdog timer	Enabled or disabled
External interrupt triggering	Edge-sensitive only or edge- and level-sensitive
Port A $\overline{IRQ}$ pin interrupts	Enabled or disabled
Port pulldown resistors	Enabled or disabled
STOP instruction mode	Stop mode or halt mode
Crystal oscillator internal resistor	Enabled or disabled
EPROM security	Enabled or disabled
Short oscillator delay counter	Enabled or disabled

1.5 Pin Assignments

Figure 1-2 shows the MC68HC705J1A pin assignments.

1.5.1 V_{DD} and V_{SS}

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Very fast signal transitions occur on the MCU pins, placing high, short-duration current demands on the power supply. To prevent noise problems, take special care as **Figure 1-3** shows, by placing the bypass capacitors as close as possible to the MCU. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.

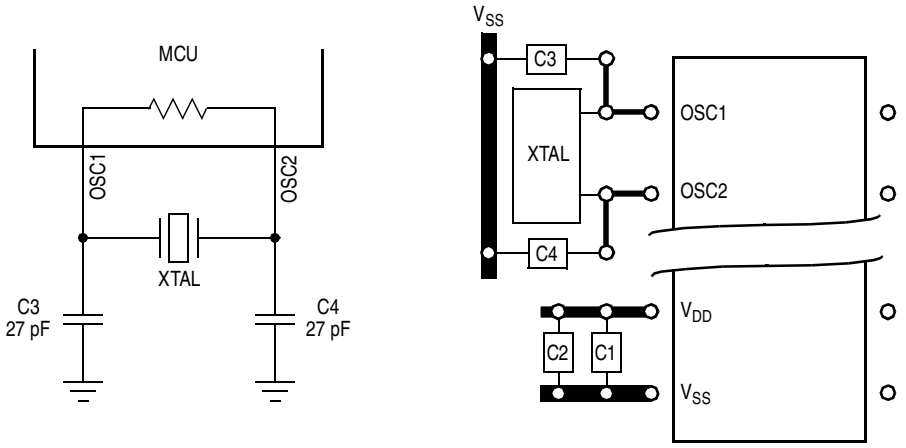


Figure 1-4. Crystal Connections with Oscillator Internal Resistor Mask Option

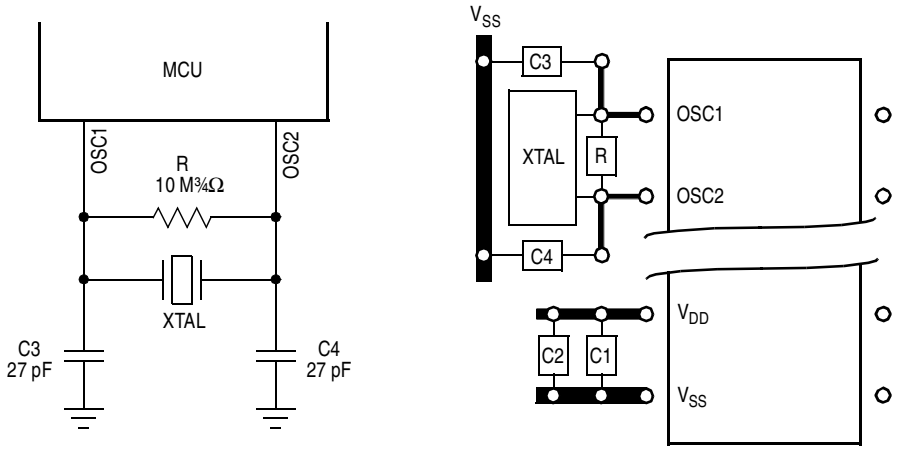


Figure 1-5. Crystal Connections without Oscillator Internal Resistor Mask Option

1.5.2.2 Ceramic Resonator Oscillator

To reduce cost, use a ceramic resonator instead of the crystal. The circuits shown in **Figure 1-6** and **Figure 1-7** show ceramic resonator circuits. Follow the resonator manufacturer's recommendations, as the resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances.

1.5.2.3 RC Oscillator

Refer to **Appendix A. MC68HRC705J1A** and **Appendix C. MC68HSR705J1A**.

1.5.2.4 External Clock

An external clock from another complementary metal-oxide semiconductor (CMOS)-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in **Figure 1-8**. This configuration is possible regardless of whether the crystal/ceramic resonator or the RC oscillator is enabled.

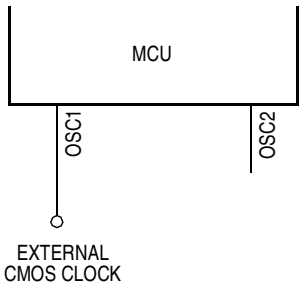


Figure 1-8. External Clock Connections

1.6 $\overline{\text{RESET}}$

Applying a logic 0 to the $\overline{\text{RESET}}$ pin forces the MCU to a known startup state. An internal reset also pulls the $\overline{\text{RESET}}$ pin low. An internal resistor to V_{DD} pulls the $\overline{\text{RESET}}$ pin high. A steering diode between the $\overline{\text{RESET}}$ and V_{DD} pins discharges any $\overline{\text{RESET}}$ pin voltage when power is removed from the MCU. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity as an input. Refer to **Section 4. Resets and Interrupts** for more information.

2.4 Input/Output Register Summary

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 89.	Read:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PORTB) See page 92.	Read:	0	0	PB5	PB4	PB3	PB2	PB1	PB0
		Write:								
		Reset:	Unaffected by reset							
$0002	Unimplemented									
$0003	Unimplemented									
$0004	Data Direction Register A (DDRA) See page 90.	Read:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 93.	Read:	0	0	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0006	Unimplemented									
$0007	Unimplemented									
$0008	Timer Status and Control Register (TSCR) See page 112.	Read:	TOF	RTIF	TOIE	RTIE	0	0	RT1	RT0
		Write:					TOFR	RTIFR		
		Reset:	0	0	0	0	0	0	1	1

= Unimplemented R = Reserved

Figure 2-2. I/O Register Summary (Sheet 1 of 3)

H — Half-Carry Flag

The CPU sets the half-carry flag when a carry occurs between bits 3 and 4 of the accumulator during an ADD (add without carry) or ADC (add with carry) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations.

I — Interrupt Mask Bit

Setting the interrupt mask disables interrupts. If an interrupt request occurs while the interrupt mask is logic 0, the CPU saves the CPU registers on the stack, sets the interrupt mask, and then fetches the interrupt vector. If an interrupt request occurs while the interrupt mask is logic 1, the interrupt request is latched. Normally, the CPU processes the latched interrupt request as soon as the interrupt mask is cleared again.

A return-from-interrupt instruction (RTI) unstacks the CPU registers, restoring the interrupt mask to its cleared state. After any reset, the interrupt mask is set and can be cleared only by a software instruction.

N — Negative Flag

The CPU sets the negative flag when an ALU operation produces a negative result.

Z — Zero Flag

The CPU sets the zero flag when an ALU operation produces a result of $00.

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some logical operations and data manipulation instructions also clear or set the carry/borrow flag.

3.6.2.5 Control Instructions

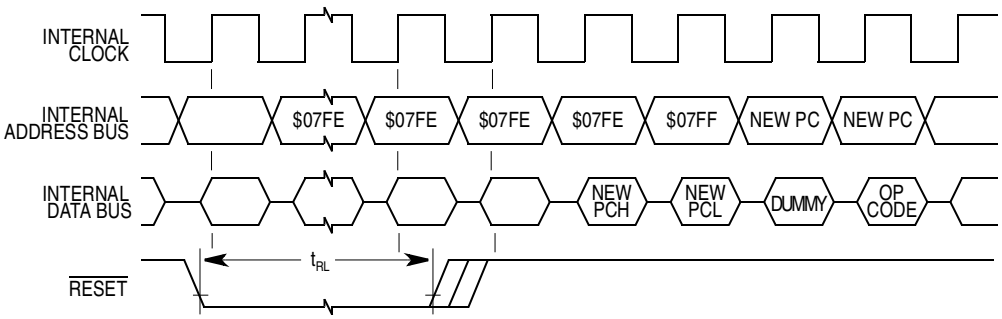
These instructions act on CPU registers and control CPU operation during program execution.

Table 3-5. Control Instructions

Instruction	Mnemonic
Clear carry bit	CLC
Clear interrupt mask	CLI
No operation	NOP
Reset stack pointer	RSP
Return from interrupt	RTI
Return from subroutine	RTS
Set carry bit	SEC
Set interrupt mask	SEI
Stop oscillator and enable $\overline{\text{IRQ}}$ pin	STOP
Software interrupt	SWI
Transfer accumulator to index register	TAX
Transfer index register to accumulator	TXA
Stop CPU clock and enable interrupts	WAIT

4.3.2 External Reset

A logic 0 applied to the $\overline{\text{RESET}}$ pin for 1 1/2 t_{cyc} generates an external reset. A Schmitt trigger senses the logic level at the $\overline{\text{RESET}}$ pin.



Notes:
1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 4-3. External Reset Timing

Table 4-1. External Reset Timing

Characteristic	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ pulse width	t_{RL}	1.5	—	t_{cyc}

4.3.3 COP Watchdog Reset

A timeout of the COP watchdog generates a COP reset. The COP watchdog is part of a software error detection system and must be cleared periodically to start a new timeout period. To clear the COP watchdog and prevent a COP reset, write a logic 0 to bit 0 (COPC) of the COP register at location $07F0.

4.3.4 Illegal Address Reset

An opcode fetch from an address not in random-access memory (RAM) or erasable, programmable read-only memory (EPROM) generates a reset.

The CPU clears the IRQ latch during interrupt processing, so that another interrupt signal on the $\overline{IRQ}/V_{PP}$ pin can latch another interrupt request during the interrupt service routine. As soon as the I bit is cleared during the return from interrupt, the CPU can recognize the new interrupt request. **Figure 4-4** shows the $\overline{IRQ}/V_{PP}$ pin interrupt logic.

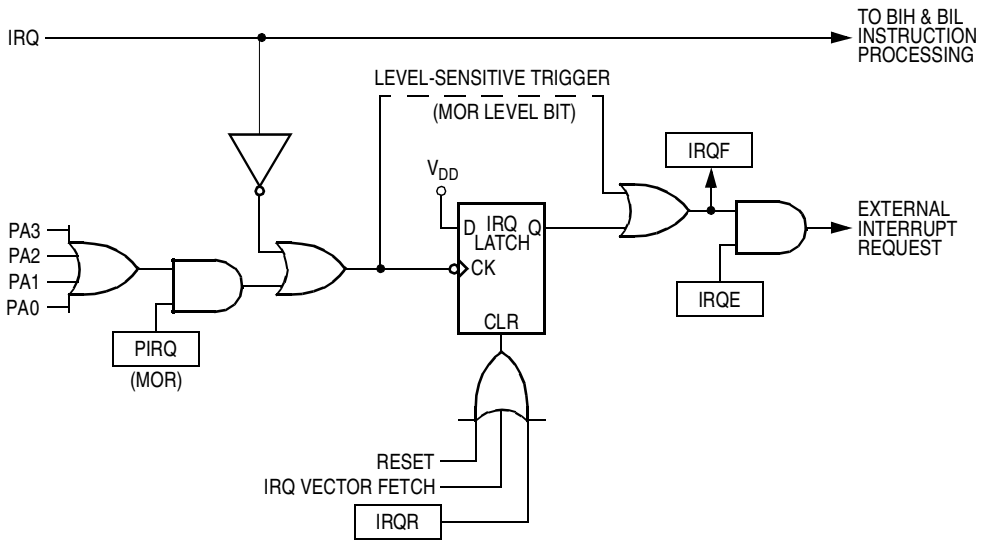


Figure 4-4. External Interrupt Logic

Setting the I bit in the condition code register disables external interrupts.

The port A external interrupt bit (PIRQ) in the mask option register enables pins PA0–PA3 to function as external interrupt pins.

The external interrupt sensitivity bit (LEVEL) in the mask option register controls interrupt triggering sensitivity of external interrupt pins. The $\overline{IRQ}/V_{PP}$ pin can be negative-edge triggered only or negative-edge and low-level triggered. Port A external interrupt pins can be positive-edge triggered only or both positive-edge and high-level triggered. The level-sensitive triggering option allows multiple external interrupt sources to be wire-ORed to an external interrupt pin. An external interrupt request, shown in **Figure 4-5**, is latched as long as any source is holding an external interrupt pin low.

4.4.3 Timer Interrupts

The timer can generate these interrupt requests:

- Real time
- Timer overflow

Setting the I bit in the condition code register disables timer interrupts.

4.4.3.1 Real-Time Interrupt

A real-time interrupt occurs if the real-time interrupt flag, RTIF, becomes set while the real-time interrupt enable bit, RTIE, is also set. RTIF and RTIE are in the timer status and control register.

4.4.3.2 Timer Overflow Interrupt

A timer overflow interrupt request occurs if the timer overflow flag, TOF, becomes set while the timer overflow interrupt enable bit, TOIE, is also set. TOF and TOIE are in the timer status and control register.

4.4.4 Interrupt Processing

The CPU takes these actions to begin servicing an interrupt:

- Stores the CPU registers on the stack in the order shown in **Figure 4-6**
- Sets the I bit in the condition code register to prevent further interrupts
- Loads the program counter with the contents of the appropriate interrupt vector locations:
  - $07FC and $07FD (software interrupt vector)
  - $07FA and $07FB (external interrupt vector)
  - $07F8 and $07F9 (timer interrupt vector)

The return-from-interrupt (RTI) instruction causes the CPU to recover the CPU registers from the stack as shown in **Figure 4-6**.

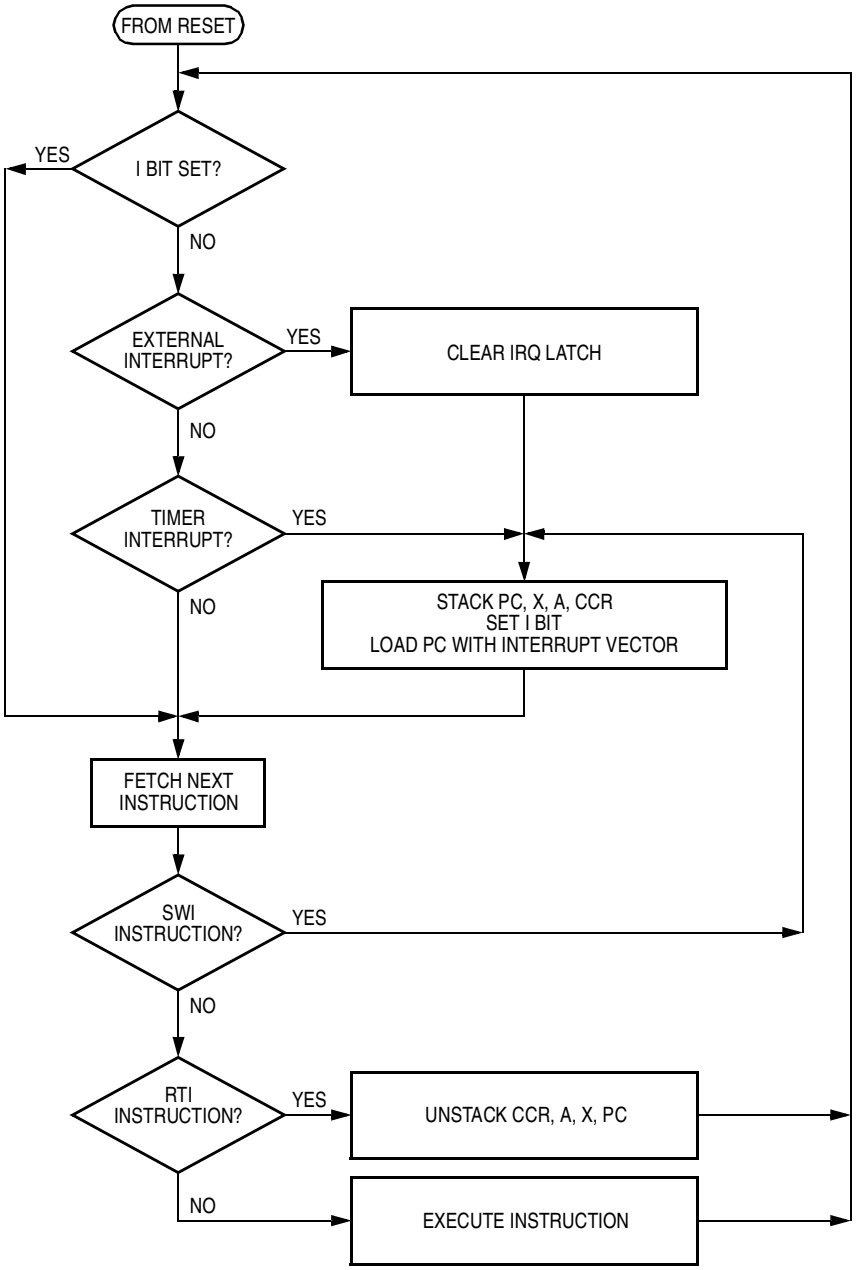


Figure 4-7. Interrupt Flowchart

Section 6. Parallel Input/Output (I/O) Ports

6.1 Contents

6.2 Introduction

Fourteen bidirectional pins form one 8-bit input/output (I/O) port and one 6-bit I/O port. All the bidirectional port pins are programmable as inputs or outputs.

NOTE: *Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS}. Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.*

6.4.2 Data Direction Register B

Data direction register B (DDRB) determines whether each port B pin is an input or an output.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 6-7. Data Direction Register B (DDRB)

DDRB[5:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[5:0], configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured as input

NOTE: *Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1.*

Figure 6-8 shows the I/O logic of port B.

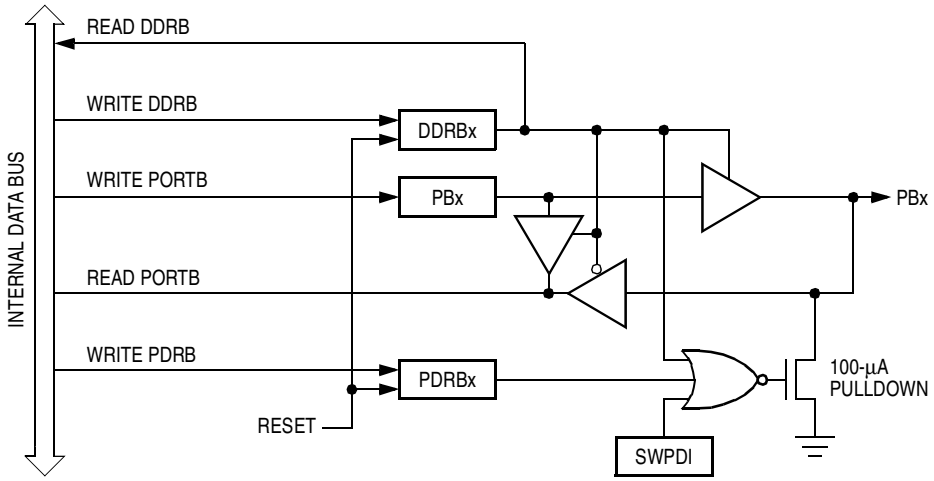


Figure 6-8. Port B I/O Circuitry

8.3.1 $\overline{IRQ}/V_{PP}$ Pin

An interrupt signal on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. The LEVEL bit in the mask option register provides negative edge-sensitive triggering or both negative edge-sensitive and low level-sensitive triggering for the interrupt function.

If edge- and level-sensitive triggering is selected, a falling edge or a low level on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. Edge- and level-sensitive triggering allows the use of multiple wired-OR external interrupt sources. An external interrupt request is latched as long as any source is holding the $\overline{IRQ}/V_{PP}$ pin low.

If level-sensitive triggering is selected, the $\overline{IRQ}/V_{PP}$ input requires an external resistor to V_{DD} for wired-OR operation. If the $\overline{IRQ}/V_{PP}$ pin is not used, it must be tied to the V_{DD} supply.

If edge-sensitive-only triggering is selected, a falling edge on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. A subsequent external interrupt request can be latched only after the voltage level on the $\overline{IRQ}/V_{PP}$ pin returns to logic 1 and then falls again to logic 0.

The $\overline{IRQ}/V_{PP}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin can affect the mode of operation and should not exceed V_{DD}.

8.3.2 Optional External Interrupts

The inputs for the lower four bits of port A (PA0–PA3) can be connected to the $\overline{IRQ}$ pin input of the CPU if enabled by the PIRQ bit in the mask option register. This capability allows keyboard scan applications where the transitions or levels on the I/O pins will behave the same as the $\overline{IRQ}/V_{PP}$ pin except for the inverted phase (logic 1, rising edge). The active state of the $\overline{IRQ}/V_{PP}$ pin is a logic 0 (falling edge).

The PA0–PA3 pins are selected as a group to function as IRQ interrupts and are enabled by the IRQE bit in the IRQ status and control register. The PA0–PA3 pins can be positive-edge triggered only or positive-edge and high-level triggered.

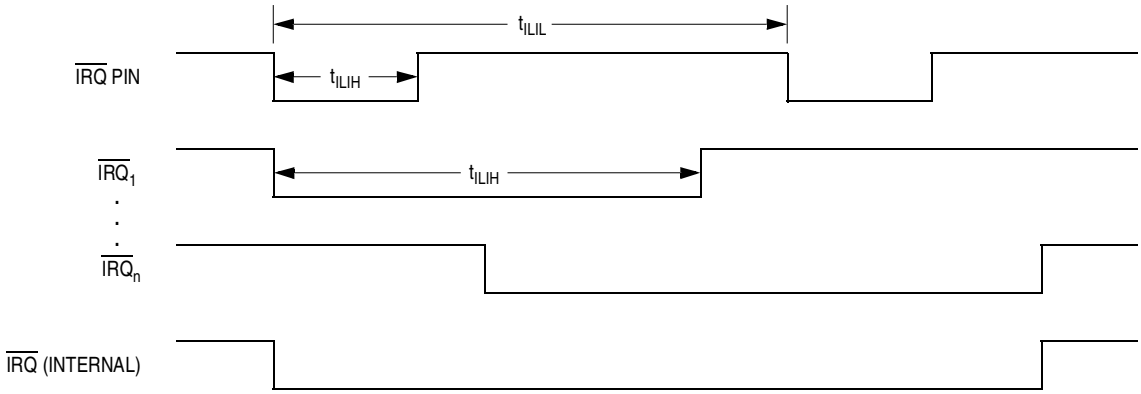
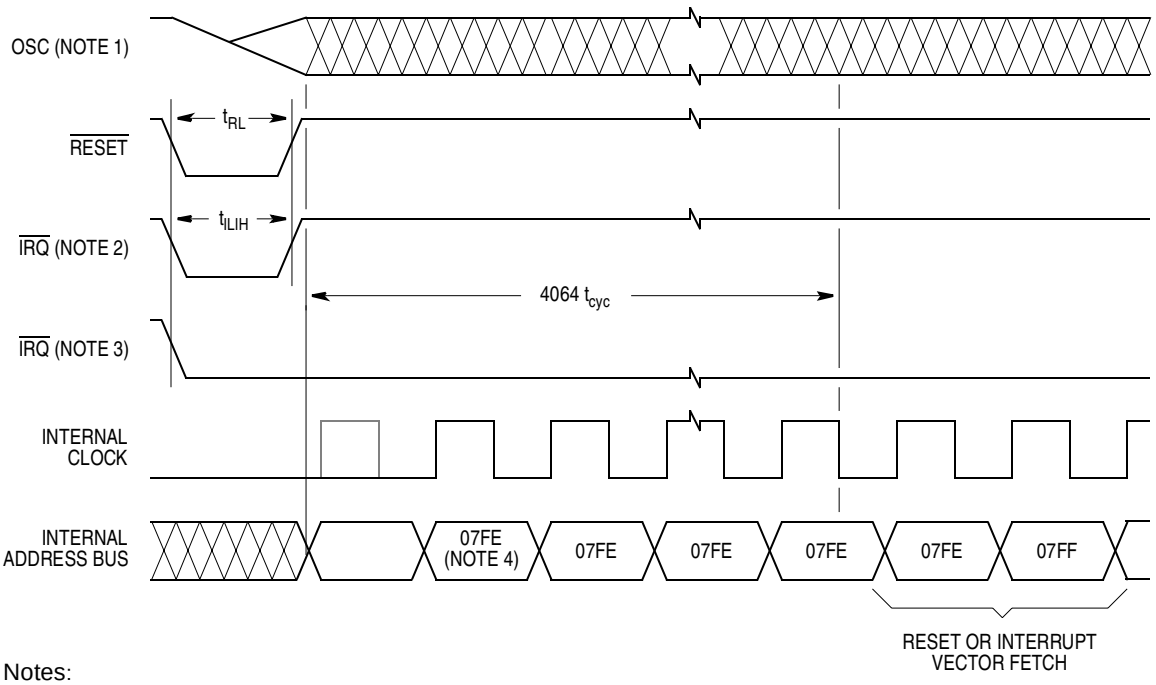


Figure 10-6. External Interrupt Timing



Notes:
1. Internal clocking from OSC1 pin
2. Edge-triggered external interrupt mask option
3. Edge- and level-triggered external interrupt mask option
4. Reset vector shown as example

Figure 10-7. Stop Mode Recovery Timing

Appendix B. MC68HSC705J1A

B.1 Contents

B.2 Introduction

This appendix introduces the MC68HSC705J1A, a high-speed version of the MC68HC705J1A. All of the information in this document applies to the MC68HSC705J1A with the exceptions given in this appendix.

C.7 Package Types and Order Numbers

Table C-1. MC68HSR705J1A (High-Speed RC Oscillator Option) Order Numbers(1)

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number
PDIP	738-03	20	0 to 70°C –40 to +85°C	MC68HSR705J1AP(2) MC68HSR705J1AC(3)P
SOIC	751D-04	20	0 to 70°C –40 to +85°C	MC68HSR705J1ADW(4) MC68HSR705J1ACDW
Cerdip	732-03	20	0 to 70°C –40 to +85°C	MC68HSR705J1AS(5) MC68HSR705J1ACS

1. Refer to **Section 12. Ordering Information** for standard part ordering information.
2. P = plastic dual in-line package (PDIP)
3. C = extended temperature range
4. DW = small outline integrated circuit (SOIC)
5. S = ceramic dual in-line package (cerdip)