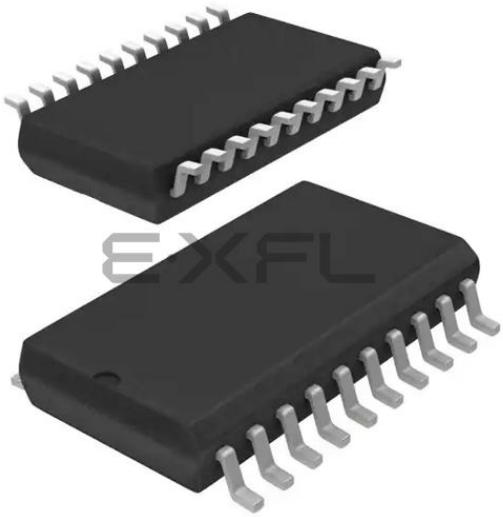

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705j1acdwe

Section 6. Parallel Input/Output (I/O) Ports

Section 7. Computer Operating Properly (COP) Module

Appendix B. MC68HSC705J1A

Appendix C. MC68HSR705J1A

Index

1.3 Features

Features of the MC68HC705J1A include:

- Peripheral modules:
  - 15-stage multifunction timer
  - Computer operating properly (COP) watchdog
- 14 bidirectional input/output (I/O) lines, including:
  - 10-mA sink capability on four I/O pins
  - Mask option register (MOR) and software programmable pulldowns on all I/O pins
  - MOR selectable interrupt on four I/O pins, a keyboard scan feature
- MOR selectable sensitivity on external interrupt (edge- and level-sensitive or edge-sensitive only)
- On-chip oscillator with connections for:
  - Crystal
  - Ceramic resonator
  - Resistor-capacitor (RC) oscillator
  - External clock
- 1240 bytes of EPROM/OTPROM, including eight bytes for user vectors
- 64 bytes of user random-access memory (RAM)
- Memory-mapped I/O registers
- Fully static operation with no minimum clock speed
- Power-saving stop, halt, wait, and data-retention modes
- External interrupt mask bit and acknowledge bit
- Illegal address reset
- Internal steering diode and pullup resistor from $\overline{\text{RESET}}$ pin to V_{DD}

1.5.2.3 RC Oscillator

Refer to **Appendix A. MC68HRC705J1A** and **Appendix C. MC68HSR705J1A**.

1.5.2.4 External Clock

An external clock from another complementary metal-oxide semiconductor (CMOS)-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in **Figure 1-8**. This configuration is possible regardless of whether the crystal/ceramic resonator or the RC oscillator is enabled.

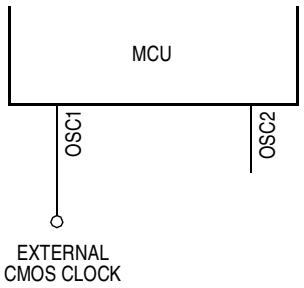


Figure 1-8. External Clock Connections

1.6 $\overline{\text{RESET}}$

Applying a logic 0 to the $\overline{\text{RESET}}$ pin forces the MCU to a known startup state. An internal reset also pulls the $\overline{\text{RESET}}$ pin low. An internal resistor to V_{DD} pulls the $\overline{\text{RESET}}$ pin high. A steering diode between the $\overline{\text{RESET}}$ and V_{DD} pins discharges any $\overline{\text{RESET}}$ pin voltage when power is removed from the MCU. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity as an input. Refer to **Section 4. Resets and Interrupts** for more information.

General Description

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0019	Unimplemented									
↓										
$001E	Unimplemented									
$001F	Reserved		R	R	R	R	R	R	R	R
$07F0	COP Register (COPR) See page 99.	Read:								
		Write:								COPC
		Reset:								0
$07F1	Mask Option Register (MOR) See page 41.	Read:	SOSCD	EPMSEC	OSCRES	SWAIT	SWPDI	PIRQ	LEVEL	COPEN
		Write:								
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved

Figure 2-2. I/O Register Summary (Sheet 3 of 3)

2.5 RAM

The 64 addresses from $00C0 to $00FF serve as both the user RAM and the stack RAM. Before processing an interrupt, the central processor unit (CPU) uses five bytes of the stack to save the contents of the CPU registers. During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements when the CPU stores a byte on the stack and increments when the CPU retrieves a byte from the stack.

NOTE: *Be careful when using nested subroutines or multiple interrupt levels. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.*

H — Half-Carry Flag

The CPU sets the half-carry flag when a carry occurs between bits 3 and 4 of the accumulator during an ADD (add without carry) or ADC (add with carry) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations.

I — Interrupt Mask Bit

Setting the interrupt mask disables interrupts. If an interrupt request occurs while the interrupt mask is logic 0, the CPU saves the CPU registers on the stack, sets the interrupt mask, and then fetches the interrupt vector. If an interrupt request occurs while the interrupt mask is logic 1, the interrupt request is latched. Normally, the CPU processes the latched interrupt request as soon as the interrupt mask is cleared again.

A return-from-interrupt instruction (RTI) unstacks the CPU registers, restoring the interrupt mask to its cleared state. After any reset, the interrupt mask is set and can be cleared only by a software instruction.

N — Negative Flag

The CPU sets the negative flag when an ALU operation produces a negative result.

Z — Zero Flag

The CPU sets the zero flag when an ALU operation produces a result of $00.

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some logical operations and data manipulation instructions also clear or set the carry/borrow flag.

3.7 Instruction Set Summary

Table 3-6. Instruction Set Summary (Sheet 1 of 6)

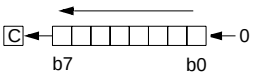
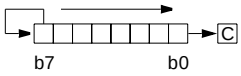
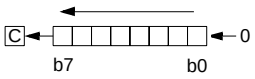
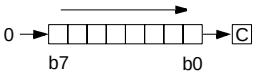
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X	Add with Carry	A ← (A) + (M) + (C)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X	Add without Carry	A ← (A) + (M)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #*opr* AND *opr* AND *opr* AND *opr*,X AND *opr*,X AND ,X	Logical AND	A ← (A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff 	5 3 3 6 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BCLR *n opr*	Clear Bit n	Mn ← 0	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? Z = 1	—	—	—	—	—	REL	27	rr	3
BHCC *rel*	Branch if Half-Carry Bit Clear	PC ← (PC) + 2 + *rel* ? H = 0	—	—	—	—	—	REL	28	rr	3
BHCS *rel*	Branch if Half-Carry Bit Set	PC ← (PC) + 2 + *rel* ? H = 1	—	—	—	—	—	REL	29	rr	3

Table 3-6. Instruction Set Summary (Sheet 4 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Unconditional Jump	PC ← Jump Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Effective Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	5 6 7 6 5
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
LSR *opr* LSRA LSRX LSR *opr*,X LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff 	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		11
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X	Negate Byte (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	—	—	↕	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	dd ff 	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3

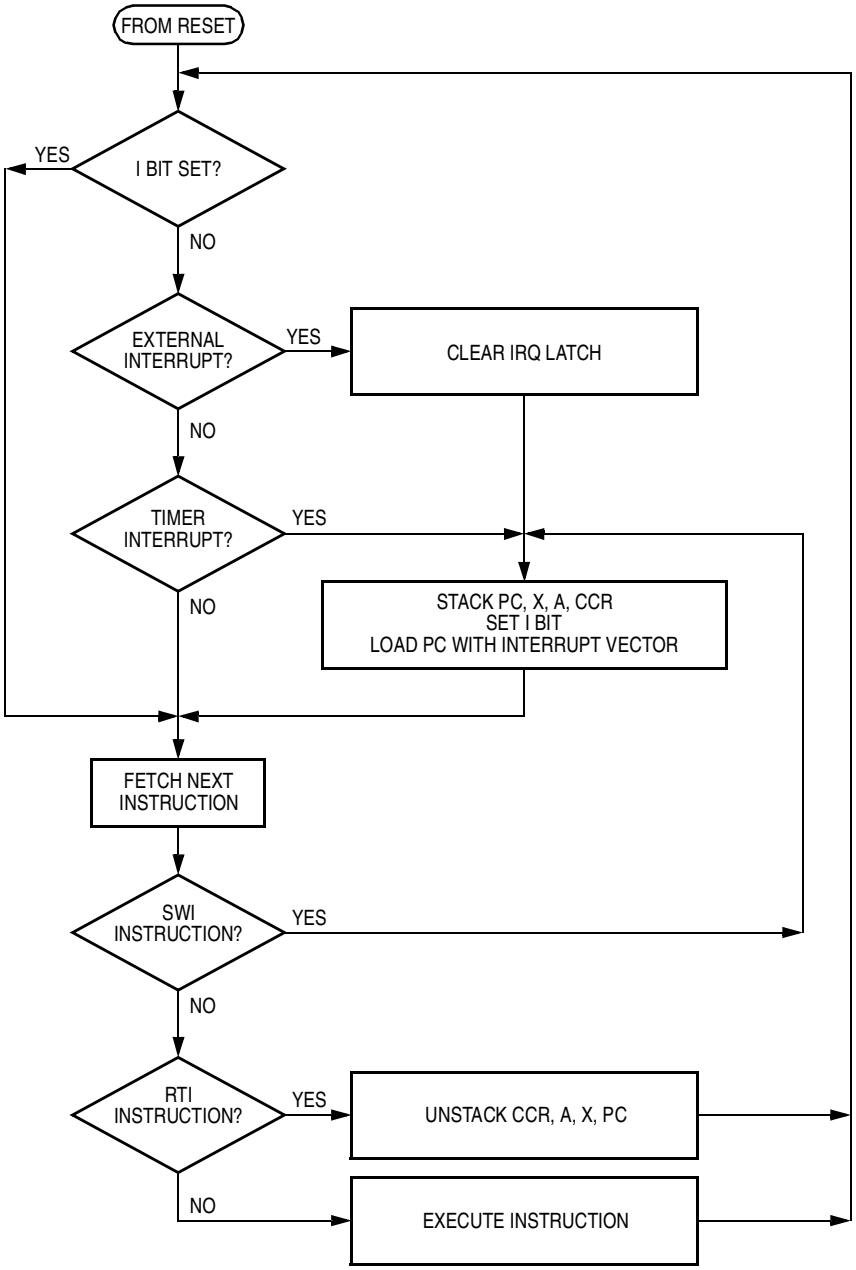


Figure 4-7. Interrupt Flowchart

7.6 Low-Power Modes

The STOP and WAIT instructions have these effects on the COP watchdog.

7.6.1 Stop Mode

The STOP instruction clears the COP watchdog counter and disables the clock to the COP watchdog.

NOTE: *To prevent the STOP instruction from disabling the COP watchdog, program the stop-to-wait conversion bit (SWAIT) in the mask option register to logic 1.*

Upon exit from stop mode by external reset:

- The counter begins counting from $0000.
- The counter is cleared again after the oscillator stabilization delay and begins counting from $0000 again.

Upon exit from stop mode by external interrupt:

- The counter begins counting from $0000.
- The counter is not cleared again after the oscillator stabilization delay and continues counting throughout the oscillator stabilization delay.

NOTE: *Immediately after exiting stop mode by external interrupt, service the COP to ensure a full COP timeout period.*

7.6.2 Wait Mode

The WAIT instruction has no effect on the COP watchdog.

NOTE: *To prevent a COP timeout during wait mode, exit wait mode periodically to service the COP.*

8.3 Operation

The interrupt request/programming voltage pin ($\overline{IRQ}/V_{PP}$) and port A pins 0–3 (PA0–PA3) provide external interrupts. The PIRQ bit in the mask option register (MOR) enables PA0–PA3 as IRQ interrupt sources, which are combined into a single ORing function to be latched by the IRQ latch. **Figure 8-1** shows the structure of the IRQ module.

After completing its current instruction, the CPU tests the IRQ latch. If the IRQ latch is set, the CPU then tests the I bit in the condition code register and the IRQE bit in the IRQ status and control register. If the I bit is clear and the IRQE bit is set, the CPU then begins the interrupt sequence. This interrupt is serviced by the interrupt service routine located at $07FA and $07FB.

The CPU clears the IRQ latch while it fetches the interrupt vector, so that another external interrupt request can be latched during the interrupt service routine. As soon as the I bit is cleared during the return from interrupt, the CPU can recognize the new interrupt request. **Figure 8-2** shows the sequence of events caused by an interrupt.

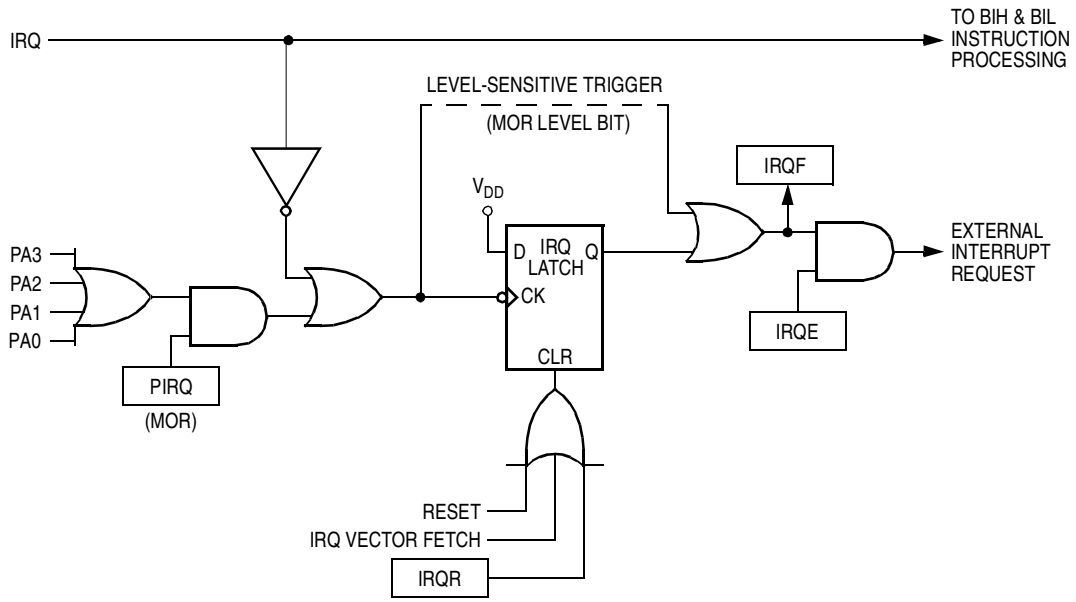


Figure 8-1. IRQ Module Block Diagram

External Interrupt Module (IRQ)

9.4 Interrupts

These timer sources can generate interrupts:

- Timer overflow flag (TOF) — The TOF bit is set when the first eight stages of the counter roll over from $FF to $00. The timer overflow interrupt enable bit, TOIE, enables TOF interrupt requests.
- Real-time interrupt flag (RTIF) — The RTIF bit is set when the selected RTI output becomes active. The real-time interrupt enable bit, RTIE, enables RTIF interrupt requests.

9.5 I/O Registers

These registers control and monitor the timer operation:

- Timer status and control register (TSCR)
- Timer counter register (TCR)

9.5.1 Timer Status and Control Register

The read/write timer status and control register (TSCR) performs these functions:

- Flags timer interrupts
- Enables timer interrupts
- Resets timer interrupt flags
- Selects real-time interrupt rates

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	RTIF	TOIE	RTIE	0	0	RT1	RT0
Write:					TOFR	RTIFR		
Reset:	0	0	0	0	0	0	1	1

= Unimplemented

Figure 9-3. Timer Status and Control Register (TSCR)

interrupt request to be generated. To prevent this occurrence, clear the COP timer before changing RT1 and RT0.

Table 9-1. Real-Time Interrupt Rate Selection

RT1:RT0	Number of Cycles to RTI	RTI Period(1)	Number of Cycles to COP Reset	COP Timeout Period(1)
0 0	2^{14} = 16,384	8.2 ms	2^{17} = 131,072	65.5 ms
0 1	2^{15} = 32,768	16.4 ms	2^{18} = 262,144	131.1 ms
1 0	2^{16} = 65,536	32.8 ms	2^{19} = 524,288	262.1 ms
1 1	2^{17} = 131,072	65.5 ms	2^{20} = 1,048,576	524.3 ms

1. At 2-MHz bus, 4-MHz XTAL, 0.5 µs per cycle

9.5.2 Timer Counter Register

A 15-stage ripple counter is the core of the timer. The value of the first eight stages is readable at any time from the read-only timer counter register (TCR) shown in **Figure 9-4**.

Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-4. Timer Counter Register (TCR)

Power-on clears the entire counter chain and the internal clock begins clocking the counter. After 4064 cycles (or 16 cycles if the SOSCD bit in the mask option register is set), the power-on reset circuit is released, clearing the counter again and allowing the MCU to come out of reset.

A timer overflow function at the eighth counter stage allows a timer interrupt every 1024 internal clock cycles.

10.4 Operating Temperature Range

Package Type	Symbol	Value (T_L to T_H)	Unit
MC68HC705J1AP(1), DW(2), S(3)	T_A	0 to 70	°C
MC68HC705J1AC(4)P, CDW, CS	T_A	–40 to +85	°C
MC68HC705J1AV(5)P, VDW, VS	T_A	–40 to +105	°C

1. P = plastic dual in-line package (PDIP)
2. DW = small outline integrated circuit (SOIC)
3. S = ceramic DIP (cerdip)
4. C = extended temperature range
5. V = automotive temperature range

10.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance MC68HC705J1AP(1) MC68HC705J1ADW(2) MC68HC705J1AS(3)	θ_{JA}	60	°C/W

1. P = plastic dual in-line package (PDIP)
2. DW = small outline integrated circuit (SOIC)
3. S = ceramic DIP (cerdip)

10.7 5.0-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD} – 0.1	 — —	 0.1 —	 V
Output high voltage (I_{Load} = –0.8 mA) PA0–PA7, PB0–PB5	V_{OH}	V_{DD} – 0.8	—	—	V
Output low voltage (I_{Load} = 1.6 mA) PA0–PA3, PB0–PB5 (I_{Load} = 10.0 mA) PA4–PA7	V_{OL}	—	—	0.4 0.4	V
Input high voltage PA0–PA7, PB0–PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current Run mode[3] Wait mode[4] Stop mode[5] 25°C –40 to 105°C	I_{DD}	 — — — —	 3.5 0.45 0.2 2.0	 6.0 2.75 10 20	 mA mA µA µA
I/O ports hi-z leakage current PA0–PA7, PB0–PB5 (without individual pulldown activated)	I_{IL}	—	0.2	±1	µA
Input pulldown current PA0–PA7, PB0–PB5 (with individual pulldown activated)	I_{IL}	35	80	200	µA
Input pullup current $\overline{RESET}$	I_{IL}	–15	–35	–85	µA
Input current[6] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{In}	—	0.2	±1	µA
Capacitance Ports (as inputs or outputs) $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1, OSC2	 C_{Out} C_{In}	 — —	 — —	 12 8	 pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2[7]	R_{osc}	1.0	2.0	3.0	MΩ

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source (f_{osc} = 4.2 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source (f_{osc} = 4.2 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V
6. Only input high current rated to +1 µA on $\overline{RESET}$.
7. The R_{osc} value selected for RC oscillator versions of this device is unspecified. See **Appendix C. MC68HSR705J1A** for additional information.

Section 12. Ordering Information

12.1 Contents

12.2 Introduction

This section contains ordering information for the available package types.

12.3 MCU Order Numbers

Table 12-1 lists the MC order numbers.

Table 12-1. Order Numbers

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number(1)
PDIP	738-03	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1AP(2) MC68HC705J1AC(3)P MC68HC705J1AV(4)P
SOIC	751D-04	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1ADW(5) MC68HC705J1ACDW MC68HC705J1AVDW
Cerdip	732-03	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1AS(6) MC68HC705J1ACS MC68HC705J1AVS

1. Refer to **Appendix A. MC68HRC705J1A**, **Appendix B. MC68HSC705J1A**, and **Appendix C. MC68HSR705J1A** for ordering information on optional high-speed and resistor-capacitor oscillator devices.
2. P = Plastic dual in-line package (PDIP)
3. C = Extended temperature range
4. V = Automotive temperature range
5. DW = Small outline integrated circuit (SOIC)
6. S = Ceramic dual in-line package (cerdip)

A.3 RC Oscillator Connections

For greater cost reduction, the RC oscillator mask option allows the configuration shown in **Figure A-1** to drive the on-chip oscillator. Mount the RC components as close as possible to the pins for startup stabilization and to minimize output distortion.

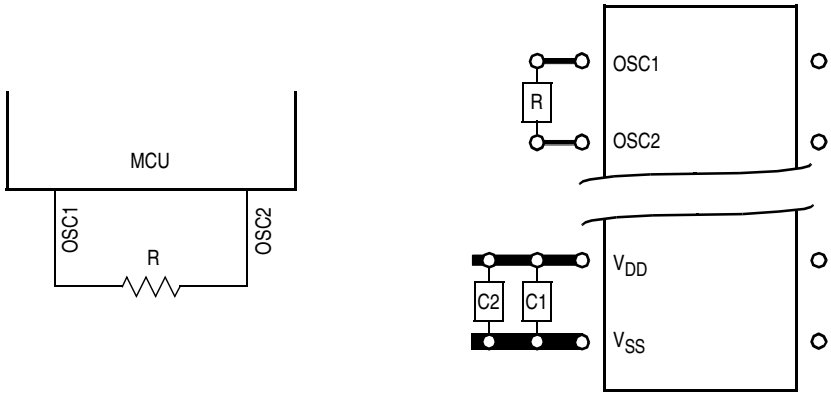


Figure A-1. RC Oscillator Connections

NOTE: *The optional internal resistor is **not** recommended for configurations that use the RC oscillator connections as shown in **Figure A-1**. For such configurations, the oscillator internal resistor (OSCRES) bit of the mask option register should be programmed to a logic 0.*