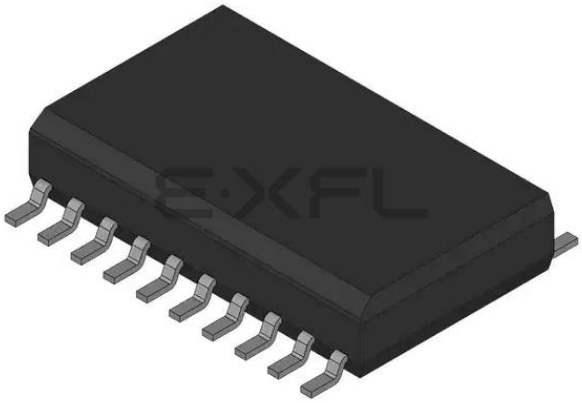


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mchrc705j1acdwe

List of Sections

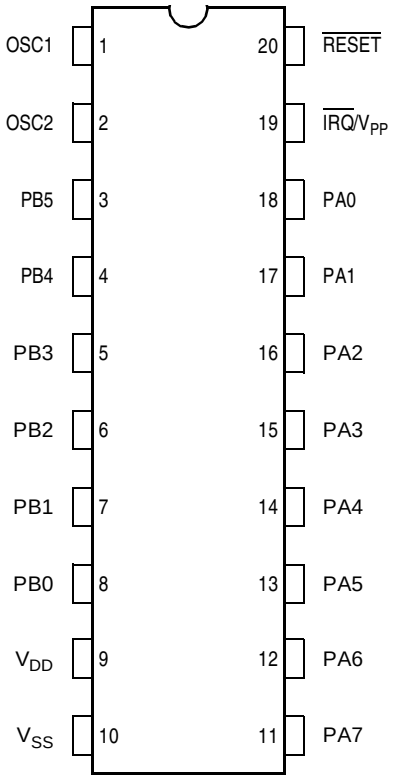


Figure 1-2. Pin Assignments

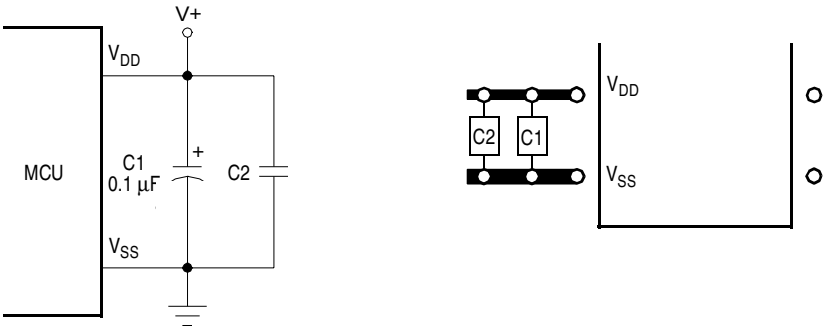


Figure 1-3. Bypassing Layout Recommendation

Take these steps to program the mask option register:

1. Apply the programming voltage, V_{PP}, to the $\overline{IRQ}/V_{PP}$ pin.
2. Write to the MOR.
3. Set the MPGM bit and wait for a time, t_{MPGM}.
4. Clear the MPGM bit.
5. Reset the MCU.

Address: $07F1

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SOSCD	EPMSEC	OSCRES	SWAIT	SWPDI	PIRQ	LEVEL	COPEN
Reset:	Unaffected by reset							

Figure 2-4. Mask Option Register (MOR)

SOSCD — Short Oscillator Delay Bit

The SOSCD bit controls the oscillator stabilization counter. The normal stabilization delay following reset or exit from stop mode is 4064 t_{cyc}. Setting SOSCD enables a short oscillator stabilization delay.

1 = Short oscillator delay enabled
0 = Short oscillator delay disabled

EPMSEC — EPROM Security Bit

The EPMSEC bit controls access to the EPROM/OTPROM.

1 = External access to EPROM/OTPROM denied
0 = External access to EPROM/OTPROM not denied

OSCRES — Oscillator Internal Resistor Bit

The OSCRES bit enables a 2-MΩ internal resistor in the oscillator circuit.

1 = Oscillator internal resistor enabled
0 = Oscillator internal resistor disabled

NOTE: *Program the OSCRES bit to logic 0 in devices using RC oscillators.*

Section 3. Central Processor Unit (CPU)

3.1 Contents

H — Half-Carry Flag

The CPU sets the half-carry flag when a carry occurs between bits 3 and 4 of the accumulator during an ADD (add without carry) or ADC (add with carry) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations.

I — Interrupt Mask Bit

Setting the interrupt mask disables interrupts. If an interrupt request occurs while the interrupt mask is logic 0, the CPU saves the CPU registers on the stack, sets the interrupt mask, and then fetches the interrupt vector. If an interrupt request occurs while the interrupt mask is logic 1, the interrupt request is latched. Normally, the CPU processes the latched interrupt request as soon as the interrupt mask is cleared again.

A return-from-interrupt instruction (RTI) unstacks the CPU registers, restoring the interrupt mask to its cleared state. After any reset, the interrupt mask is set and can be cleared only by a software instruction.

N — Negative Flag

The CPU sets the negative flag when an ALU operation produces a negative result.

Z — Zero Flag

The CPU sets the zero flag when an ALU operation produces a result of $00.

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some logical operations and data manipulation instructions also clear or set the carry/borrow flag.

4.3 Resets

A reset immediately stops the operation of the instruction being executed, initializes certain control and status bits, and loads the program counter with a user-defined reset vector address. These sources can generate a reset:

- Power-on reset (POR) circuit
- $\overline{\text{RESET}}$ pin
- Computer operating properly (COP) watchdog
- Illegal address

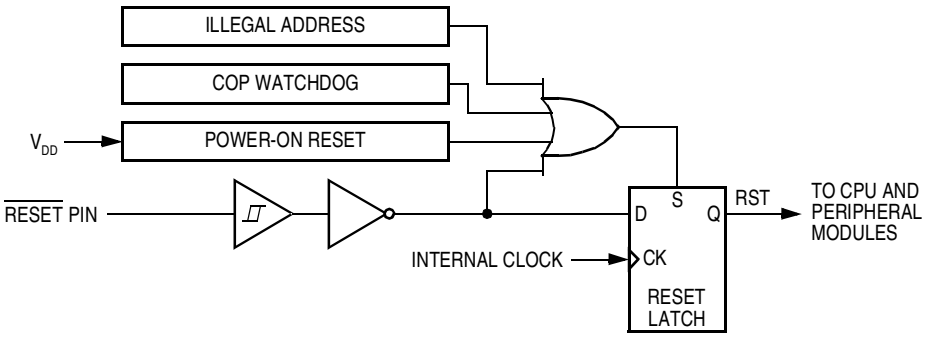


Figure 4-1. Reset Sources

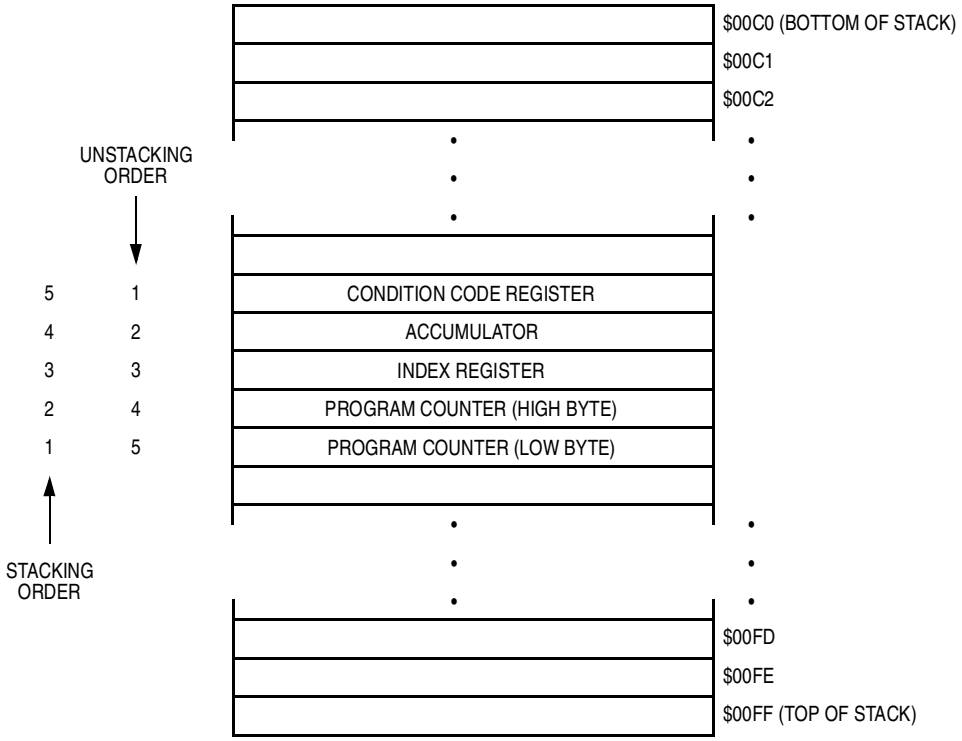


Figure 4-6. Interrupt Stacking Order

Table 4-4. Reset/Interrupt Vector Addresses

Function	Source	Local Mask	Global Mask	Priority (1 = Highest)	Vector Address
Reset	$\overline{\text{Power-on}}$ $\overline{\text{RESET}}$ pin COP watchdog[1] illegal address	None	None	1	$07FE–$07FF
Software interrupt (SWI)	User code	None	None	Same priority as instruction	$07FC–$07FD
External interrupt	$\overline{\text{IRQ}}/V_{PP}$ pin	IRQE	I bit	2	$07FA–$07FB
Timer interrupts	RTIF bit TOF bit	RTIE bit TOIE bit	I bit	3	$07F8–$07F9

1. The COP watchdog is programmable in the mask option register.

Section 5. Low-Power Modes

5.1 Contents

5.2 Introduction

The microcontroller unit (MCU) can enter these low-power standby modes:

- Stop mode — The STOP instruction puts the MCU in its lowest power-consumption mode.
- Wait mode — The WAIT instruction puts the MCU in an intermediate power-consumption mode.
- Halt mode — Halt mode is identical to wait mode, except that an oscillator stabilization delay of 1 to 4064 internal clock cycles occurs when the MCU exits halt mode. The stop-to-wait conversion bit, SWAIT, in the mask option register, enables halt mode.

5.4.2 CPU

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

After exit from stop mode by external interrupt, the I bit remains clear.

After exit from stop mode by reset, the I bit is set.

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts
- Disables the CPU clock

After exit from wait mode by interrupt, the I bit remains clear.

After exit from wait mode by reset, the I bit is set.

5.4.3 COP Watchdog

The STOP instruction:

- Clears the COP watchdog counter
- Disables the COP watchdog clock

NOTE: *To prevent the STOP instruction from disabling the COP watchdog, program the stop-to-wait conversion bit (SWAIT) in the mask option register to logic 1.*

After exit from stop mode by external interrupt, the COP watchdog counter immediately begins counting from $0000 and continues counting throughout the oscillator stabilization delay.

NOTE: *Immediately after exiting stop mode by external interrupt, service the COP to ensure a full COP timeout period.*

Section 6. Parallel Input/Output (I/O) Ports

6.1 Contents

6.2 Introduction

Fourteen bidirectional pins form one 8-bit input/output (I/O) port and one 6-bit I/O port. All the bidirectional port pins are programmable as inputs or outputs.

NOTE: *Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS}. Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.*

6.4.2 Data Direction Register B

Data direction register B (DDRB) determines whether each port B pin is an input or an output.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 6-7. Data Direction Register B (DDRB)

DDRB[5:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[5:0], configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured as input

NOTE: *Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1.*

Figure 6-8 shows the I/O logic of port B.

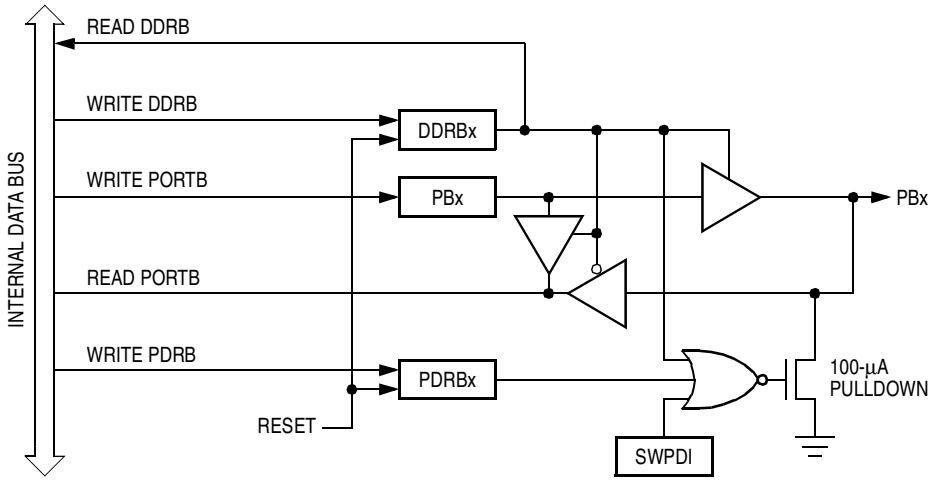


Figure 6-8. Port B I/O Circuitry

Section 9. Multifunction Timer Module

9.1 Contents

9.2 Introduction

The multifunction timer provides a timing reference with programmable real-time interrupt (RTI) capability. **Figure 9-1** shows the timer organization.

Features include:

- Timer overflow
- Four selectable interrupt rates
- Computer operating properly (COP) watchdog timer

10.4 Operating Temperature Range

Package Type	Symbol	Value (T_L to T_H)	Unit
MC68HC705J1AP(1), DW(2), S(3)	T_A	0 to 70	°C
MC68HC705J1AC(4)P, CDW, CS	T_A	–40 to +85	°C
MC68HC705J1AV(5)P, VDW, VS	T_A	–40 to +105	°C

1. P = plastic dual in-line package (PDIP)
2. DW = small outline integrated circuit (SOIC)
3. S = ceramic DIP (cerdip)
4. C = extended temperature range
5. V = automotive temperature range

10.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance MC68HC705J1AP(1) MC68HC705J1ADW(2) MC68HC705J1AS(3)	θ_{JA}	60	°C/W

1. P = plastic dual in-line package (PDIP)
2. DW = small outline integrated circuit (SOIC)
3. S = ceramic DIP (cerdip)

10.13 3.3-Volt Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{osc}	— dc	2.0 2.0	MHz
Internal operating frequency ($f_{osc} \div 2$) Crystal oscillator External clock	f_{op}	— dc	1.0 1.0	MHz
Cycle time ($1 \div f_{OP}$)	t_{cyc}	1000	—	ns
$\overline{\text{RESET}}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note[2]	t_{cyc}
PA0–PA3 interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note[2]	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	400	—	ns

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. The maximum width, t_{ILIL} or t_{ILIH}, should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.

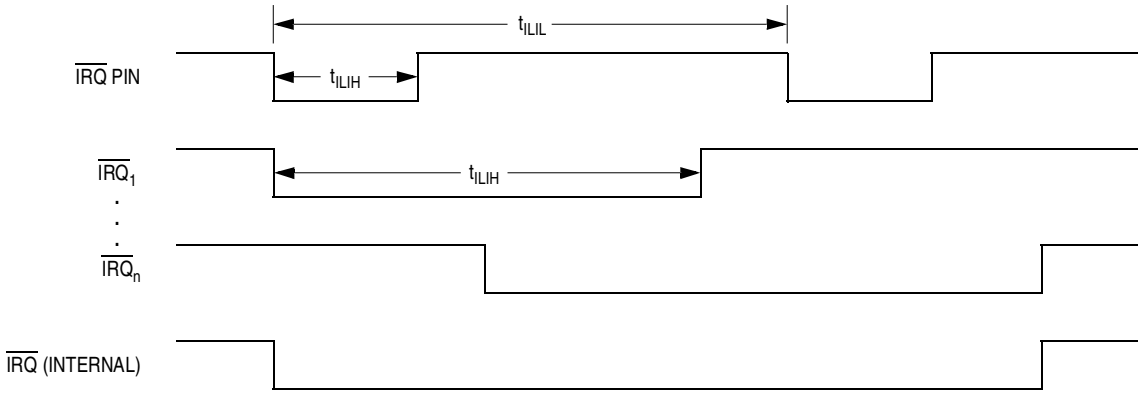
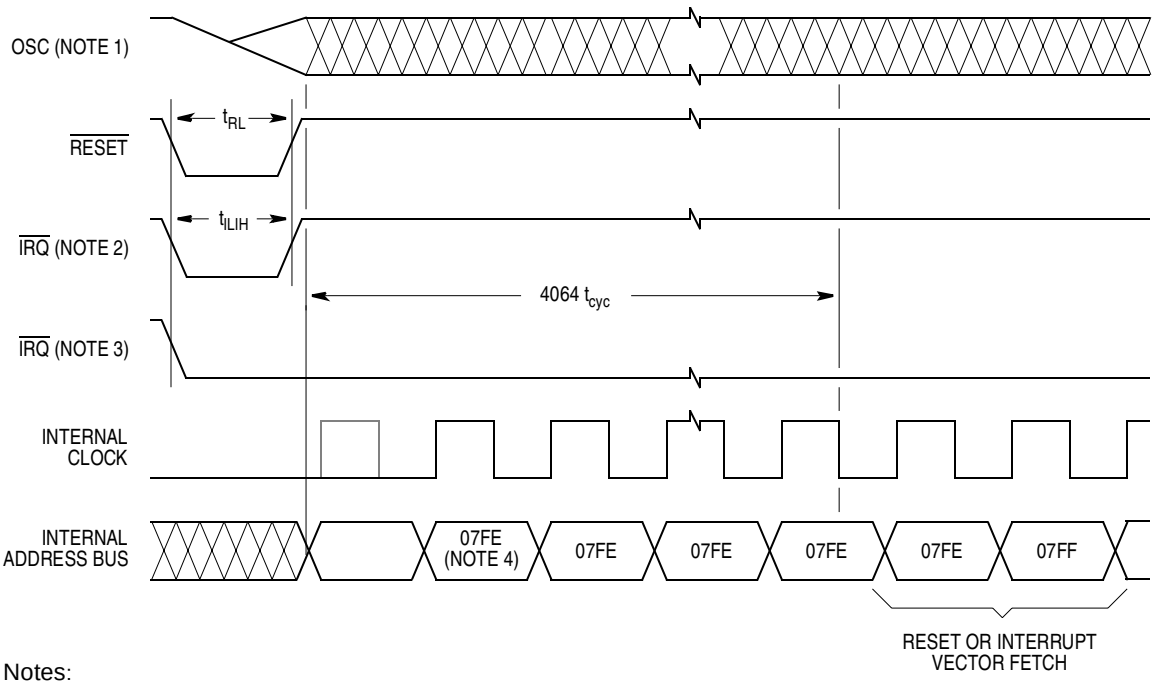


Figure 10-6. External Interrupt Timing



Notes:
1. Internal clocking from OSC1 pin
2. Edge-triggered external interrupt mask option
3. Edge- and level-triggered external interrupt mask option
4. Reset vector shown as example

Figure 10-7. Stop Mode Recovery Timing

Electrical Specifications

Section 11. Mechanical Specifications

11.1 Contents

11.2 Introduction

The MC68HC705J1A, the resistor-capacitor (RC) oscillator, and high-speed option devices described in **Appendix A. MC68HRC705J1A**, **Appendix B. MC68HSC705J1A**, and **Appendix C. MC68HSR705J1A** are available in the following packages:

- 738-03 — plastic dual in-line package (PDIP)
- 751D-04 — small outline integrated circuit (SOIC)
- 732-03 — ceramic DIP (cerdip) (windowed)

A.4 Typical Internal Operating Frequency for RC Oscillator Option

Figure A-2 shows typical internal operating frequencies at 25°C for the RC oscillator option.

NOTE: *Tolerance for resistance is ±50%. When selecting resistor size, consider the tolerance to ensure that the resulting oscillator frequency does not exceed the maximum operating frequency.*

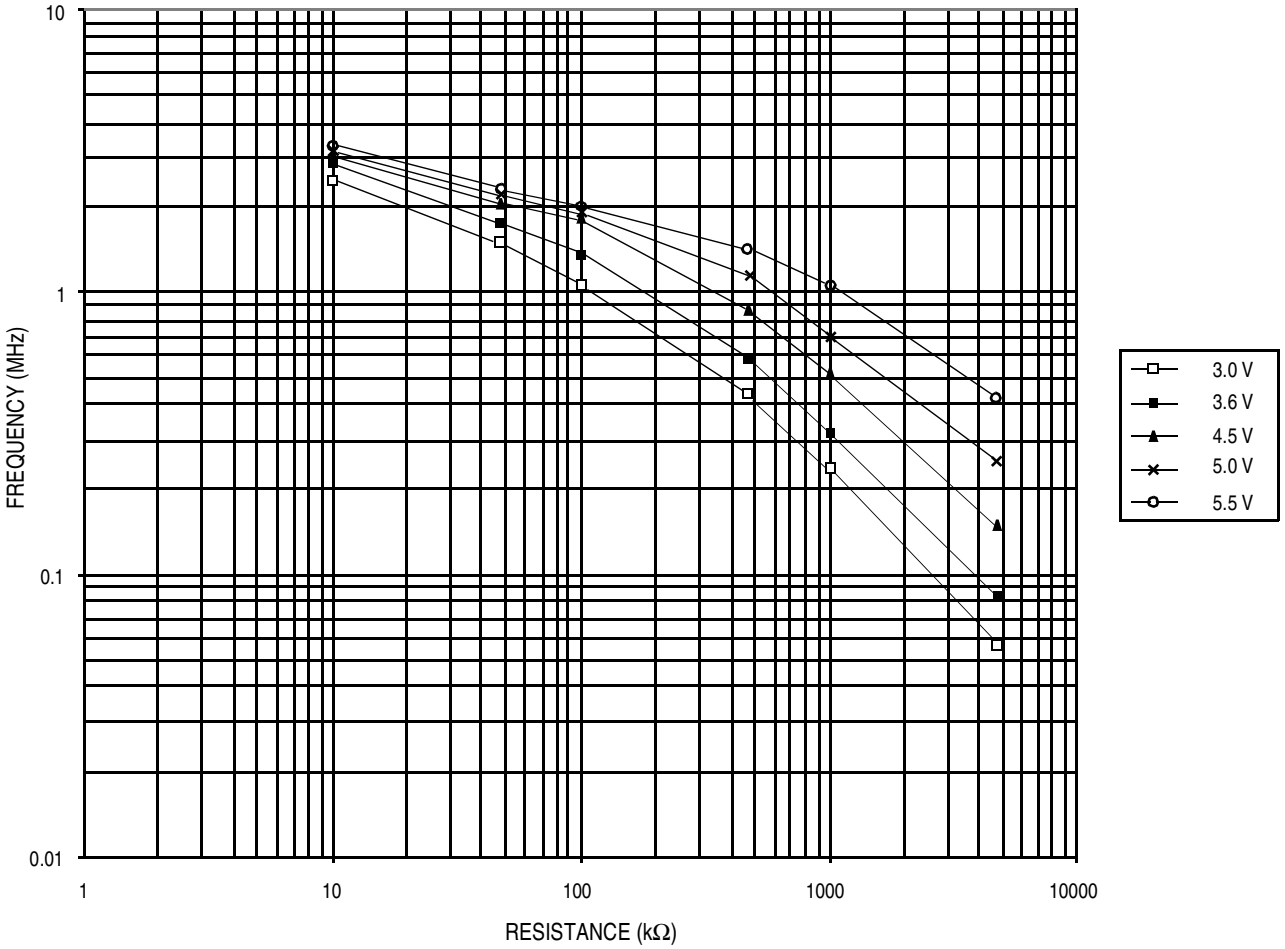


Figure A-2. Typical Internal Operating Frequency for Various V_{DD} at 25°C — RC Oscillator Option Only

C.6 Typical Internal Operating Frequency versus Temperature (No External Resistor)

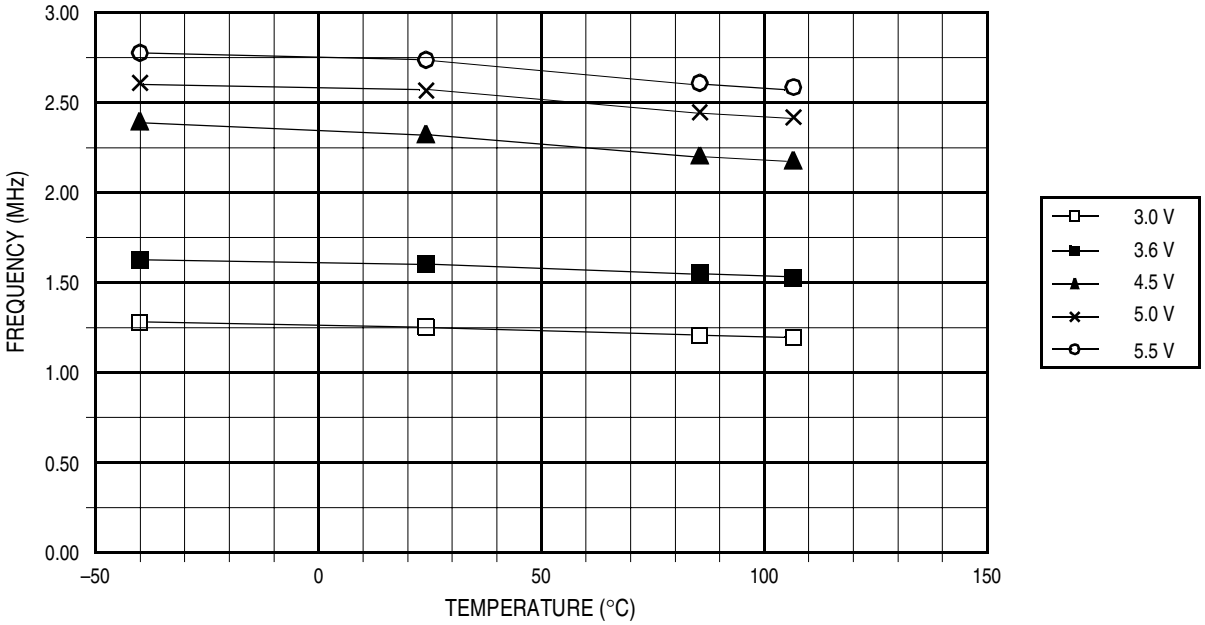


Figure C-3. Typical Internal Operating Frequency versus Temperature (OSCRES Bit = 1)

NOTE: *Due to process variations, operating voltages, and temperature requirements, the internal resistance and tolerance are unspecified. Typically for a given voltage and temperature, the frequency should not vary more than ±500 kHz. However, this data is not guaranteed. It is the user's responsibility to ensure that the resulting internal operating frequency meets the user's requirements.*

R